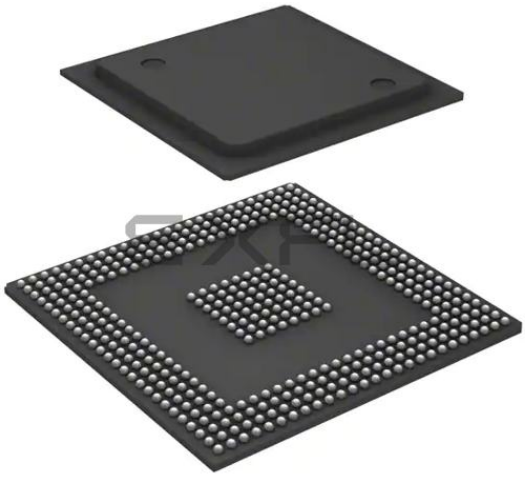

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What is "Embedded - Microcontrollers"?

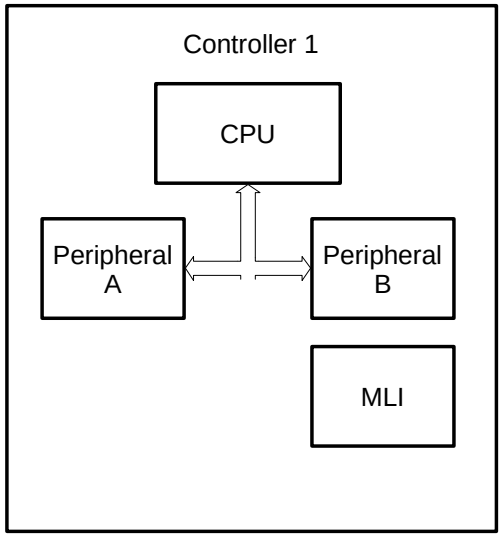
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	ASC, CANbus, EBI/EMI, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	123
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 44x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BBGA
Supplier Device Package	PG-BGA-416-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-tc1796-256f150e-bd

3.13 Micro Link Serial Bus Interface (MLI0, MLI1)

The Micro Link Interface (MLI) is a fast synchronous serial interface that allows to exchange data between microcontrollers of the 32-bit AUDO microcontroller family without intervention of a CPU or other bus masters. **Figure 12** shows how two microcontrollers are typically connected together via their MLI interfaces. The MLI operates in both microcontrollers as a bus master on the system bus.



MCA05869

Figure 12 Typical Micro Link Interface Connection

Features

- Synchronous serial communication between MLI transmitters and MLI receivers located on the same or on different microcontroller devices
- Automatic data transfer/request transactions between local/remote controller
- Fully transparent read/write access supported (= remote programming)
- Complete address range of remote controller available
- Specific frame protocol to transfer commands, addresses and data
- Error control by parity bit
- 32-bit, 16-bit, and 8-bit data transfers
- Programmable baud rate:
  - MLI transmitter baud rate: max. $f_{MLI}/2$ (= 37.5 Mbit/s @ 75 MHz module clock)
  - MLI receiver baud rate: max. f_{MLI}
- Multiple remote (slave) controllers supported

MLI transmitter and MLI receiver communicate with other off-chip MLI receivers and MLI transmitters via a 4-line serial I/O bus each. Several I/O lines of these I/O buses are available outside the MLI module kernel as four-line output or input buses.

Figure 13 shows the functional blocks of the two MLI modules with its interfaces.

3.14.1 Functionality of GPTA0/GPTA1

Each of the General Purpose Timer Arrays (GPTA0 and GPTA1) provides a set of hardware modules required for high speed digital signal processing:

- Filter and Prescaler Cells (FPC) support input noise filtering and prescaler operation.
- Phase Discrimination Logic units (PDL) decode the direction information output by a rotation tracking system.
- Duty Cycle Measurement Cells (DCM) provide pulse-width measurement capabilities.
- A Digital Phase Locked Loop unit (PLL) generates a programmable number of GPTA module clock ticks during an input signal's period.
- Global Timer units (GT) driven by various clock sources are implemented to operate as a time base for the associated Global Timer Cells.
- Global Timer Cells (GTC) can be programmed to capture the contents of a Global Timer on an external or internal event. A GTC may be also used to control an external port pin depending on the result of an internal compare operation. GTCs can be logically concatenated to provide a common external port pin with a complex signal waveform.
- Local Timer Cells (LTC) operating in Timer, Capture, or Compare Mode may be also logically tied together to drive a common external port pin with a complex signal waveform. LTCs — enabled in Timer Mode or Capture Mode — can be clocked or triggered by various external or internal events.

Input lines can be shared by an LTC and a GTC to trigger their programmed operation simultaneously.

The following sections summarize the specific features of the GPTA units. The clock signal f_{GPTA} is the input clock of the GPTA modules (max. 75 MHz in TC1796).

Clock Generation Unit

- Filter and Prescaler Cell (FPC)
  - Six independent units
  - Three basic operating modes: #
    Prescaler, Delayed Debounce Filter, Immediate Debounce Filter
  - Selectable input sources:#
    Port lines, GPTA module clock, FPC output of preceding FPC cell
  - Selectable input clocks:#
    GPTA module clock, prescaled GPTA module clock, DCM clock, compensated or uncompensated PLL clock.
  - $f_{GPTA}/2$ maximum input signal frequency in Filter Modes
- Phase Discriminator Logic (PDL)
  - Two independent units
  - Two operating modes (2 and 3 sensor signals)

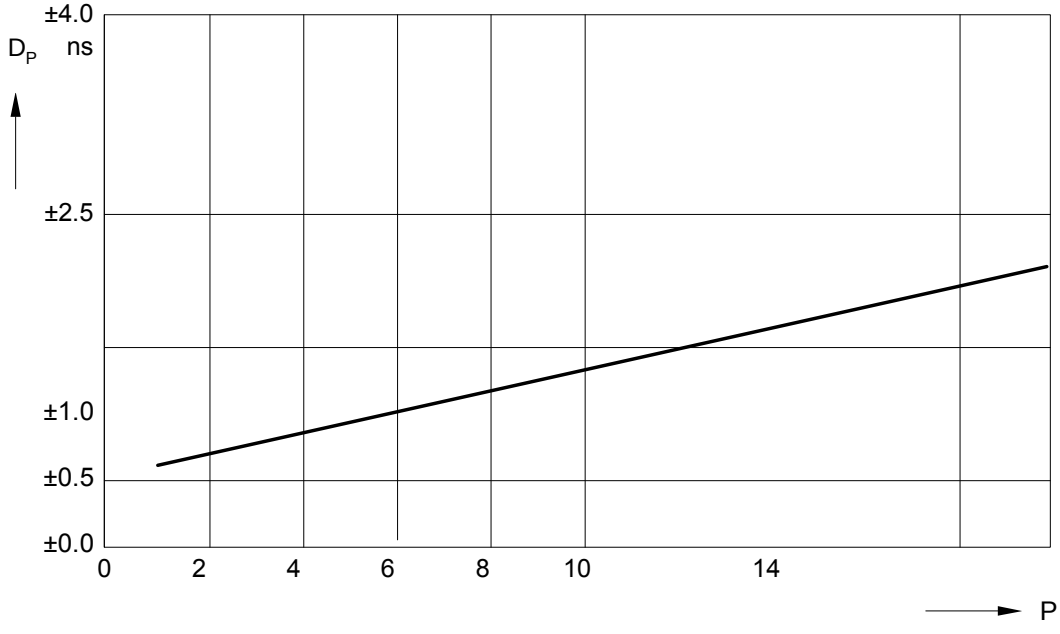


Figure 33 Approximated Maximum Accumulated PLL Jitter for Typical CPU Clock Frequencies f_{CPU} (detail)

Note: The specified PLL jitter values are valid if the capacitive load at the External Bus Unit (EBU) is limited to C_L=20pF.

Note: The maximum peak-to-peak noise on the Core Supply Voltage (measured between V_{DD} at pin E23 and V_{SS} at pin D23, or adjacent supply pairs) is limited to a peak-to-peak voltage of V_{PP} = 30mV. This condition can be achieved by appropriate blocking of the Core Supply Voltage as near as possible to the supply pins and using PCB supply and ground planes.=20pF.

4.3.6 BFCLKO Output Clock Timing

V_{SS} = 0 V;V_{DD} = 1.5 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%;#
T_A = -40 ∀C to +125 ∀C; C_L = 35 pF

Table 25 BFCLK0 Output Clock Timing Parameters[1)]

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
BFCLKO clock period	t_{BFCLKO}	CC	13.33[2)]	–	–	ns	–
BFCLKO high time	t_5	CC	3	–	–	ns	–
BFCLKO low time	t_6	CC	3	–	–	ns	–
BFCLKO rise time	t_7	CC	–	–	3	ns	–
BFCLKO fall time	t_8	CC	–	–	3	ns	–
BFCLKO duty cycle $t_5/(t_5 + t_6)$[3)]	DC24	CC	45	50	55	%	divider of 2, 4, ...[4)]
BFCLKO duty cycle $t_5/(t_5 + t_6)$[3)]	DC3	CC	30	33.33	36	%	divider of 3 [4)]
BFCLKO high time reduction[5)]	dt_5	CC	–	–	1.1	ns	C_L = 20pF

1) Not subject to production test, verified by design/characterization.
2) The PLL jitter characteristics add to this value according to the application settings. See the PLL jitter parameters.
3) The PLL jitter is not included in this parameter. If the BFCLKO frequency is equal to f_{CPU}, the K-divider setting determines the duty cycle.
4) The division ratio between LMB and BFCLKO frequency is set by EBU_BFCON.EXTCLOCK.
5) Due to asymmetry of the delays and slopes of the rising and falling edge of the pad. The influence of the PLL jitter is included in this parameter. This parameter should be applied taking the typical value of the duty cycle in the account, not the minimum or maximum value.

Figure 34 BFCLKO Output Clock Timing

4.3.8 JTAG Interface Timing

Operating Conditions apply, CL = 50 pF

Table 27 TCK Clock Timing Parameter

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TCK clock period[1)]	t_{TCK}	SR	25	–	–	ns	–
TCK high time	t_1	SR	10	–	–	ns	–
TCK low time	t_2	SR	10	–	–	ns	–
TCK clock rise time	t_3	SR	–	–	4	ns	–
TCK clock fall time	t_4	SR	–	–	4	ns	–

1) f_{TCK} should be lower or equal to f_{SYS}.

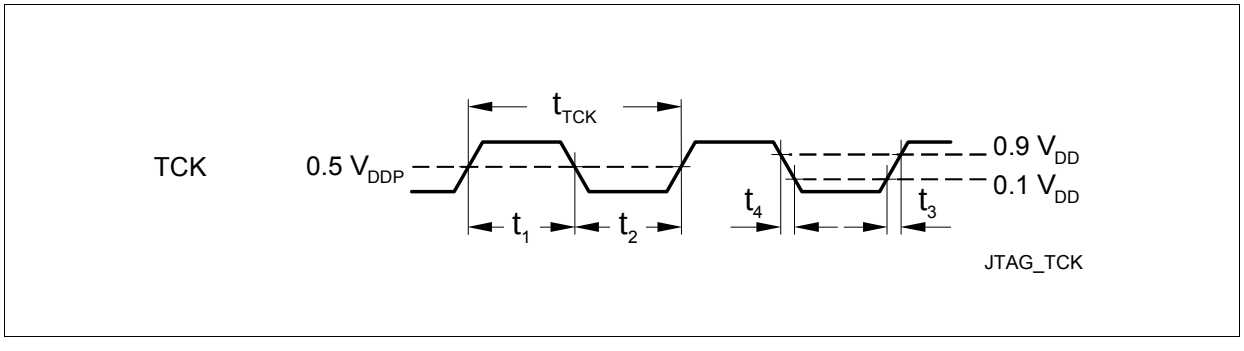


Figure 36 TCK Clock Timing