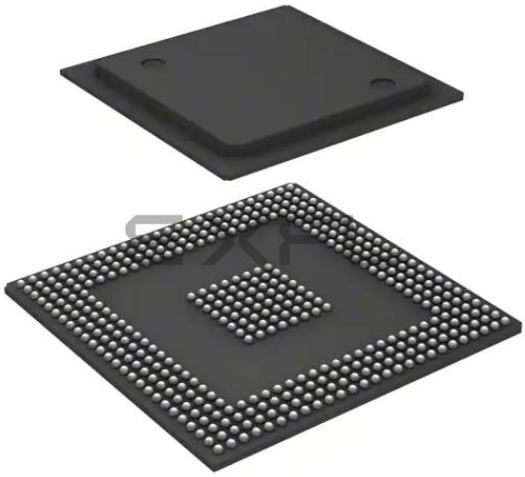
Infeon Technologies - TC1796256F150EBCKDUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	ASC, CANbus, EBI/EMI, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	123
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 44x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BGA
Supplier Device Package	PG-BGA-416
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1796256f150ebckduma1

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC1796 please refer to the **“Product Catalog Microcontrollers”**, which summarizes all available microcontroller variants.

This document describes the derivatives of the device.The **Table 1** enumerates these derivatives and summarizes the differences.

Table 1 TC1796 Derivative Synopsis

Derivative	Ambient Temperature Range
SAK-TC1796-256F150E	T_A = -40°C to +125°C

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
BFCLKO	AF25	O	B2	V_{DDEBU}	**Burst Mode Flash Clock Output (non-differential)**
BFCLKI	AF24	I	B1		**Burst Mode Flash Clock Input** (feedback clock)
$\overline{RD}$	AF20	O	B1		**Read Control Line**
RD/$\overline{WR}$	AF21	O	B1		**Write Control Line**
$\overline{ADV}$	AF22	O	B1		Address Valid Output
MR/$\overline{W}$	AF19	O	B1		**Motorola-style Read/Write Control Signal**
			B1		**Byte Control Lines**
$\overline{BC0}$	AE17	O			Byte control line 0
$\overline{BC1}$	AD17	O			Byte control line 1
$\overline{BC2}$	AF18	O			Byte control line 2
$\overline{BC3}$	AE18	O			Byte control line 3
$\overline{WAIT}$	AE20	I	B1		**Wait Input for inserting Wait-States**
$\overline{BAA}$	AF23	O	B1		**Burst Address Advance Output**
$\overline{HOLD}$	AF17	I	B1		**Hold Request Input**
$\overline{HLDA}$	AD18	O	B1		**Hold Acknowledge Output**
$\overline{BREQ}$	AD22	O	B1		**Bus Request Output**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions	
P5		I/O	A2	V_{DDP}	**Port 5** Port 5 is an 8-bit bi-directional general-purpose I/O port which can be alternatively used for ASC0/1 or MSC0/1 lines.	
P5.0	B13	I/O			RXD0A	ASC0 receiver input / output A
P5.1	A13	O			TXD0A	ASC0 transmitter output A
P5.2	A14	I/O			RXD1A	ASC1 receiver input / output A
P5.3	B14	O			TXD1A	ASC1 transmitter output A P5.3 is latched with the rising edge of $\overline{\text{PORST}}$ if BYPASS = 1 and stored in inverted state as bit OSC_CON.MOSC.
P5.4	C15	O			EN00	MSC0 device select output 0
		O			RREADY0B	MLI0 receive channel ready output B
P5.5	C14	I			SDI0	MSC0 serial data input
P5.6	B15	O			EN10	MSC1 device select output 0
		O			TVALID0B	MLI0 transmit channel valid output B
P5.7	A15	I			SDI1	MSC1 serial data input

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
P10		I	A1	V_{DDP}	**Hardware Configuration Inputs / Port 10** These inputs are boot mode (hardware configuration) control inputs. They are latched with the rising edge of HDRST.
P10.0	A21	I			Port 10 input line 0 / HWCFG0
P10.1	B21	I			Port 10 input line 1 / HWCFG1
P10.2	C21	I			Port 10 input line 2 / HWCFG2
P10.3	D21	I			Port 10 input line 3 / HWCFG3 After reset (HDRST = 1) the state of the Port 10 input pins may be modified from the reset configuration state. There actual state can be read via software (P10_IN register). During normal operation input HWCFG1 serves as emergency shut-off control input for certain I/O lines (e.g. GPTA related outputs).
Dedicated Peripheral I/Os					
SLSO0	AE14	O	A2	V_{DDP}	**SSC0 Slave Select Output Line 0**
SLSO1	AC15	O			**SSC0 Slave Select Output Line 1**
MTSR0	AF15	O I			**SSC0 Master Transmit Output / SSC0 Slave Receive Input**
MRST0	AE15	I O			**SSC0 Master Receive Input / SSC0 Slave Transmit Output**
SCLK0	AF14	I/O			**SSC0 Clock Input/Output**
SLSI0	AD15	I			**SSC0 Slave Select Input**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
			D	–	**ADC Analog Input Port (cont'd)**
AN32	AC3	I			Analog input 32
AN33	AE2	I			Analog input 33
AN34	AD3	I			Analog input 34
AN35	AD5	I			Analog input 35
AN36	AE3	I			Analog input 36
AN37	AF2	I			Analog input 37
AN38	AC4	I			Analog input 38
AN39	AF3	I			Analog input 39
AN40	AD4	I			Analog input 40
AN41	AE4	I			Analog input 41
AN42	AC5	I			Analog input 42
AN43	AF4	I			Analog input 43
TR[15:0]		O	A3	V_{DDP}	**OCDS Level 2 Debug Trace Lines**[2] (located on center balls)
TR0	U12	O			Trace output line 0
TR1	T12	O			Trace output line 1
TR2	U11	O			Trace output line 2
TR3	T11	O			Trace output line 3
TR4	U10	O			Trace output line 4
TR5	R12	O			Trace output line 5
TR6	R10	O			Trace output line 4
TR7	R11	O			Trace output line 7
TR8	M11	O			Trace output line 8
TR9	M10	O			Trace output line 9
TR10	L11	O			Trace output line 10
TR11	L10	O			Trace output line 11
TR12	K10	O			Trace output line 12
TR13	K11	O			Trace output line 13
TR14	L12	O			Trace output line 14
TR15	K12	O			Trace output line 15
TRCLK	T10	O	A4		**Trace Clock for OCDS Level 2 Debug Trace Lines**[1] (located on a center ball)

3.10 High-Speed Synchronous Serial Interfaces (SSC0, SSC1)

Figure 9 shows a global view of the functional blocks and interfaces of the two High-Speed Synchronous Serial interfaces SSC0 and SSC1.

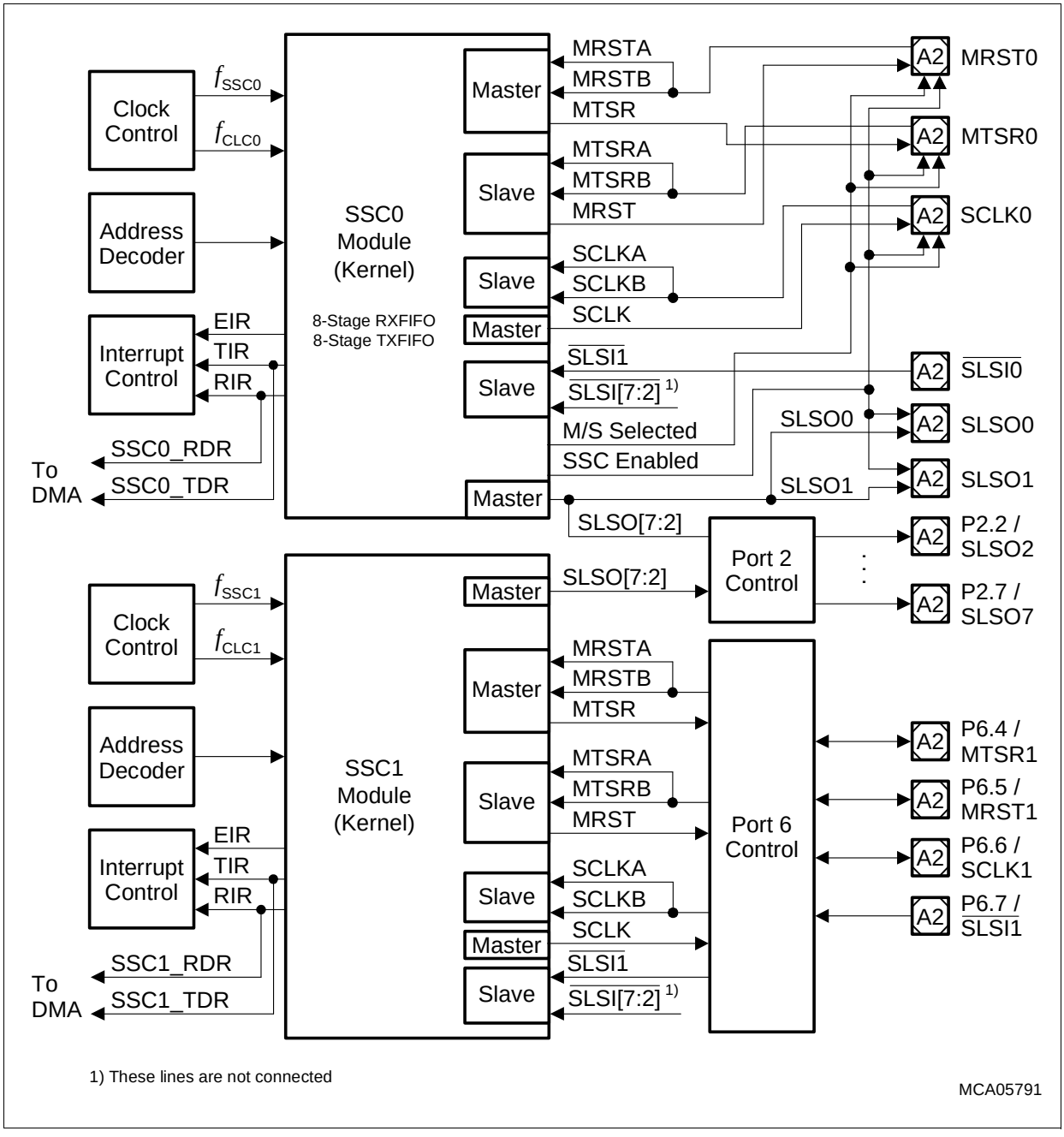

Figure 9 Block Diagram of the SSC Interfaces

The SSC allows full-duplex and half-duplex serial synchronous communication up to 37.5 Mbit/s (@ 75 MHz module clock) with Receive and Transmit FIFO support. (FIFO only in SSC0). The serial clock signal can be generated by the SSC itself (Master Mode)

The downstream and upstream channels of the MSC module communicate with the external world via nine I/O lines. Eight output lines are required for the serial communication of the downstream channel (clock, data, and enable signals). One out of eight input lines SDI[7:0] is used as serial data input signal for the upstream channel. The source of the serial data to be transmitted by the downstream channel can be MSC register contents or data that is provided at the ALTINL/ALTINH input lines. These input lines are typically connected to other on-chip peripheral units (for example with a timer unit like the GPTA). An emergency stop input signal allows to set bits of the serial data stream to dedicated values in emergency case.

Clock control, address decoding, and interrupt service request control are managed outside the MSC module kernel. Service request outputs are able to trigger an interrupt or a DMA request.

Features

- Fast synchronous serial interface to connect power switches in particular, or other peripheral devices via serial buses
- High-speed synchronous serial transmission on downstream channel
  - Maximum serial output clock frequency: $f_{FCL} = f_{MSC}/2$ (= 37.5 Mbit/s @ 75 MHz module clock)
  - Fractional clock divider for precise frequency control of serial clock f_{MSC}
  - Command, data, and passive frame types
  - Start of serial frame: Software-controlled, timer-controlled, or free-running
  - Programmable upstream data frame length (16 or 12 bits)
  - Transmission with or without SEL bit
  - Flexible chip select generation indicates status during serial frame transmission
  - Emergency stop without CPU intervention
- Low-speed asynchronous serial reception on upstream channel
  - Baud rate: f_{MSC} divided by 8, 16, 32, 64, 128, 256, or 512
  - Standard asynchronous serial frames
  - Parity error checker
  - 8-to-1 input multiplexer for SDI lines
  - Built-in spike filter on SDI lines

3.12 MultiCAN Controller (CAN)

Figure 11 shows a global view of the MultiCAN module with its functional blocks and interfaces.

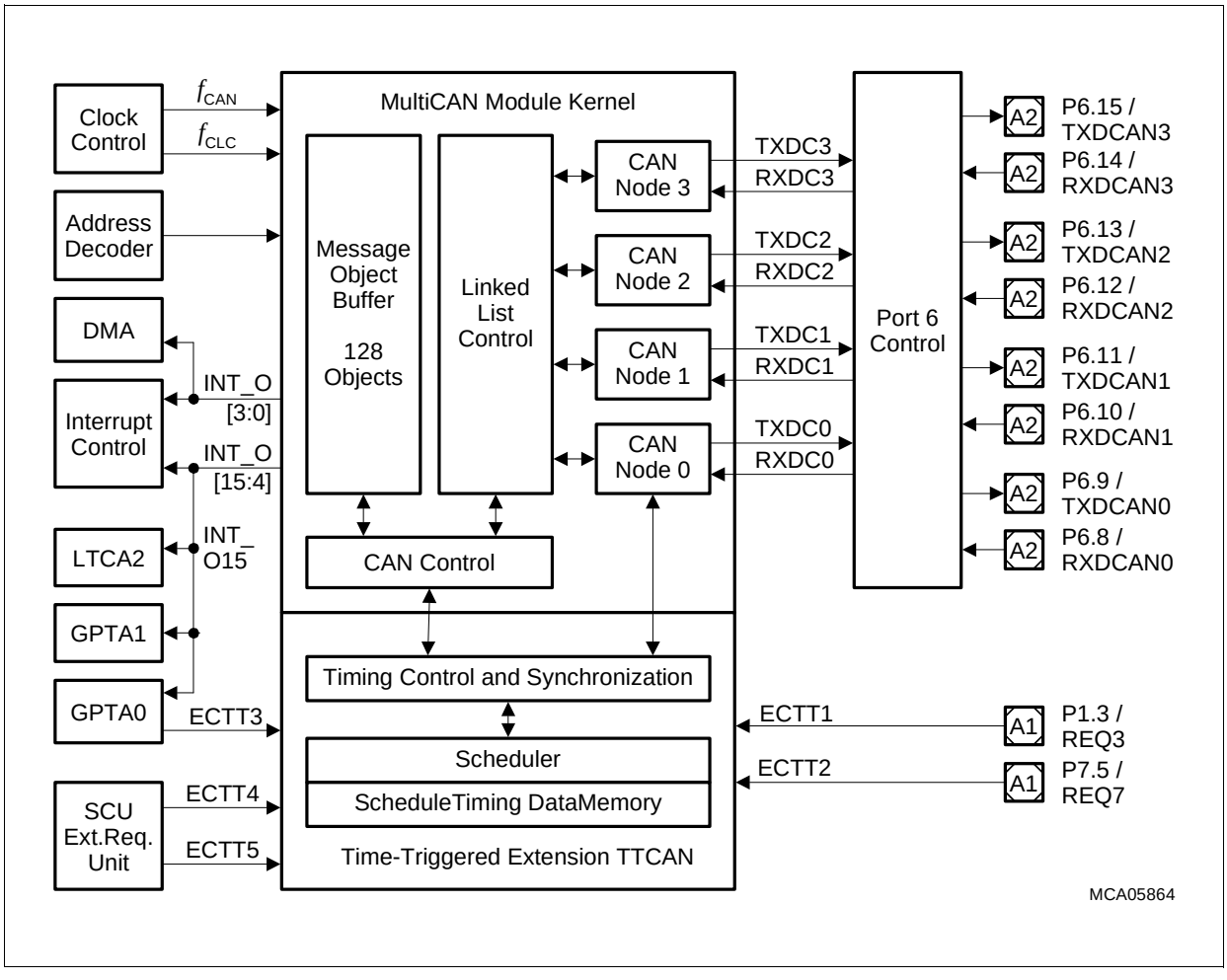

Figure 11 Block Diagram of MultiCAN Module with Time-Triggered Extension

The MultiCAN module contains four independently operating CAN nodes with Full-CAN functionality that are able to exchange Data and Remote Frames via a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All four CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to setup a FIFO buffer.

The message objects are organized in double-chained linked lists, where each CAN node has it's own list of message objects. A CAN node stores frames only into message

The A/D converters operate by the method of the successive approximation. A multiplexer selects between up to 32 analog inputs that can be connected with the 16 conversion channels in each ADC module. An automatic self-calibration adjusts the ADC modules to changing temperatures or process variations.

External Clock control, address decoding, and service request (interrupt) control is managed outside the ADC module kernel. A synchronization bridge is used for synchronization of two ADC modules. External trigger conditions are controlled by an External Request Unit. This unit generates the control signals for auto-scan control (ASGT), software trigger control (SW0TR, SW0GT), the event trigger control (ETR, EGT), queue control (QTR, QGT), and timer trigger control (TTR, TGT).

Features

- 8-bit, 10-bit, 12-bit A/D conversion
- Minimum conversion times (without sample time, @ 75 MHz module clock):
  - 1.05 µs @ 8-bit resolution
  - 1.25 µs @ 10-bit resolution
  - 1.45 µs @ 12-bit resolution
- Extended channel status information on request source
- Successive approximation conversion method
- Total Unadjusted Error (TUE) of ±2 LSB @ 10-bit resolution
- Integrated sample & hold functionality
- Direct control of up to 16(32) analog input channels per ADC
- Dedicated control and status registers for each analog channel
- Powerful conversion request sources
- Selectable reference voltages for each channel
- Programmable sample and conversion timing schemes
- Limit checking
- Flexible ADC module service request control unit
- Synchronization of the two on-chip A/D converters
- Automatic control of external analog multiplexers
- Equidistant samples initiated by timer
- External trigger and gating inputs for conversion requests
- Power reduction and clock control feature
- On-chip die temperature sensor output voltage measurement via ADC1

3.18 Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failure. The WDT helps to abort an accidental malfunction of the TC1796 in a user-specified time period. When enabled, the WDT will cause the TC1796 system to be reset if the WDT is not serviced within a user-programmable time period. The CPU must service the WDT within this time interval to prevent the WDT from causing a TC1796 system reset. Hence, routine service of the WDT confirms that the system is functioning properly.

In addition to this standard “Watchdog” function, the WDT incorporates the EndInit feature and monitors its modifications. A system-wide line is connected to the End-of-Initialization (Endinit) feature and monitors its modifications. A system-wide line is connected to the WDT_CON0.ENDINIT bit, serving as an additional write-protection for critical registers (besides Supervisor Mode protection)

A further enhancement in the TC1796’s WDT is its reset pre-warning operation. Instead of immediately resetting the device on the detection of an error (the way that standard Watchdogs do), the WDT first issues an Non-Maskable Interrupt (NMI) to the CPU before finally resetting the device at a specified time period later. This gives the CPU a chance to save system state to memory for later examination of the cause of the malfunction, an important aid in debugging.

Features

- 16-bit Watchdog counter
- Selectable input frequency: f_{SYS}/256 or f_{SYS}/16384
- 16-bit user-definable reload value for normal Watchdog operation, fixed reload value for Time-Out and Pre-warning Modes
- Incorporation of the ENDINIT bit and monitoring of its modifications
- Sophisticated password access mechanism with fixed and user-definable password fields
- Proper access always requires two write accesses. The time between the two accesses is monitored by the WDT and limited.
- Access Error Detection: Invalid password (during first access) or invalid guard bits (during second access) trigger the Watchdog reset generation.
- Overflow Error Detection: An overflow of the counter triggers the Watchdog reset generation.
- Watchdog function can be disabled; access protection and ENDINIT monitor function remain enabled.
- Double Reset Detection: If a Watchdog induced reset occurs twice, a severe system malfunction is assumed and the TC1796 is held in reset until a power-on reset. This prevents the device from being periodically reset if, for instance, connection to the external memory has been lost such that even system initialization could not be performed

3.21 Power Management System

The TC1796 power management system allows software to configure the various processing units so that they automatically adjust to draw the minimum necessary power for the application. There are three power management modes:

- Run Mode
- Idle Mode
- Sleep Mode

The operation of each system component in each of these states can be configured by software. The power-management modes provide flexible reduction of power consumption through a combination of techniques, including stopping the CPU clock, stopping the clocks of other system components individually, and individually clock-speed reduction of some peripheral components.

Besides these explicit software-controlled power-saving modes, in the TC1796 special attention has been paid for automatic power-saving in those operating units which are currently not required or idle. In that case they are shut off automatically until their operation is required again.

Table 8 describes the features of the power management modes.

Table 8 Power Management Mode Summary

Mode	Description
Run	The system is fully operational. All clocks and peripherals are enabled, as determined by software.
Idle	The CPU clock is disabled, waiting for a condition to return it to Run Mode. Idle Mode can be entered by software when the processor has no active tasks to perform. All peripherals remain powered and clocked. Processor memory is accessible to peripherals. A reset, Watchdog Timer event, a falling edge on the NMI pin, or any enabled interrupt event will return the system to Run Mode.
Sleep	The system clock signal is distributed only to those peripherals programmed to operate in Sleep Mode. The other peripheral module will be shut down by the suspend signal. Interrupts from operating peripherals, the Watchdog Timer, a falling edge on the NMI pin, or a reset event will return the system to Run Mode. Entering this state requires an orderly shut-down controlled by the Power Management State Machine.

In typical operation, Idle Mode and Sleep Mode may be entered and exited frequently during the run time of an application. For example, system software will typically cause the CPU to enter Idle Mode each time it has to wait for an interrupt before continuing its tasks. In Sleep Mode and Idle Mode, wake-up is performed automatically when any enabled interrupt signal is detected, or if the Watchdog Timer signals the CPU with an NMI trap.

are derived from f_{VCO} only by the K-Divider. In this mode, the system clock f_{SYS} can be equal to f_{CPU} or $f_{CPU}/2$.

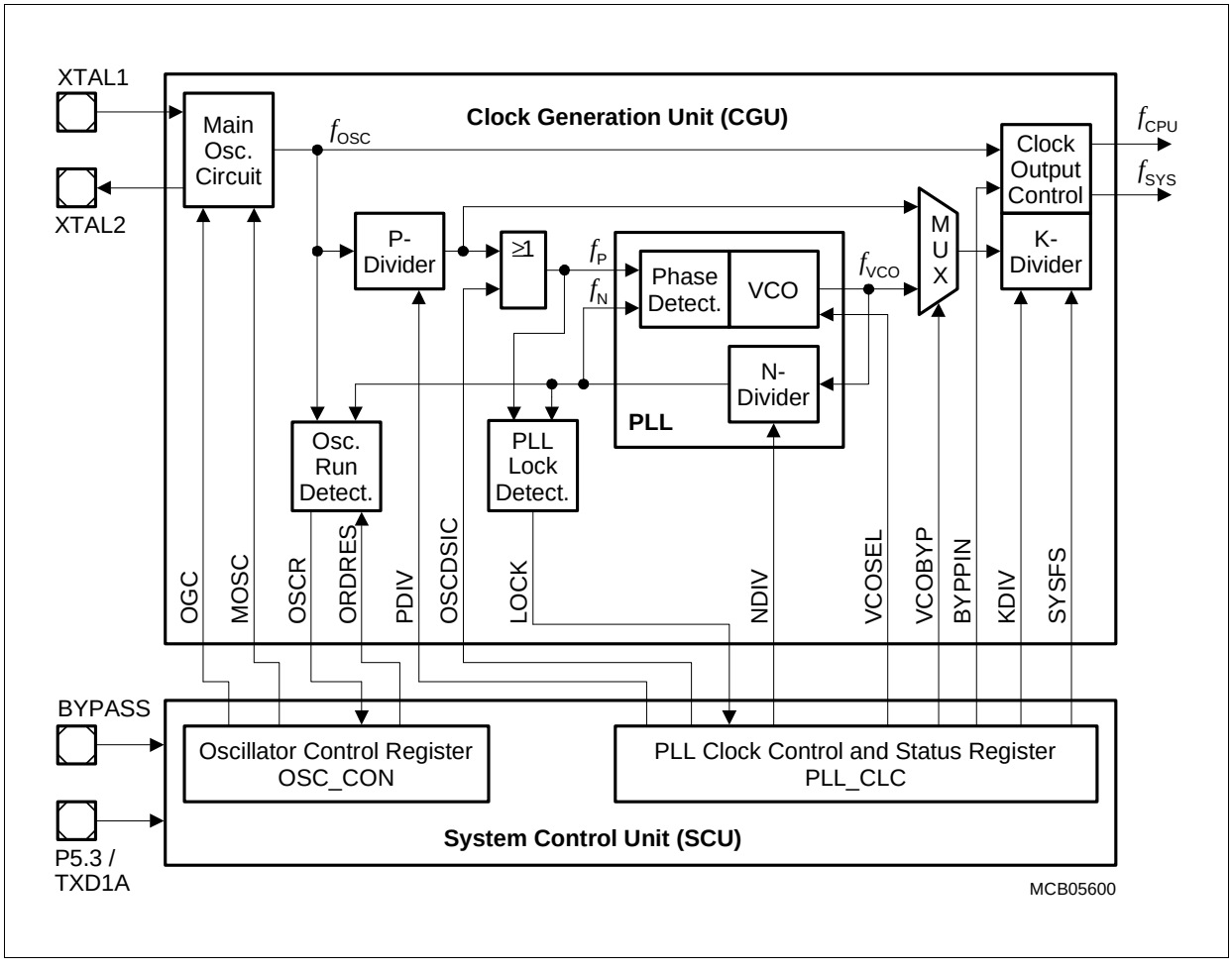

Figure 19 Clock Generation Unit

Recommended Oscillator Circuits

The oscillator circuit, a Pierce oscillator, is designed to work with both, an external crystal oscillator or an external stable clock source. It basically consists of an inverting amplifier and a feedback element with XTAL1 as input, and XTAL2 as output.

When using a crystal, a proper external oscillator circuitry must be connected to both pins, XTAL1 and XTAL2. The crystal frequency can be within the range of 4 MHz to 25 MHz. Additionally are necessary, two load capacitances C_{X1} and C_{X2}, and depending on the crystal type a series resistor R_{X2} to limit the current. A test resistor R_Q may be temporarily inserted to measure the oscillation allowance (negative resistance) of the oscillator circuitry. R_Q values are typically specified by the crystal vendor. The C_{X1} and C_{X2} values shown in **Figure 20** can be used as starting points for the negative resistance evaluation and for non-productive systems. The exact values and related operating range are dependent on the crystal frequency and have to be determined and

Table 9 TC1796 Identification Registers (cont'd)

Short Name	Address	Value	Stepping
ADC0_ID	F010 0408$_H$	0030 C002$_H$	–
MLI0_ID	F010 C008$_H$	0025 C005$_H$	–
MLI1_ID	F010 C108$_H$	0025 C005$_H$	–
MCHK_ID	F010 C208$_H$	001B C001$_H$	–
CPS_ID	F7E0 FF08$_H$	0015 C006$_H$	–
CPU_ID	F7E1 FE18$_H$	000A C005$_H$	–
EBU_ID	F800 0008$_H$	0014 C005$_H$	–
PMU_ID	F800 0508$_H$	002E C002$_H$	–
FLASH_ID	F800 2008$_H$	0031 C002$_H$	–
DMU_ID	F801 0108$_H$	002D C002$_H$	–
DBCU_ID	F87F FA08$_H$	000F C005$_H$	–
DMI_ID	F87F FC08$_H$	0008 C004$_H$	–
PMI_ID	F87F FD08$_H$	000B C004$_H$	–
LFI_ID	F87F FF08$_H$	000C C005$_H$	–
PBCU_ID	F87F FE08$_H$	000F C005$_H$	–

4 Electrical Parameters

4.1 General Parameters

4.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC1796 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC1796 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements which must provided by the microcontroller system in which the TC1796 designed in.

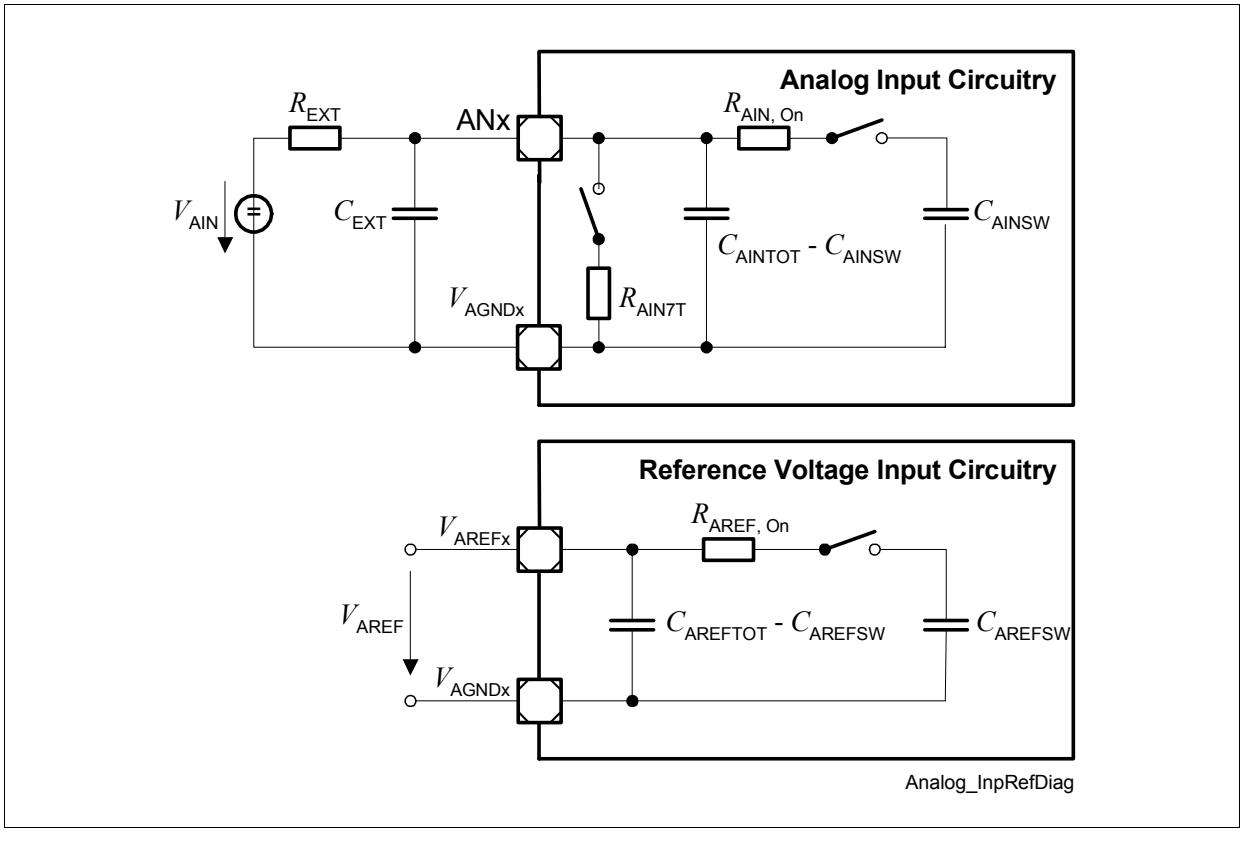

Figure 23 ADC0/ADC1 Input Circuits

4.2.6 Power Supply Current

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Table 21 Power Supply Currents (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
$\overline{\text{PORST}}$ low current at V_{DD}	I_{DD_PORST}	CC	–	–	300	mA	The PLL running at the base frequency
$\overline{\text{PORST}}$ low current at V_{DDP}, and $\overline{\text{PORST}}$ high current without any port activity	I_{DDP_PORST}	CC	–	–	25	mA	The PLL running at the base frequency
Active mode core supply current[1)2)]	I_{DD}	CC	10	–	700	mA	f_{CPU}=150MHzf_{CPU}/f_{SYS} = 2:1
Active mode analog supply current	I_{DDAx}; I_{DDMx}	CC	–	–	–	mA	See ADC0/1 FADC
Stand-by RAM supply current in stand-by	I_{SBSB}	CC	–	–	9	mA	V_{DDSB} = 1V, T_j = 150°C
Oscillator and PLL core power supply	I_{DDOSC}[3)]	CC	–	–	5	mA	–
Oscillator and PLL pads power supply	I_{DDOSC3}	CC	–	–	3.6	mA	–
LVDS port supply (via V_{DDP})[4)]	I_{LVDS}	CC	–	–	50	mA	LVDS pads active
Flash power supply current	I_{DDFL3}	CC	–	–	80	mA	–
Maximum Allowed Power Dissipation[5)]	P_D	SR	–	–	$P_D \times R_{TJA}$ < 25°C	–	worst case T_A = 125°C

1) Infineon Power Loop: CPU and PCP running, all peripherals active. The power consumption of each custom application will most probably be lower than this value, but must be evaluated separately.

2) The I_{DD} decreases for typically 120 mA if the f_{CPU} is decreased for 50 MHz, at constant T_J = 150C, for the Infineon Max Power Loop.
The dependency in this range is, at constant junction temperature, linear.

3) V_{DDOSC} and V_{SSOSC} are not bonded externally in the BC and BD steps of TC1796. An option for bonding them in future steps and products is kept open.

4) In case the LVDS pads are disabled, the power consumption pro pair is negligible (less than 1µA).

5) For the calculation of junction to ambient thermal resistance R_{TJA}, see **Page 130**.

4.3.4 Power, Pad and Reset Timing

Table 23 Power, Pad and Reset Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Min. V_{DDP} voltage to ensure defined pad states[1]	V_{DDPPA}	CC	0.6	–	–	V	–
Oscillator start-up time[2]	t_{OSCS}	CC	–	–	10	ms	–
Minimum $\overline{\text{PORST}}$ active time after power supplies are stable at operating levels	t_{POA}	SR	10	–	–	ms	–
$\overline{\text{HDRST}}$ pulse width	t_{HD}	CC	1024 clock cycles[3][6]	–	–	f_{SYS}	–
$\overline{\text{PORST}}$ rise time	t_{POR}	SR	–	–	50	ms	–
Setup time to $\overline{\text{PORST}}$ rising edge[4]	t_{POS}	SR	0	–	–	ns	–
Hold time from $\overline{\text{PORST}}$ rising edge[4]	t_{POH}	SR	100	–	–	ns	–
Setup time to $\overline{\text{HDRST}}$ rising edge[5]	t_{HDS}	SR	0	–	–	ns	–
Hold time from $\overline{\text{HDRST}}$ rising edge[5]	t_{HDH}	SR	100 + (2 × 1/ f_{SYS})[6]	–	–	ns	–
Ports inactive after $\overline{\text{PORST}}$ reset active[7][8]	t_{PIP}	CC	–	–	150	ns	–
Ports inactive after $\overline{\text{HDRST}}$ reset active	t_{PI}	CC	–	–	150 + 5 × 1/ f_{SYS}	ns	–
Minimum V_{DDP} $\overline{\text{PORST}}$ activation threshold[9]	$V_{PORST3.3}$	SR	–	–	2.9	V	–
Minimum V_{DD} $\overline{\text{PORST}}$ activation threshold[9]	$V_{PORST1.5}$	SR	–	–	1.32	V	–
Power on Reset Boot Time[9]	t_{BP}	CC	–	–	2	ms	–
Hardware/Software Reset Boot Time at f_{CPU}=150MHz[10]	t_B	CC	150	–	350	µs	–

4.3.8 JTAG Interface Timing

Operating Conditions apply, CL = 50 pF

Table 27 TCK Clock Timing Parameter

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TCK clock period[1)]	t_{TCK}	SR	25	–	–	ns	–
TCK high time	t_1	SR	10	–	–	ns	–
TCK low time	t_2	SR	10	–	–	ns	–
TCK clock rise time	t_3	SR	–	–	4	ns	–
TCK clock fall time	t_4	SR	–	–	4	ns	–

1) f_{TCK} should be lower or equal to f_{SYS}.

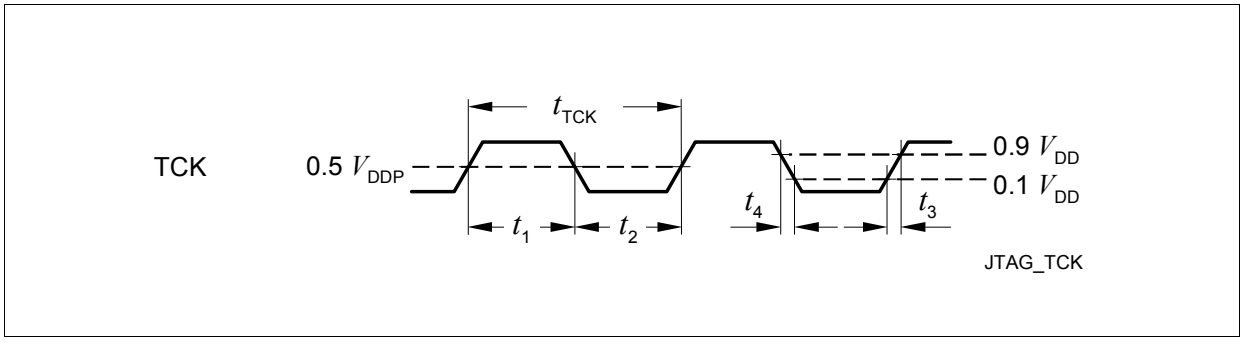


Figure 36 TCK Clock Timing

4.3.12.3 Synchronous Serial Channel (SSC) Master Mode Timing

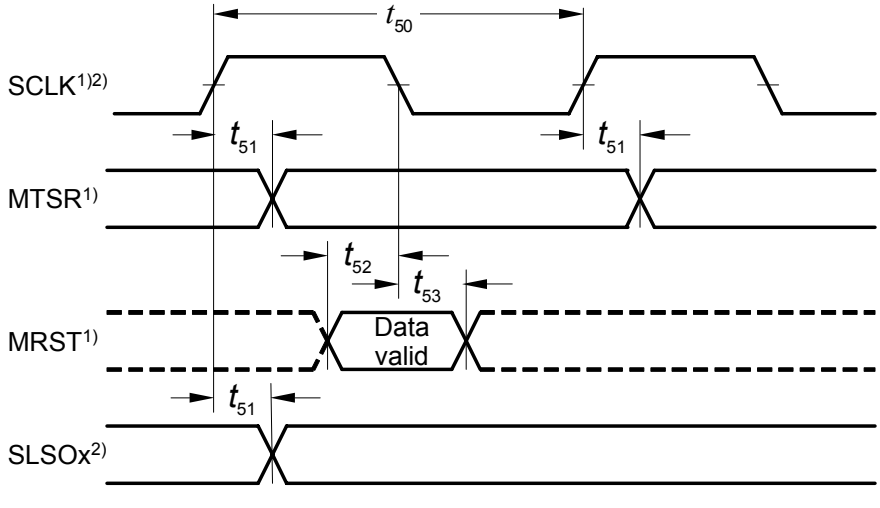
Table 34 SSC Master Mode Timing (Operating Conditions apply), C_L = 50 pF

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SCLK clock period[1)2)]	t_{50}	CC	$2 \times T_{SSC}$[3)]	–	–	ns	–
MTSR/SLSOx delay from SCLK rising edge	t_{51}	CC	0	–	8	ns	–
MRST setup to SCLK falling edge	t_{52}	SR	10	–	–	ns	–
MRST hold from SCLK falling edge	t_{53}	SR	5	–	–	ns	–

1) SCLK signal rise/fall times are the same as the A2 Pads rise/fall times.

2) SCLK signal high and low times can be minimum $1 \times T_{SSC}$.

3) $T_{SSCmin} = T_{SYS} = 1/f_{SYS}$. When f_{SYS} = 75 MHz, t_{50} = 26,67ns



1) This timing is based on the following setup: CON.PH = CON.PO = 0.

2) The transition at SLSOx is based on the following setup: SSOTC.TRAIL = 0 and the first SCLK high pulse is in the first one of a transmission.

SSC_Tmg_1.vsd

Figure 44 SSC Master Mode Timing

5.3 Flash Memory Parameters

The data retention time of the TC1796's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Table 36 Flash Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Program / Data Flash Retention Time, Physical Sector[1)2)]	t_{RET}	CC	20	–	–	years	Max. 1000 erase/program cycles
Program / Data Flash Retention Time Logical Sector[1)2)]	t_{RETL}	CC	20	–	–	years	Max. 100 erase/program cycles
Data Flash Endurance (128 KB)	N_E	CC	15 000	–	–	–	Max. data retention time 5 years
Data Flash Endurance, EEPROM Emulation (8 × 16 KB)	N_{E8}	CC	120 000	–	–	–	Max. data retention time 5 years
Programming Time per Page[3)]	t_{PR}	CC	–	–	5	ms	–
Program Flash Erase Time per 256-KB Sector	t_{ERP}	CC	–	–	5	s	f_{CPU} = 150 MHz
Data Flash Erase Time per 64-KB Sector	t_{ERD}	CC	–	–	2.5	s	f_{CPU} = 150 MHz
Wake-up time	t_{WU}	CC	4300 × $1/f_{CPU}$ + 40µs	–	–	–	–

1) Storage and inactive time included.

2) At average weighted junction temperature T_j = 100°C, or
the retention time at average weighted temperature of T_j = 110°C is minimum 10 years, or
the retention time at average weighted temperature of T_j = 150°C is minimum 0.7 years.

3) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes additional 5 ms.