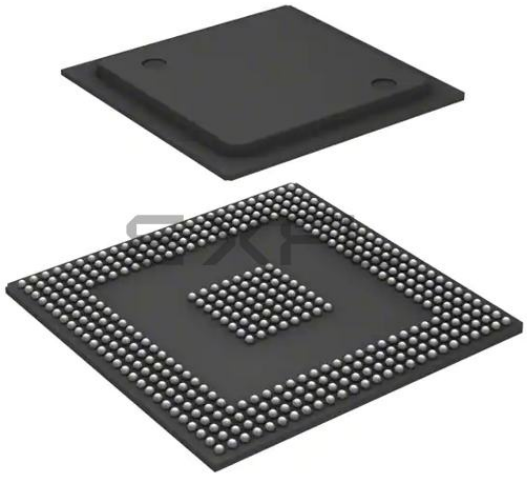
Infineon Technologies - TC1796256F150EBEKDUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	ASC, CANbus, EBI/EMI, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	123
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 44x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BGA
Supplier Device Package	PG-BGA-416
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1796256f150ebekduma1

Table of Contents

  - One MultiCAN Module with four CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - Two 16-channel Analog-to-Digital Converter units (ADC) with selectable 8-bit, 10-bit, or 12-bit resolution
  - One 4-channel Fast Analog-to-Digital Converter unit (FADC) with concatenated comb filters for hardware data reduction: supporting 10-bit resolution, min. conversion time of 280ns
- 44 analog input lines for ADC and FADC
- 123 digital general purpose I/O lines, 4 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 and 2 (CPU, PCP3, DMA)
- Dedicated Emulation Device chip for multi-core debugging, tracing, and calibration via USB V1.1 interface available (TC1796ED)
- Power Management System
- Clock Generation Unit with PLL
- Core supply voltage of 1.5 V
- I/O voltage of 3.3 V
- Full automotive temperature range: -40° to +125°C
- P/PG-BGA-416-4 package

Table 2 Pin Definitions and Functions

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
External Bus Interface Lines (EBU)					
D[31:0]		I/O	B1	V_{DDEBU}	**EBU Data Bus Lines** The EBU Data Bus Lines D[31:0] serve as external data bus.
D0	T26	I/O			Data bus line 0
D1	T24	I/O			Data bus line 1
D2	U26	I/O			Data bus line 2
D3	T25	I/O			Data bus line 3
D4	V26	I/O			Data bus line 4
D5	U25	I/O			Data bus line 5
D6	U23	I/O			Data bus line 6
D7	W26	I/O			Data bus line 7
D8	V25	I/O			Data bus line 8
D9	U24	I/O			Data bus line 9
D10	Y26	I/O			Data bus line 10
D11	AA26	I/O			Data bus line 11
D12	W25	I/O			Data bus line 12
D13	V24	I/O			Data bus line 13
D14	Y25	I/O			Data bus line 14
D15	AB26	I/O			Data bus line 15
D16	W24	I/O			Data bus line 16
D17	AA25	I/O			Data bus line 17
D18	Y24	I/O			Data bus line 18
D19	AA23	I/O			Data bus line 19
D20	AB25	I/O			Data bus line 20
D21	AB24	I/O			Data bus line 21
D22	AA24	I/O			Data bus line 22
D23	AC26	I/O			Data bus line 23
D24	AD26	I/O			Data bus line 24
D25	AC25	I/O			Data bus line 25
D26	AE26	I/O			Data bus line 26
D27	AD25	I/O			Data bus line 27
D28	AC24	I/O			Data bus line 28
D29	AE25	I/O			Data bus line 29
D30	AE24	I/O			Data bus line 30
D31	AD24	I/O			Data bus line 31

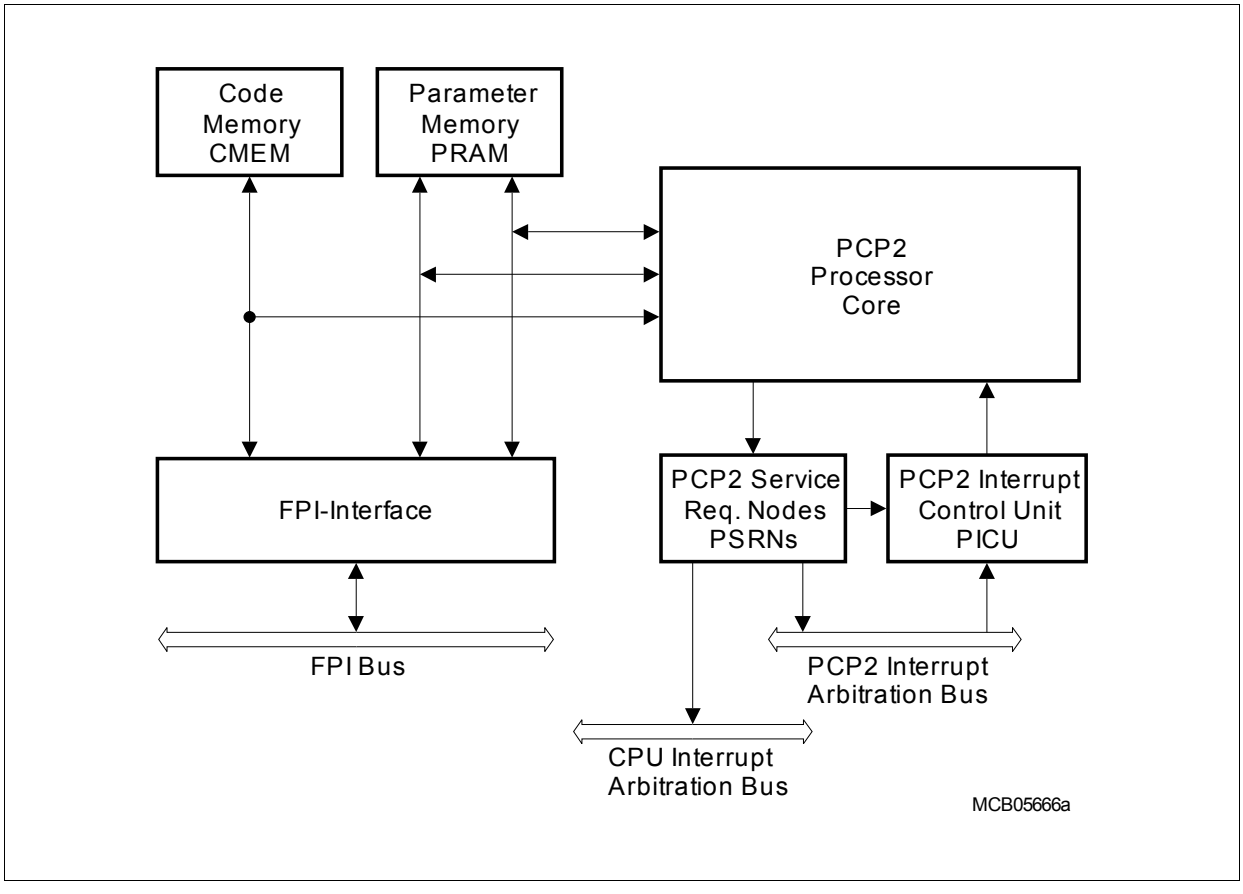

Figure 5 PCP2 Block Diagram

Table 6 PCP2 Instruction Set Overview

Instruction Group	Description
DMA primitives	Efficient DMA channel implementation
Load/Store	Transfer data between PRAM or FPI memory and the general purpose registers, as well as move or exchange values between registers
Arithmetic	Add, subtract, compare and complement
Divide/Multiply	Divide and multiply
Logical	And, Or, Exclusive Or, Negate
Shift	Shift right or left, rotate right or left, prioritize
Bit Manipulation	Set, clear, insert and test bits
Flow Control	Jump conditionally, jump long, exit
Miscellaneous	No operation, Debug

Mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be selected. Parity, framing, and overrun error detection are provided to increase the reliability of data transfers. Transmission and reception of data are double-buffered. For multiprocessor communication, a mechanism is included to distinguish address bytes from data bytes. Testing is supported by a loop-back option. A 13-bit baud rate generator provides the ASC with a separate serial clock signal which can be very accurately adjusted by a prescaler implemented as a fractional divider.

Each ASC module, ASC0 and ASC1, communicates with the external world via two I/O lines. The RXD line is the receive data input signal (in Synchronous Mode also output). TXD is the transmit output signal. In the TC1796, the two I/O lines of each ASC can be alternatively switched to different pairs of GPIO lines.

Clock control, address decoding, and interrupt service request control are managed outside the ASC module kernel.

Features

- Full-duplex asynchronous operating modes
  - 8-bit or 9-bit data frames, LSB first
  - Parity bit generation/checking
  - One or two stop bits
  - Baud rate from 4.69 Mbit/s to 1.12 Bit/s (@ 75 MHz clock)
  - Multiprocessor mode for automatic address/data byte detection
  - Loop-back capability
- Half-duplex 8-bit synchronous operating mode
  - Baud rate from 9.38 Mbit/s to 763 Bit/s (@ 75 MHz clock)
- Double buffered transmitter/receiver
- Interrupt generation
  - On a transmit buffer empty condition
  - On a transmit last bit of a frame condition
  - On a receive buffer full condition
  - On an error condition (frame, parity, overrun error)

or can be received from an external master (Slave Mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data is double-buffered. A shift clock generator provides the SSC with a separate serial clock signal. One slave select input is available for Slave Mode operation. Eight programmable slave select outputs (chip selects) are supported in Master Mode. The I/O lines of the SSC0 module are connected to dedicated device pins while the SSC1 module I/O lines are wired with general purpose I/O port lines.

Features

- Master and Slave Mode operation
  - Full-duplex or half-duplex operation
  - Automatic pad control possible
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: Idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Baud rate generation from 37.5 Mbit/s to 572.2 Bit/s (@ 75 MHz module clock)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)
- Flexible SSC pin configuration
- One slave select input $\overline{\text{SLSI}}$ in slave mode
- Eight programmable slave select outputs SLSO in Master Mode
  - Automatic SLSO generation with programmable timing
  - Programmable active level and enable control
- SSC0 with 8-stage receive FIFO (RXFIFO) and 8-stage transmit FIFO (TXFIFO)
  - Independent control of RXFIFO and TXFIFO
  - 2- to 16-bit FIFO data width
  - Programmable receive/transmit interrupt trigger level
  - Receive and Transmit FIFO filling level indication
  - Overrun error generation
  - Underflow error generation

3.12 MultiCAN Controller (CAN)

Figure 11 shows a global view of the MultiCAN module with its functional blocks and interfaces.

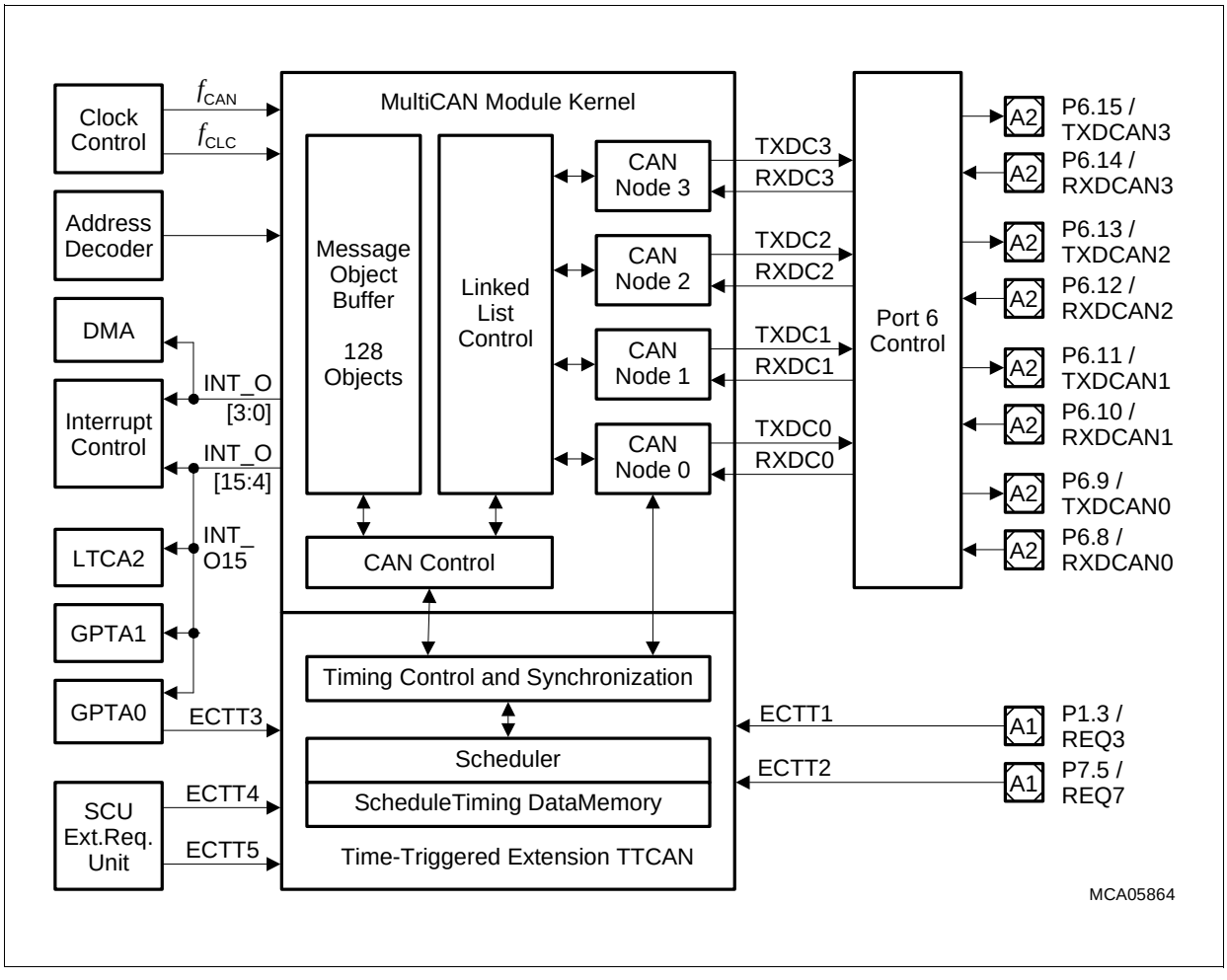

Figure 11 Block Diagram of MultiCAN Module with Time-Triggered Extension

The MultiCAN module contains four independently operating CAN nodes with Full-CAN functionality that are able to exchange Data and Remote Frames via a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All four CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to setup a FIFO buffer.

The message objects are organized in double-chained linked lists, where each CAN node has it's own list of message objects. A CAN node stores frames only into message

Time-Triggered Extension (TTCAN)

In addition to the event-driven CAN functionality, a deterministic behavior can be achieved for CAN node 0 by an extension module that supports time-triggered CAN (TTCAN) functionality. The TTCAN protocol is compliant with the confirmed standardization proposal for ISO 11898-4 and fully conforms to the existing CAN protocol.

The time-triggered functionality is added as higher-layer extension (session layer) to the CAN protocol in order to be able to operate in safety critical applications. The new features allow a deterministic behavior of a CAN network and the synchronization of networks. A global time information is available. The time-triggered extension is based on a scheduler mechanism with a timing control unit and a dedicated timing data part.

TTCAN Features

- Full support of basic cycle and system matrix functionality
- Support of reference messages level 1 and level 2
- Usable as time master
- Arbitration windows supported in time-triggered mode
- Global time information available
- CAN node 0 can be configured either for event-driven or for time-triggered mode
- Built-in scheduler mechanism and a timing synchronization unit
- Write protection for scheduler timing data memory
- Module-external CAN time trigger inputs (ECTTx lines) can be used as transmit trigger for a reference message
- Timing-related interrupt functionality
- Parity protection for scheduler memory

3.13 Micro Link Serial Bus Interface (MLI0, MLI1)

The Micro Link Interface (MLI) is a fast synchronous serial interface that allows to exchange data between microcontrollers of the 32-bit AUDO microcontroller family without intervention of a CPU or other bus masters. **Figure 12** shows how two microcontrollers are typically connected together via their MLI interfaces. The MLI operates in both microcontrollers as a bus master on the system bus.

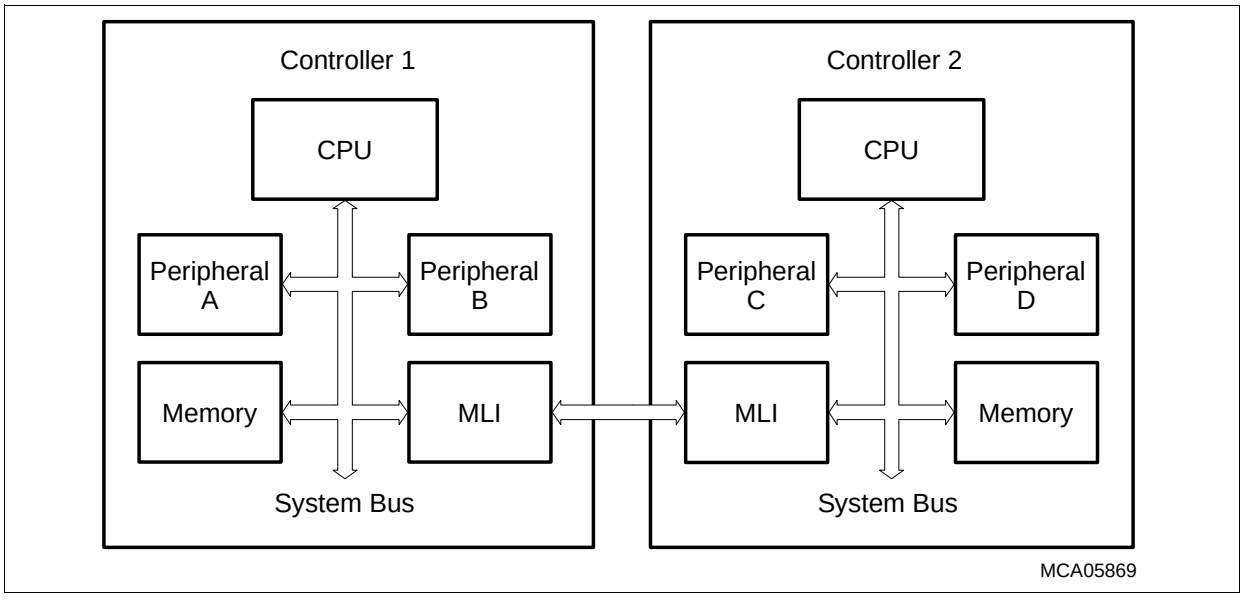

Figure 12 Typical Micro Link Interface Connection

Features

- Synchronous serial communication between MLI transmitters and MLI receivers located on the same or on different microcontroller devices
- Automatic data transfer/request transactions between local/remote controller
- Fully transparent read/write access supported (= remote programming)
- Complete address range of remote controller available
- Specific frame protocol to transfer commands, addresses and data
- Error control by parity bit
- 32-bit, 16-bit, and 8-bit data transfers
- Programmable baud rate:
  - MLI transmitter baud rate: max. $f_{MLI}/2$ (= 37.5 Mbit/s @ 75 MHz module clock)
  - MLI receiver baud rate: max. f_{MLI}
- Multiple remote (slave) controllers supported

MLI transmitter and MLI receiver communicate with other off-chip MLI receivers and MLI transmitters via a 4-line serial I/O bus each. Several I/O lines of these I/O buses are available outside the MLI module kernel as four-line output or input buses.

Figure 13 shows the functional blocks of the two MLI modules with its interfaces.

3.15 Analog-to-Digital Converter (ADC0, ADC1)

The two ADC modules of the TC1796 are analog to digital converters with 8-bit, 10-bit, or 12-bit resolution including sample & hold functionality.

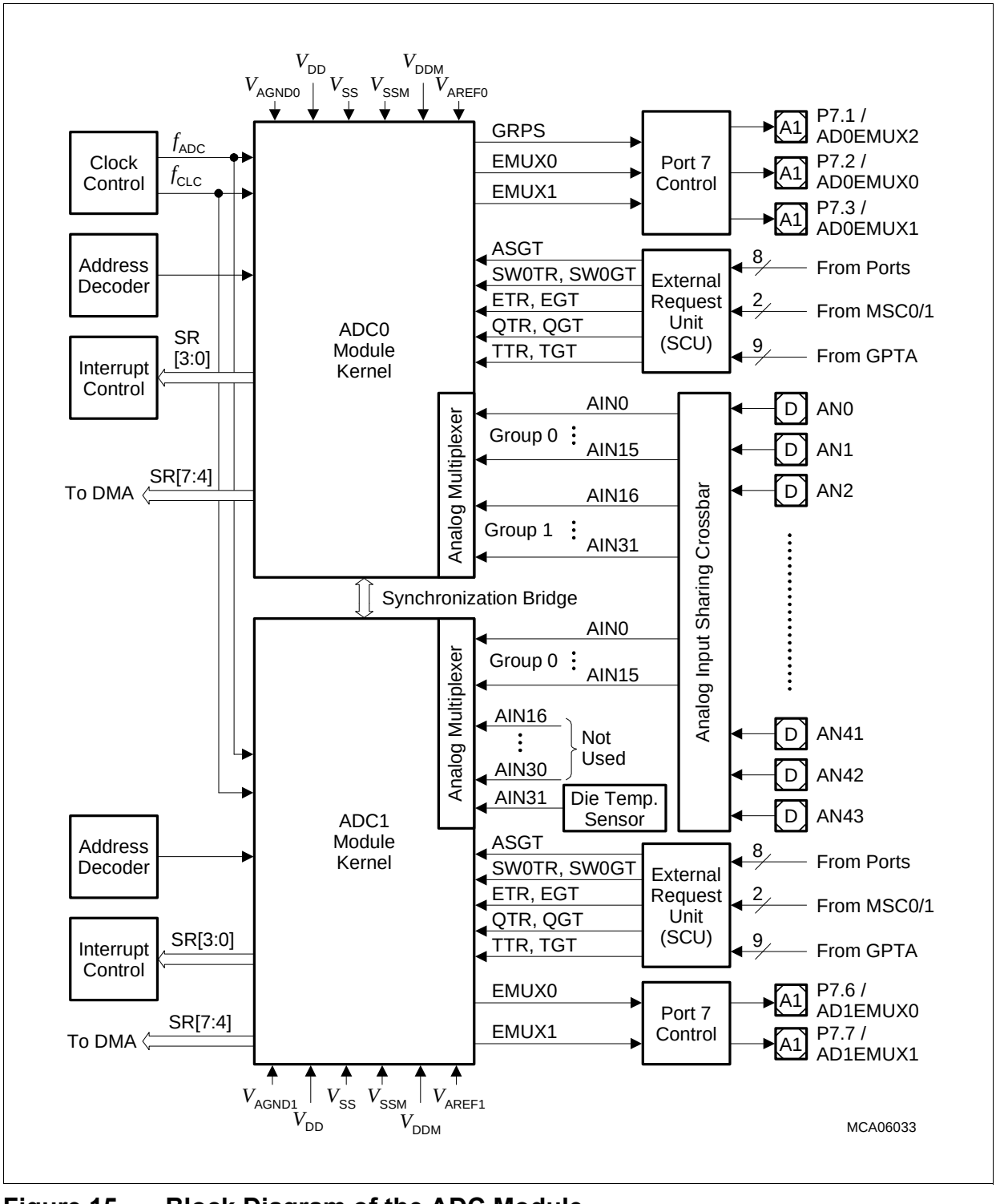

Figure 15 Block Diagram of the ADC Module

3.18 Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failure. The WDT helps to abort an accidental malfunction of the TC1796 in a user-specified time period. When enabled, the WDT will cause the TC1796 system to be reset if the WDT is not serviced within a user-programmable time period. The CPU must service the WDT within this time interval to prevent the WDT from causing a TC1796 system reset. Hence, routine service of the WDT confirms that the system is functioning properly.

In addition to this standard “Watchdog” function, the WDT incorporates the EndInit feature and monitors its modifications. A system-wide line is connected to the End-of-Initialization (Endinit) feature and monitors its modifications. A system-wide line is connected to the WDT_CON0.ENDINIT bit, serving as an additional write-protection for critical registers (besides Supervisor Mode protection)

A further enhancement in the TC1796’s WDT is its reset pre-warning operation. Instead of immediately resetting the device on the detection of an error (the way that standard Watchdogs do), the WDT first issues an Non-Maskable Interrupt (NMI) to the CPU before finally resetting the device at a specified time period later. This gives the CPU a chance to save system state to memory for later examination of the cause of the malfunction, an important aid in debugging.

Features

- 16-bit Watchdog counter
- Selectable input frequency: f_{SYS}/256 or f_{SYS}/16384
- 16-bit user-definable reload value for normal Watchdog operation, fixed reload value for Time-Out and Pre-warning Modes
- Incorporation of the ENDINIT bit and monitoring of its modifications
- Sophisticated password access mechanism with fixed and user-definable password fields
- Proper access always requires two write accesses. The time between the two accesses is monitored by the WDT and limited.
- Access Error Detection: Invalid password (during first access) or invalid guard bits (during second access) trigger the Watchdog reset generation.
- Overflow Error Detection: An overflow of the counter triggers the Watchdog reset generation.
- Watchdog function can be disabled; access protection and ENDINIT monitor function remain enabled.
- Double Reset Detection: If a Watchdog induced reset occurs twice, a severe system malfunction is assumed and the TC1796 is held in reset until a power-on reset. This prevents the device from being periodically reset if, for instance, connection to the external memory has been lost such that even system initialization could not be performed

3.21 Power Management System

The TC1796 power management system allows software to configure the various processing units so that they automatically adjust to draw the minimum necessary power for the application. There are three power management modes:

- Run Mode
- Idle Mode
- Sleep Mode

The operation of each system component in each of these states can be configured by software. The power-management modes provide flexible reduction of power consumption through a combination of techniques, including stopping the CPU clock, stopping the clocks of other system components individually, and individually clock-speed reduction of some peripheral components.

Besides these explicit software-controlled power-saving modes, in the TC1796 special attention has been paid for automatic power-saving in those operating units which are currently not required or idle. In that case they are shut off automatically until their operation is required again.

Table 8 describes the features of the power management modes.

Table 8 Power Management Mode Summary

Mode	Description
Run	The system is fully operational. All clocks and peripherals are enabled, as determined by software.
Idle	The CPU clock is disabled, waiting for a condition to return it to Run Mode. Idle Mode can be entered by software when the processor has no active tasks to perform. All peripherals remain powered and clocked. Processor memory is accessible to peripherals. A reset, Watchdog Timer event, a falling edge on the NMI pin, or any enabled interrupt event will return the system to Run Mode.
Sleep	The system clock signal is distributed only to those peripherals programmed to operate in Sleep Mode. The other peripheral module will be shut down by the suspend signal. Interrupts from operating peripherals, the Watchdog Timer, a falling edge on the NMI pin, or a reset event will return the system to Run Mode. Entering this state requires an orderly shut-down controlled by the Power Management State Machine.

In typical operation, Idle Mode and Sleep Mode may be entered and exited frequently during the run time of an application. For example, system software will typically cause the CPU to enter Idle Mode each time it has to wait for an interrupt before continuing its tasks. In Sleep Mode and Idle Mode, wake-up is performed automatically when any enabled interrupt signal is detected, or if the Watchdog Timer signals the CPU with an NMI trap.

Table 9 TC1796 Identification Registers (cont'd)

Short Name	Address	Value	Stepping
ADC0_ID	F010 0408$_H$	0030 C002$_H$	–
MLI0_ID	F010 C008$_H$	0025 C005$_H$	–
MLI1_ID	F010 C108$_H$	0025 C005$_H$	–
MCHK_ID	F010 C208$_H$	001B C001$_H$	–
CPS_ID	F7E0 FF08$_H$	0015 C006$_H$	–
CPU_ID	F7E1 FE18$_H$	000A C005$_H$	–
EBU_ID	F800 0008$_H$	0014 C005$_H$	–
PMU_ID	F800 0508$_H$	002E C002$_H$	–
FLASH_ID	F800 2008$_H$	0031 C002$_H$	–
DMU_ID	F801 0108$_H$	002D C002$_H$	–
DBCU_ID	F87F FA08$_H$	000F C005$_H$	–
DMI_ID	F87F FC08$_H$	0008 C004$_H$	–
PMI_ID	F87F FD08$_H$	000B C004$_H$	–
LFI_ID	F87F FF08$_H$	000C C005$_H$	–
PBCU_ID	F87F FE08$_H$	000F C005$_H$	–

Table 12 Operating Condition Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Absolute sum of short circuit currents of the device	$\Sigma\|I_{SC}\|$	SR	–	–	100	mA	See note[10)]
External load capacitance	C_L	SR	–	–	–	pF	Depending on pin class. See DC characteristics

1) Digital supply voltages applied to the TC1796 must be static regulated voltages which allow a typical voltage swing of ±5%.

2) V_{DDOSC} and V_{SSOSC} are not bonded externally in the BC and BD steps of TC1796. An option for bonding them in future steps and products is kept open.

3) Voltage overshoot up to 1.7 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h.

4) Voltage overshoot to 4 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h

5) The V_{DDSB} must be properly connected and supplied with power. If not, the TC1796 will not operate. In case of a stand-by operation, the core voltage must not float, but must be pulled low, in order to avoid internal cross-currents.

6) This applies only during power down state. During normal SRAM operation regular V_{DD} has to be applied.

7) The TC1796 uses a static design, so the minimum operation frequency is 0 MHz. Due to test time restriction no lower frequency boundary is tested, however.

8) The PLL jitter characteristics add to this value according to the application settings. See the PLL jitter parameters.

9) Applicable for digital outputs.

10) See additional document “TC1796 Pin Reliability in Overload“ for overload current definitions.

Table 13 Pin Groups for Overload/Short-Circuit Current Sum Parameter

Group	Pins
1	P4.[7:0]
2	P4.[14:8]
3	P4.15, SLSO[1:0], SCLK0, MTSR0, MRST0, $\overline{\text{SLSI0}}$
4	$\overline{\text{WAIT}}$, $\overline{\text{HOLD}}$, $\overline{\text{BC}}$[3:0], $\overline{\text{HLDA}}$, MR/$\overline{\text{W}}$, $\overline{\text{BAA}}$, $\overline{\text{CSCOMB}}$
5	$\overline{\text{CS}}$[3:0], $\overline{\text{RD}}$, RD/$\overline{\text{WR}}$, $\overline{\text{BREQ}}$, $\overline{\text{ADV}}$, BFCLKO
6	BFCLKI, D[31:24]
7	D[23:16]
8	D[15:8]

Table 13 Pin Groups for Overload/Short-Circuit Current Sum Parameter

Group	Pins
9	D[7:0]
10	A[23:16]
11	A[15:8]
12	A[7:0]
13	TSTRES, TDI, TMS, TCK, $\overline{\text{TRST}}$, TDO, $\overline{\text{BRKOUT}}$, $\overline{\text{BRKIN}}$, $\overline{\text{TESTMODE}}$
14	P10.[3:0], BYPASS, $\overline{\text{NMI}}$, $\overline{\text{PORST}}$, $\overline{\text{HDRST}}$
15	P9.[8:0]
16	FCLP[1:0]A, FCLN[1:0], SOP[1:0]A, SON[1:0]
17	P5.[7:0]
18	P3.[7:0]
19	P3.[15:8]
20	P0.[7:0]
21	P0.[15:8]
22	P2.[15:7]
23	P2.[6:2], P6.9, P6.8, P6.6, P6.11
24	P6.[15:12], P6.10, P6.7, P6.[5:4]
25	P8.[7:0]
26	P1.[15:13], P1.[11:8], P1.5
27	P1.12, P1.[7:6], P1.[4:0]
28	TR[15:8]
29	TR[7:1], TRCLK
30	TR0, P7.[7:0]

4.2 DC Parameters

4.2.1 Input/Output Pins

Table 14 Input/Output DC-Characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
General Parameters						
Pull-up current[1)]	$\lvert I_{PUH}\rvert$ CC	10	–	100	µA	$V_{IN} < V_{IHAmin}$; class A1/A2/Input pads.
		20	–	200	µA	$V_{IN} < V_{IHAmin}$; class A3/A4 pads.
		5	–	85	µA	$V_{IN} < V_{IHBmin}$; class B1/B2 pads.
Pull-down current[1)]	$\lvert I_{PDL}\rvert$ CC	10	–	150	µA	$V_{IN} > V_{ILAmax}$; class A1/A2/Input pads. $V_{IN} > V_{ILBmax}$; class B1/B2 pads
		20	–	200	µA	$V_{IN} > V_{ILAmax}$; class A3/A4 pads.
Pin capacitance[1)] (Digital I/O)	C_{IO} CC	–	–	10	pF	f = 1 MHz T_A = 25 °C
Input only Pads (V_{DDP} = 3.13 to 3.47 V = 3.3 V ± 5%)						
Input low voltage Class A1/A2 pins	V_{ILA} SR	-0.3	–	0.34 × V_{DDP}	V	–
Input high voltage Class A1/A2 pins	V_{IHA} SR	0.64 × V_{DDP}	–	V_{DDP}+ 0.3 or max. 3.6	V	Whatever is lower
Ratio V_{IL}/V_{IH}	CC	0.53	–	–	–	–
Input hysteresis	HYSA CC	0.1 × V_{DDP}	–	–	V	5)2)
Input leakage current	I_{OZI} CC	–	–	±3000 ±6000	nA	V_{DDP}/2-1 < V_{IN} < V_{DDP}/2+1 Otherwise[3)]

4.3.5 Phase Locked Loop (PLL)

Note: All PLL characteristics defined on this and the next page are verified by design characterization.

Table 24 PLL Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated jitter	D_P	See Figure 32	–	–	–	–
VCO frequency range	f_{VCO}	400	–	500	MHz	–
		600	–	700	MHz	–
		500	–	600	MHz	–
PLL base frequency[1)]	$f_{PLLBASE}$	140	–	320	MHz	–
		150	–	400	MHz	–
		200	–	480	MHz	–
PLL lock-in time	t_L	–	–	200	µs	–

1) The CPU base frequency which is selected after reset is calculated by dividing the limit values by 16 (this is the K factor after reset).

Phase Locked Loop Operation

When PLL operation is enabled and configured, the PLL clock f_{VCO} (and with it the CPU clock f_{CPU}) is constantly adjusted to the selected frequency. The relation between f_{VCO} and f_{SYS} is defined by: $f_{VCO} = K \times f_{CPU}$. The PLL causes a jitter of f_{CPU} and affects the clock outputs BFCLKO, TRCLK, and SYSCLK (P1.12) which are derived from the PLL clock f_{VCO}.

There will be defined two formulas that define the (absolute) approximate maximum value of jitter D_P in ns dependent on the K-factor, the CPU clock frequency f_{CPU} in MHz, and the number P of consecutive f_{CPU} clock periods.

$$P \times K < 385 \qquad Dp[ns] = \frac{7000 \times P}{fcpu^2[MHz] \times K} + 0,535 \tag{1}$$

$$P \times K \geq 385 \qquad Dp[ns] = \frac{2700000}{fcpu^2[MHz] \times K^2} + 0,535 \tag{2}$$

Note: The frequency of system clock f_{SYS} can be selected to be either f_{CPU} or $f_{CPU}/2$.

With rising number P of clock cycles the maximum jitter increases linearly up to a value of P that is defined by the K-factor of the PLL. Beyond this value of P the maximum accumulated jitter remains at a constant value. Further, a lower CPU clock frequency f_{CPU} results in a higher absolute maximum jitter value.

Figure 32 gives the jitter curves for several K/f_{CPU} combinations.

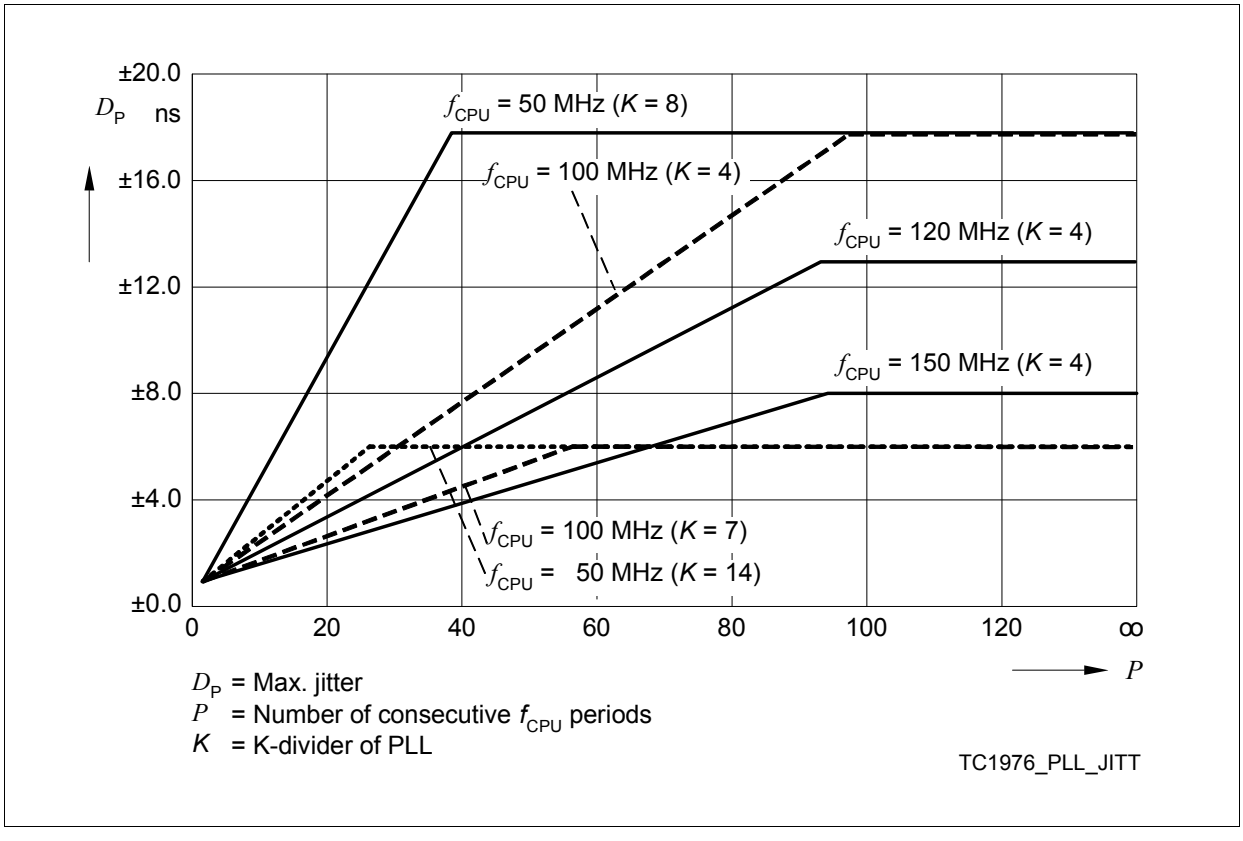

Figure 32 Approximated Maximum Accumulated PLL Jitter for Typical CPU Clock Frequencies f_{CPU} (overview)

4.3.9.1 Demultiplexed Read Timing

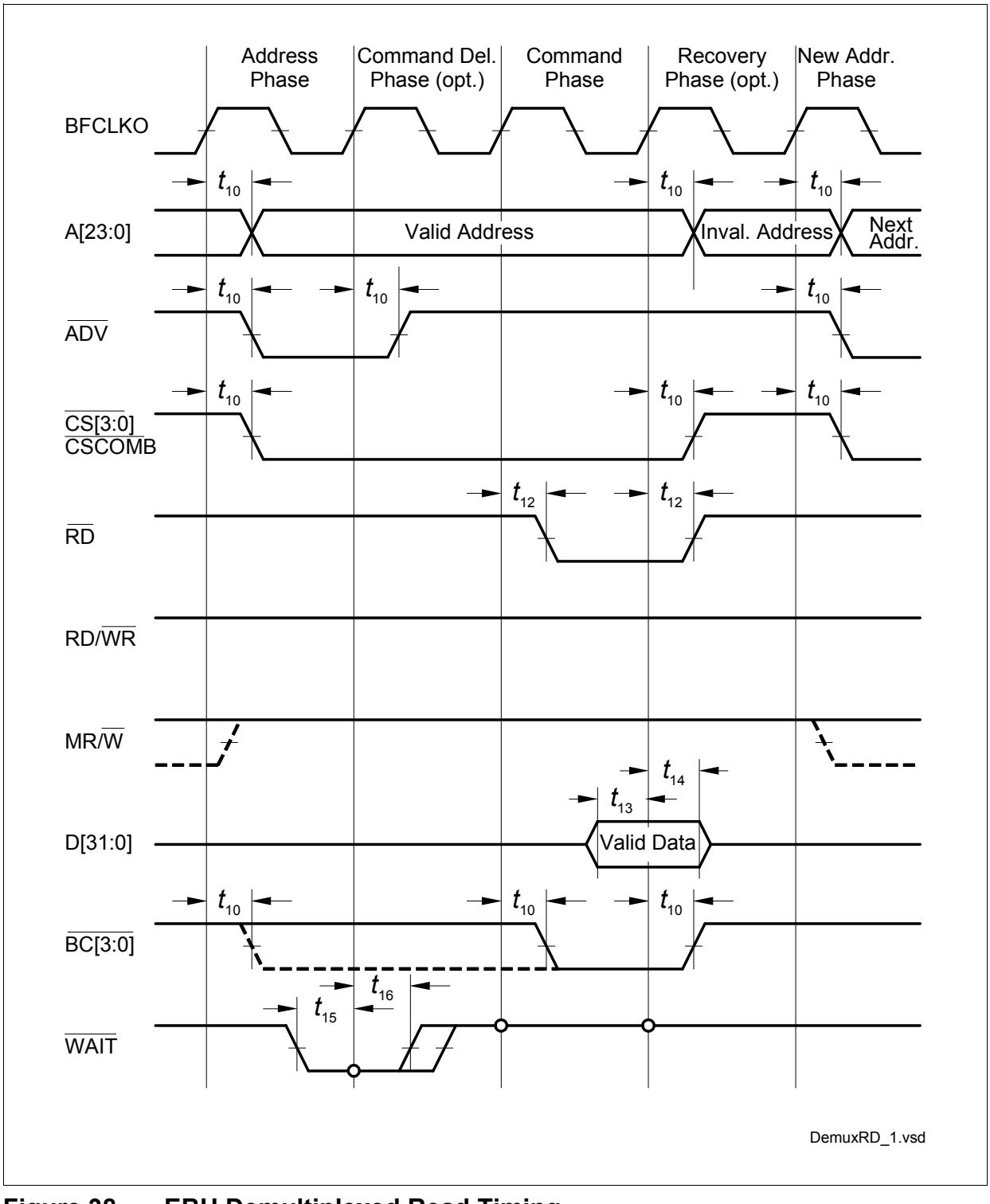

Figure 38 EBU Demultiplexed Read Timing

w w w . i n f i n e o n . c o m

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