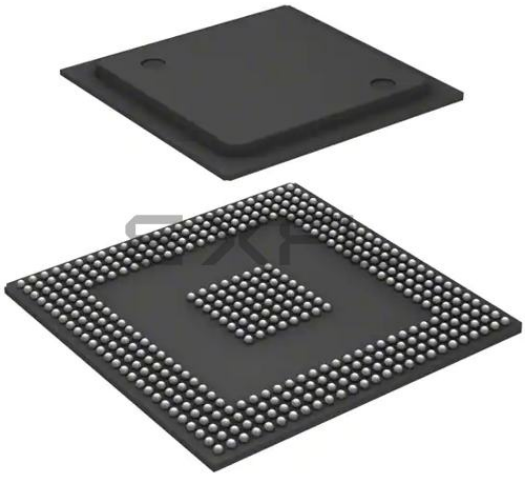
Infeon Technologies - TC1796256F150EBEKDUMA2 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	ASC, CANbus, EBI/EMI, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	123
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 44x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BGA
Supplier Device Package	PG-BGA-416
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1796256f150ebekduma2

2 General Device Information

2.1 TC1796 Block Diagram

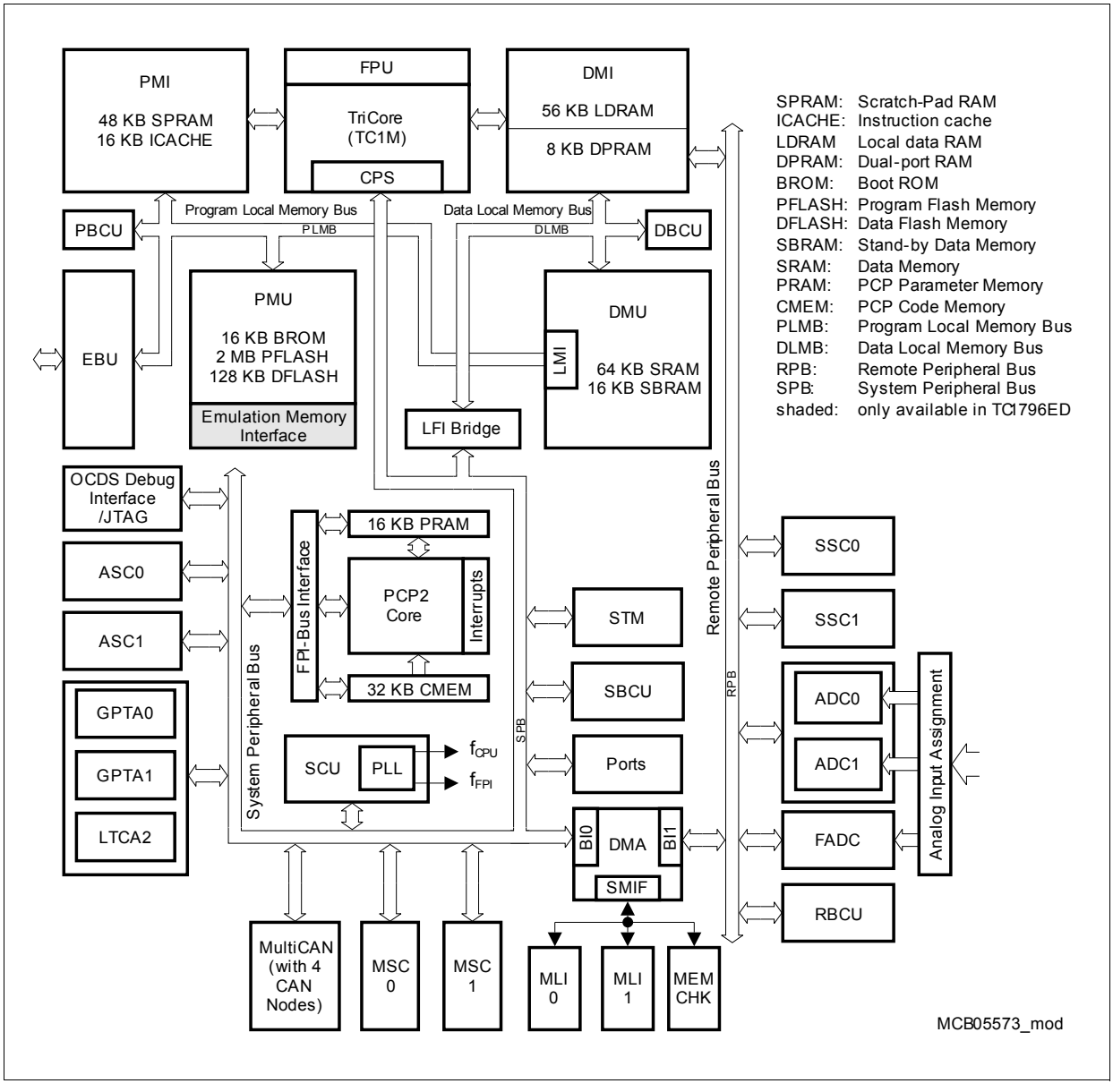


Figure 1 TC1796 Block Diagram

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions	
P7		I/O	A1	V_{DDP}	**Port 7** Port 7 is an 8-bit bi-directional general-purpose I/O port which can be alternatively used as external trigger input lines and for ADC0/1 external multiplexer control.	
P7.0	R3	I			REQ4	External trigger input 4
P7.1	R2	I			REQ5	External trigger input 5
		O			AD0EMUX2	ADC0 external multiplexer control output 2
P7.2	U4	O			AD0EMUX0	ADC0 external multiplexer control output 0
P7.3	U3	O			AD0EMUX2	ADC0 external multiplexer control output 1
P7.4	T3	I			REQ6	External trigger input 6
P7.5	T2	I			REQ7	External trigger input 7
P7.6	T1	O			AD1EMUX0	ADC1 external multiplexer control output 0
P7.7	U2	O			AD1EMUX1	ADC1 external multiplexer control output 1

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
P9		I/O	A2	V_{DDP}	**Port 9** Port 9 is a 9-bit bi-directional general-purpose I/O port which can be alternatively used as GPTA or MSC0/1 I/O lines.
P9.0	A19	I/O O			IN48/OUT48 I/O line of GPTA EN12 MSC1 device select output 2
P9.1	B19	I/O O			IN49/OUT49 I/O line of GPTA EN11 MSC1 device select output 1
P9.2	B20	I/O O			IN50/OUT50 I/O line of GPTA SOP1B MSC1 serial data output
P9.3	A20	I/O O			IN51/OUT51 I/O line of GPTA FCLP1 MSC1 clock output
P9.4	D18	I/O O			IN52/OUT52 I/O line of GPTA EN03 MSC0 device select output 3
P9.5	D19	I/O O			IN53/OUT53 I/O line of GPTA EN02 MSC0 device select output 2
P9.6	C19	I/O O			IN54/OUT54 I/O line of GPTA EN01 MSC0 device select output 1
P9.7	D20	I/O O			IN55/OUT55 I/O line of GPTA SOP0B MSC0 serial data output
P9.8	C20	O			FCLP0B MSC0 clock output

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
V_{DDEBU}	H23 H24 H25 H26 M23 T23 Y23 AC18 AC22	–	–	–	**EBU Power Supply (2.3 - 3.3V)**
V_{DD}	B26 C25 D9 D16 D24 E23 H4 P23 R4 V23 AB23 AC11 AC20	–	–	–	**Core Power Supply (1.5V)**
V_{DDP}	A25 B24 C23 D7 D14 D22 K4 AC16 AD16 AE16 AF16	–	–	–	**Port Power Supply (3.3V)** (also for OCDS)
V_{SS}	See Table 3	–	–	–	**Ground** 15 V_{SS} lines are located at outer balls. 47 V_{SS} lines are located at center balls.

1) In order to minimize noise coupling to the on-chip A/D converters, it is recommended to use these pins as less as possible in strong driver mode.

2) In case of a power-fail condition (one or more power supply voltages drop below the specified voltage range), an undefined output driving level may occur at these pins.

3) Not bonded externally in the BC and BD steps of TC1796. An option for bonding them in future steps and products is kept open.

Table 3 V_{SS} Balls

V_{SS} Outer Balls	V_{SS} Center Balls
A26, B25, C24, D8, D15, D23, J4, L23, R23, T4, W23, AC10, AC17, AC19, AC23	K[17:13], L[17:13], M[17:12], N[17:10], P[17:10], R[17:13], T[17:13], U[17:13]

3.3 Architectural Address Map

Table 5 shows the overall architectural address map as defined for the TriCore and implemented in TC1796.

Table 5 TC1796 Architectural Address Map

Seg-ment	Contents	Size	Description
0-7	Global	8 × 256 Mbyte	Reserved (MMU space), cached
8	Global Memory	256 Mbyte	EBU (246 Mbyte), PMU with PFLASH, DFLASH, BROM, memory reserved for Emulation, cached
9	Global Memory	256 Mbyte	FPI space; cached
10	Global Memory	256 Mbyte	EBU (246 Mbyte), PMU with PFLASH, DFLASH, BROM, memory reserved for Emulation, non-cached
11	Global Memory	256 Mbyte	FPI space; non-cached
12	Local LMB Memory	256 Mbyte	DMU, bottom 4 Mbyte visible from FPI Bus in segment 14, cached
13	DMI	64 Mbyte	Local Data Memory RAM, non-cached
	PMI	64 Mbyte	Local Code Memory RAM, non-cached
	EXTPER	96 Mbyte	External Peripheral Space, non-cached
	EXTEMU	16 Mbyte	External Emulator Range, non-cached
	BOOTROM	16 Mbyte	Boot ROM space, BROM mirror; non-cached
14	EXTPER	128 Mbyte	External Peripheral Space non-speculative, no execution, non-cached
	CPU[0 ..15] image region	16 × 8 Mbyte	Non-speculative, no execution, non-cached
15	LMBPER CSFRs INTPER	256 Mbyte	CSFRs of CPUs[0 ..15]; LMB & Internal Peripheral Space; non-speculative, no execution, non-cached

The downstream and upstream channels of the MSC module communicate with the external world via nine I/O lines. Eight output lines are required for the serial communication of the downstream channel (clock, data, and enable signals). One out of eight input lines SDI[7:0] is used as serial data input signal for the upstream channel. The source of the serial data to be transmitted by the downstream channel can be MSC register contents or data that is provided at the ALTINL/ALTINH input lines. These input lines are typically connected to other on-chip peripheral units (for example with a timer unit like the GPTA). An emergency stop input signal allows to set bits of the serial data stream to dedicated values in emergency case.

Clock control, address decoding, and interrupt service request control are managed outside the MSC module kernel. Service request outputs are able to trigger an interrupt or a DMA request.

Features

- Fast synchronous serial interface to connect power switches in particular, or other peripheral devices via serial buses
- High-speed synchronous serial transmission on downstream channel
  - Maximum serial output clock frequency: $f_{FCL} = f_{MSC}/2$ (= 37.5 Mbit/s @ 75 MHz module clock)
  - Fractional clock divider for precise frequency control of serial clock f_{MSC}
  - Command, data, and passive frame types
  - Start of serial frame: Software-controlled, timer-controlled, or free-running
  - Programmable upstream data frame length (16 or 12 bits)
  - Transmission with or without SEL bit
  - Flexible chip select generation indicates status during serial frame transmission
  - Emergency stop without CPU intervention
- Low-speed asynchronous serial reception on upstream channel
  - Baud rate: f_{MSC} divided by 8, 16, 32, 64, 128, 256, or 512
  - Standard asynchronous serial frames
  - Parity error checker
  - 8-to-1 input multiplexer for SDI lines
  - Built-in spike filter on SDI lines

3.12 MultiCAN Controller (CAN)

Figure 11 shows a global view of the MultiCAN module with its functional blocks and interfaces.

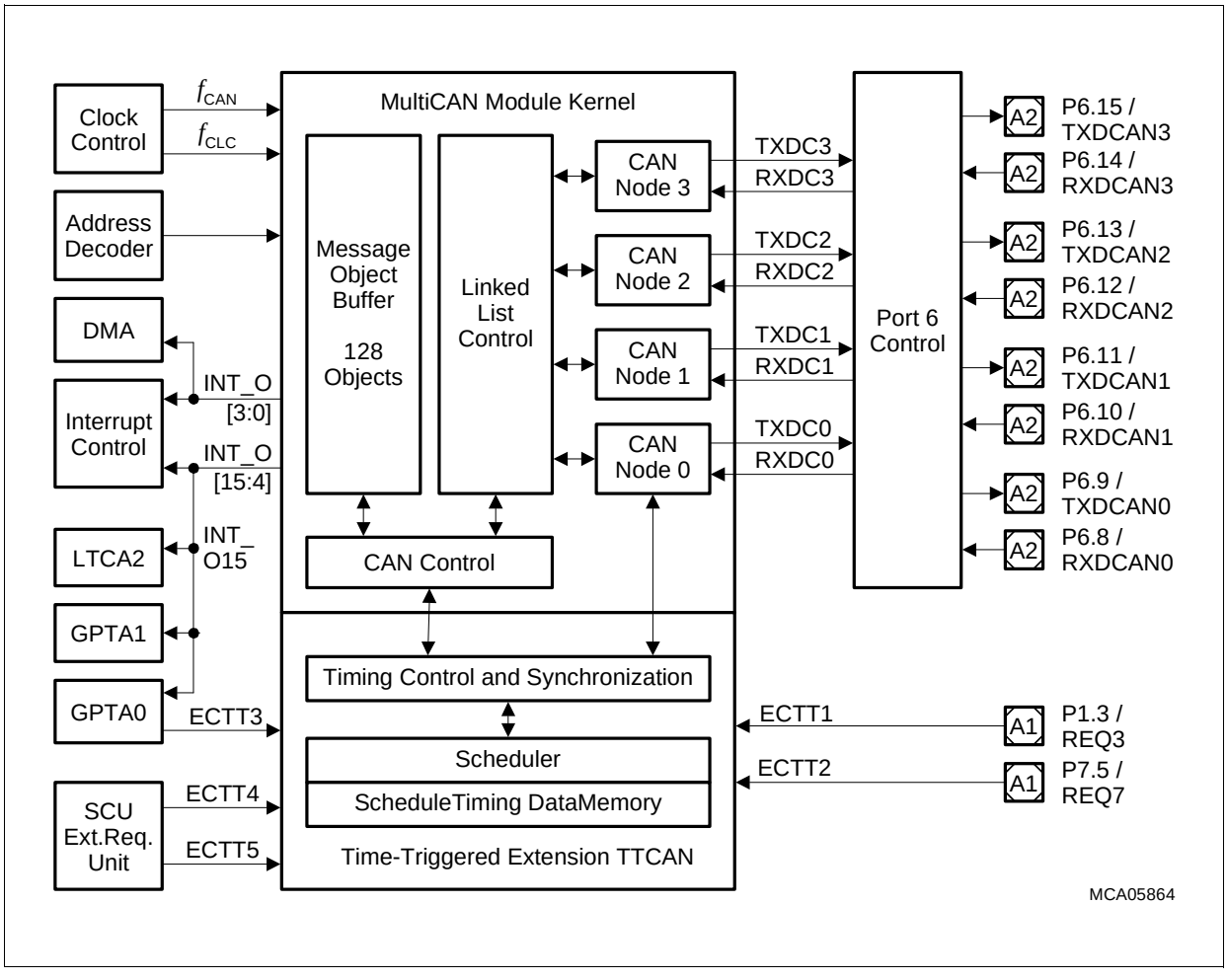


Figure 11 Block Diagram of MultiCAN Module with Time-Triggered Extension

The MultiCAN module contains four independently operating CAN nodes with Full-CAN functionality that are able to exchange Data and Remote Frames via a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All four CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to setup a FIFO buffer.

The message objects are organized in double-chained linked lists, where each CAN node has it's own list of message objects. A CAN node stores frames only into message

are derived from f_{VCO} only by the K-Divider. In this mode, the system clock f_{SYS} can be equal to f_{CPU} or $f_{CPU}/2$.

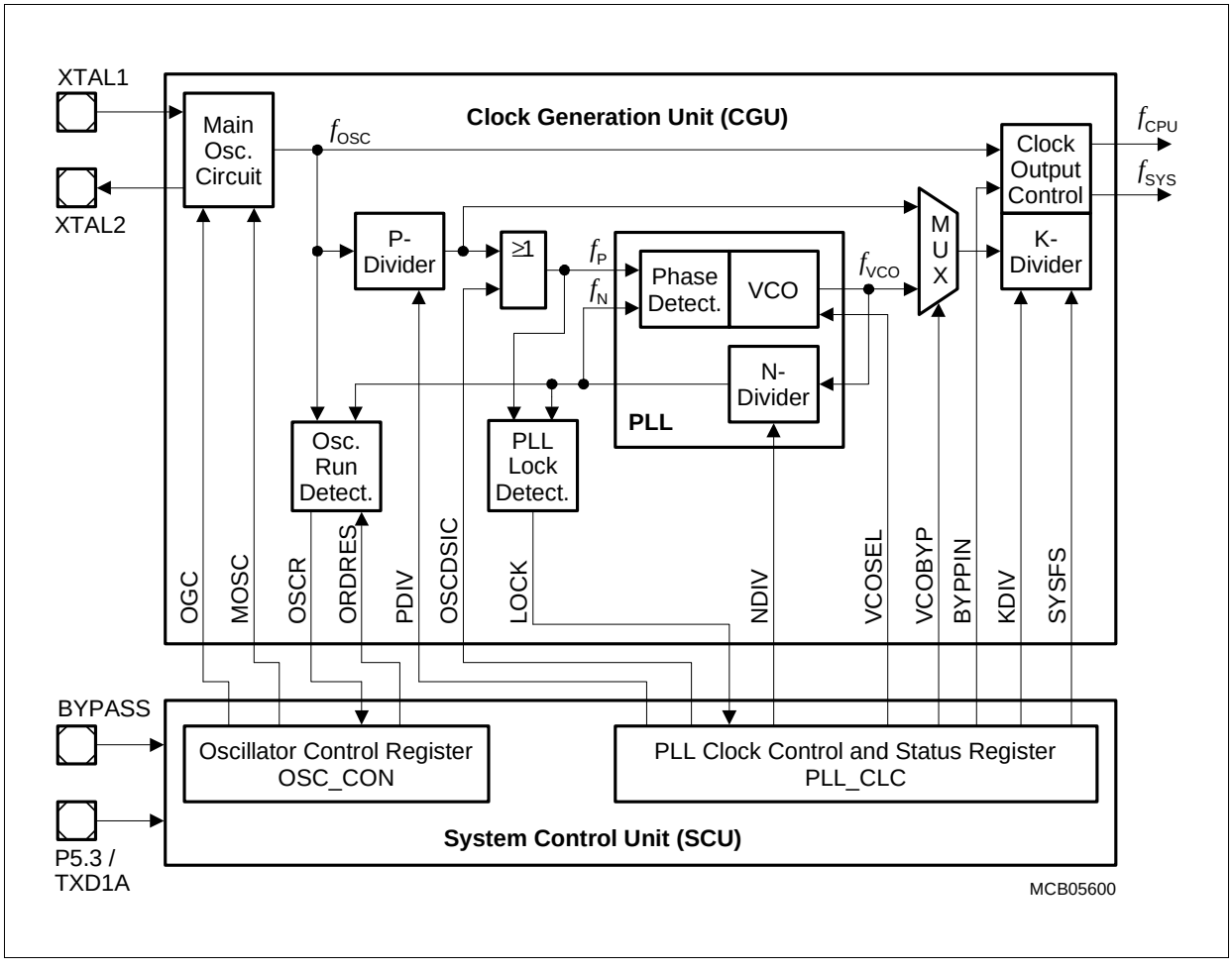


Figure 19 Clock Generation Unit

Recommended Oscillator Circuits

The oscillator circuit, a Pierce oscillator, is designed to work with both, an external crystal oscillator or an external stable clock source. It basically consists of an inverting amplifier and a feedback element with XTAL1 as input, and XTAL2 as output.

When using a crystal, a proper external oscillator circuitry must be connected to both pins, XTAL1 and XTAL2. The crystal frequency can be within the range of 4 MHz to 25 MHz. Additionally are necessary, two load capacitances C_{X1} and C_{X2}, and depending on the crystal type a series resistor R_{X2} to limit the current. A test resistor R_Q may be temporarily inserted to measure the oscillation allowance (negative resistance) of the oscillator circuitry. R_Q values are typically specified by the crystal vendor. The C_{X1} and C_{X2} values shown in **Figure 20** can be used as starting points for the negative resistance evaluation and for non-productive systems. The exact values and related operating range are dependent on the crystal frequency and have to be determined and

4.1.3 Absolute Maximum Ratings

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions (V_{IN} > related V_{DD} or V_{IN} < V_{SS}) the voltage on the related V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 11 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Ambient temperature	T_A	SR	-40	–	125	°C	Under bias
Storage temperature	T_{ST}	SR	-65	–	150	°C	–
Junction temperature	T_J	SR	-40	–	150	°C	Under bias
Voltage at 1.5 V power supply pins with respect to V_{SS} [1]	V_{DD}	SR	–	–	2.25	V	–
Voltage at 3.3 V power supply pins with respect to V_{SS} [2]	V_{DDEBU} V_{DDP}	SR	–	–	3.75	V	–
Voltage on any Class A input pin and dedicated input pins with respect to V_{SS}	V_{IN}	SR	-0.5	–	V_{DDP} + 0.5 or max. 3.7	V	Whatever is lower
Voltage on any Class B input pin with respect to V_{SS}	V_{IN}	SR	-0.5	–	V_{DDEBU} + 0.5 or max. 3.7	V	Whatever is lower
Voltage on any Class D analog input pin with respect to V_{AGND}	V_{AIN} V_{AREFx}	SR	-0.5	–	V_{DDM} + 0.5 or max. 3.7	V	Whatever is lower
Voltage on any Class D analog input pin with respect to V_{SSAF}	V_{AINF} V_{FAREF}	SR	-0.5	–	V_{DDMF} + 0.5 or max. 3.7	V	Whatever is lower
CPU & LMB Bus Frequency	f_{CPU}	SR	–	–	150[3]	MHz	–
FPI Bus Frequency	f_{SYS}	SR	–	–	75[3]	MHz	–

1) Applicable for V_{DD}, $V_{DDSBRAM}$, V_{DDOSC}, V_{DDPLL}, and V_{DDAF}.

2) Applicable for V_{DDP}, V_{DDEBU}, V_{DDFL3}, V_{DDM}, and V_{DDMF}.

3) The PLL jitter characteristics add to this value according to the application settings. See the PLL jitter parameters.

Table 13 Pin Groups for Overload/Short-Circuit Current Sum Parameter

Group	Pins
9	D[7:0]
10	A[23:16]
11	A[15:8]
12	A[7:0]
13	TSTRES, TDI, TMS, TCK, $\overline{\text{TRST}}$, TDO, $\overline{\text{BRKOUT}}$, $\overline{\text{BRKIN}}$, $\overline{\text{TESTMODE}}$
14	P10.[3:0], BYPASS, $\overline{\text{NMI}}$, $\overline{\text{PORST}}$, $\overline{\text{HDRST}}$
15	P9.[8:0]
16	FCLP[1:0]A, FCLN[1:0], SOP[1:0]A, SON[1:0]
17	P5.[7:0]
18	P3.[7:0]
19	P3.[15:8]
20	P0.[7:0]
21	P0.[15:8]
22	P2.[15:7]
23	P2.[6:2], P6.9, P6.8, P6.6, P6.11
24	P6.[15:12], P6.10, P6.7, P6.[5:4]
25	P8.[7:0]
26	P1.[15:13], P1.[11:8], P1.5
27	P1.12, P1.[7:6], P1.[4:0]
28	TR[15:8]
29	TR[7:1], TRCLK
30	TR0, P7.[7:0]

Table 15 ADC Characteristics (cont'd) (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Gain error[11)5)]	TUE_{GAIN}	CC	–	±0.5	±3.5	LSB	12-bit conversion [12)9)]
Offset error[11)5)]	TUE_{OFF}	CC	–	±1.0	±4.0	LSB	12-bit conversion [12)9)]
Input leakage current at analog inputs AN0, AN1, AN4 to AN7, AN24 to AN31. see **Figure 24** [13) 14)]	I_{OZ1}	CC	-1000	–	300	nA	(0% V_{DDM}) < V_{IN} < (2% V_{DDM})
			-200	–	400	nA	(2% V_{DDM}) < V_{IN} < (95% V_{DDM})
			-200	–	1000	nA	(95% V_{DDM}) < V_{IN} < (98% V_{DDM})
			-200	–	3000	nA	(98% V_{DDM}) < V_{IN} < (100% V_{DDM})
Input leakage current at the other analog inputs, that is AN2, AN3, AN8 to AN23, AN32 to AN43 see **Figure 24** [14)]	I_{OZ1}	CC	-1000	–	200	nA	(0% V_{DDM}) < V_{IN} < (2% V_{DDM})
			-200	–	300	nA	(2% V_{DDM}) < V_{IN} < (95% V_{DDM})
			-200	–	1000	nA	(95% V_{DDM}) < V_{IN} < (98% V_{DDM})
			-200	–	3000	nA	(98% V_{DDM}) < V_{IN} < (100% V_{DDM})
Input leakage current at V_{AREF}	I_{OZ2}	CC	–	–	±1	µA	0 V < V_{AREF} < V_{DDM}, no conversion running
Input current at $V_{AREF0/1}$[17)]	I_{AREF}	CC	–	35	75	µA rms	0 V < V_{AREF} < V_{DDM}[15)]
Total capacitance of the voltage reference inputs[16)17)]	$C_{AREFTOT}$	CC	–	–	25	pF	[9)]
Switched capacitance at the positive reference voltage input[17)]	C_{AREFSW}	CC	–	15	20	pF	[9)18)]

Table 17 FADC Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Conversion time	t_C	CC	–	–	21	CLK of f_{ADC}	10-bit conversion
Converter Clock	f_{ADC}	CC	–	–	75	MHz	–
Input resistance of the analog voltage path (Rn, Rp)	R_{FAIN}	CC	100	–	200	kΩ	10)
Channel Amplifier Cutoff Frequency	f_{COFF}	CC	2	–	–	MHz	–
Settling Time of a Channel Amplifier after changing ENN or ENP	t_{SET}	CC	–	–	5	µsec	–

1) Calibration of the gain is possible for the gain of 1 and 2, and not possible for the gain of 4 and 8.
2) Calibration should be performed at each power-up. In case of continuous operation, calibration should be performed minimum once per week.
3) The offset error voltage drifts over the whole temperature range maximum ±3 LSB.
4) Applies when the gain of the channel equals one. For the other gain settings, the offset error increases; it must be multiplied with the applied gain.
5) Voltage overshoot to 4 V are permissible, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h.
6) Voltage overshoot to 1.7 V are permissible, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.
7) A running conversion may become inexact in case of violating the normal operating conditions (voltage overshoots).
8) Current peaks of up to 40 mA with a duration of max. 2 ns may occur
9) This value applies in power-down mode.
10) Not subject to production test, verified by design / characterization.

The calibration procedure should run after each power-up, when all power supply voltages and the reference voltage have stabilized. The offset calibration must run first, followed by the gain calibration.

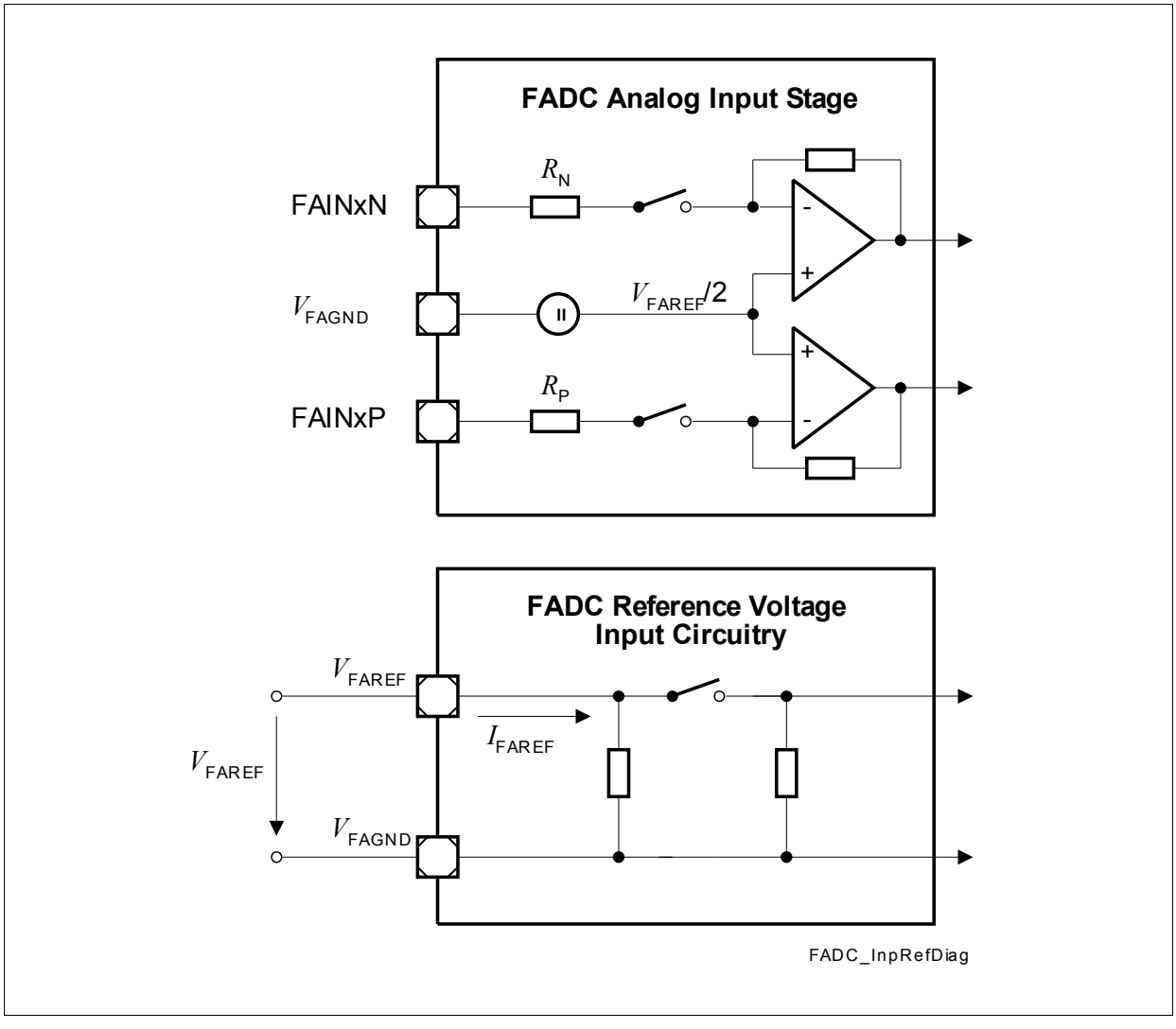


Figure 25 FADC Input Circuits

4.2.5 Temperature Sensor

Table 19 Temperature Sensor Characteristics (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Temperature Sensor Range	T_{SR}	SR	-40		150	°C	–
Start-up time after resets inactive	t_{TSST}	SR	–	–	10	µs	–
Sensor Inaccuracy	T_{TSA}	CC	–	–	±10	°C	–
A/D Converter clock for DTS signal	f_{ANA}	SR	–	–	10	MHz	conversion with ADC1

Table 20 Temperature Sensor Characteristics (Operating Conditions apply)

Parameter	Symbol		Typical Value	Unit	Note
Temperature of the die at the sensor location	T_{TS}	CC	T_{TS}× = (ADC_Code - 487) 0.396 - 40	°C	10-bit ADC result
			T_{TS}× = (ADC_Code - 1948) 0.099 - 40	°C	12-Bit ADC result

1) This parameter is valid under assumption that $\overline{\text{PORST}}$ signal is constantly at low level during the power-up/power-down of the V_{DDP}.
2) t_{OSCS} is defined from the moment when V_{DDOSC3} = 3.13V until the oscillations reach an amplitude at XTAL1 of 0,3*V_{DDOSC3}. This parameter is verified by device characterization. The external oscillator circuitry must be optimized by the customer and checked for negative resistance as recommended and specified by crystal suppliers.
3) Any $\overline{\text{HDRST}}$ activation is internally prolonged to 1024 FPI bus clock (f_{SYS}) cycles.
4) Applicable for input pins $\overline{\text{TESTMODE}}$, $\overline{\text{TRST}}$, $\overline{\text{BRKIN}}$, and TXD1A with noise suppression filter of $\overline{\text{PORST}}$ switched-on (BYPASS = 0).
5) The setup/hold values are applicable for Port 0 and Port 10 input pins with noise suppression filter of $\overline{\text{HDRST}}$ switched-on (BYPASS = 0), independently whether $\overline{\text{HDRST}}$ is used as input or output.
6) f_{SYS} = f_{CPU}/2
7) Not subject to production test, verified by design / characterization.
8) This parameter includes the delay of the analog spike filter in the $\overline{\text{PORST}}$ pad.
9) The duration of the boot-time is defined between the rising edge of the $\overline{\text{PORST}}$ and the moment when the first user instruction has entered the CPU and its processing starts.
10) The duration of the boot time is defined between the following events:
    1. Hardware reset: the falling edge of a short $\overline{\text{HDRST}}$ pulse and the moment when the first user instruction has entered the CPU and its processing starts, if the $\overline{\text{HDRST}}$ pulse is shorter than 1024 × T_{SYS}.
    If the $\overline{\text{HDRST}}$ pulse is longer than 1024 × T_{SYS}, only the time beyond the 1024 × T_{SYS} should be added to the boot time ($\overline{\text{HDRST}}$ falling edge to first user instruction).
    2. Software reset: the moment of starting the software reset and the moment when the first user instruction has entered the CPU and its processing starts

4.3.6 BFCLKO Output Clock Timing

V_{SS} = 0 V;V_{DD} = 1.5 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%;
T_A = -40 °C to +125 °C; C_L = 35 pF

Table 25 BFCLK0 Output Clock Timing Parameters[1)]

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
BFCLKO clock period	t_{BFCLKO}	CC	13.33[2)]	–	–	ns	–
BFCLKO high time	t_5	CC	3	–	–	ns	–
BFCLKO low time	t_6	CC	3	–	–	ns	–
BFCLKO rise time	t_7	CC	–	–	3	ns	–
BFCLKO fall time	t_8	CC	–	–	3	ns	–
BFCLKO duty cycle $t_5/(t_5 + t_6)$[3)]	$DC24$	CC	45	50	55	%	divider of 2, 4, ...[4)]
BFCLKO duty cycle $t_5/(t_5 + t_6)$[3)]	$DC3$	CC	30	33.33	36	%	divider of 3 [4)]
BFCLKO high time reduction[5)]	dt_5	CC	–	–	1.1	ns	C_L = 20pF

1) Not subject to production test, verified by design/characterization.
2) The PLL jitter characteristics add to this value according to the application settings. See the PLL jitter parameters.
3) The PLL jitter is not included in this parameter. If the BFCLKO frequency is equal to f_{CPU}, the K-divider setting determines the duty cycle.
4) The division ratio between LMB and BFCLKO frequency is set by EBU_BFCON.EXTCLOCK.
5) Due to asymmetry of the delays and slopes of the rising and falling edge of the pad. The influence of the PLL jitter is included in this parameter. This parameter should be applied taking the typical value of the duty cycle in the account, not the minimum or maximum value.

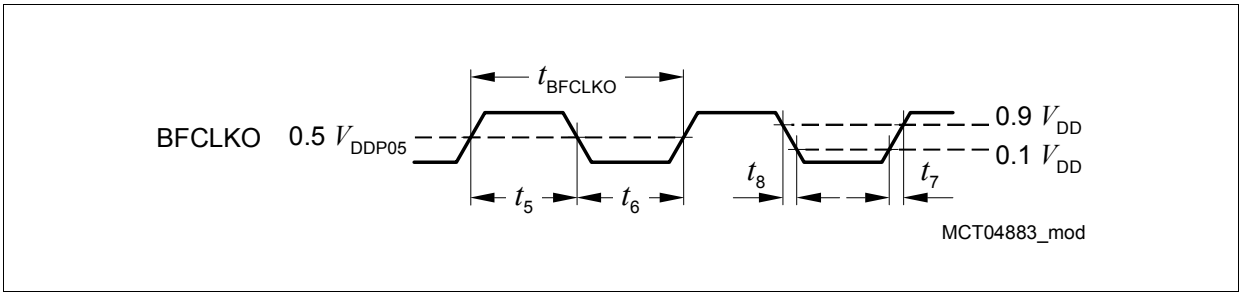


Figure 34 BFCLKO Output Clock Timing

Table 28 JTAG Timing Parameters[1)]

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TMS setup to TCK rising edge	t_1	SR	6.0	–	–	ns	–
TMS hold to TCK rising edge	t_2	SR	6.0	–	–	ns	–
TDI setup to TCK rising edge	t_1	SR	6.0	–	–	ns	–
TDI hold to TCK rising edge	t_2	SR	6.0	–	–	ns	–
TDO valid output from TCK falling edge[2)]	t_3	CC	–	–	13	ns	C_L = 50 pF
	t_3	CC	3.0	–	–	ns	C_L = 20 pF
TDO high impedance to valid output from TCK falling edge[2)]	t_4	CC	–	–	14	ns	C_L = 50 pF
TDO valid output to high impedance from TCK falling edge[2)]	t_5	CC	–	–	13.5	ns	C_L = 50 pF

1) f_{TCK} should be lower or equal to f_{SYS}.

2) The falling edge on TCK is used to capture the TDO timing.

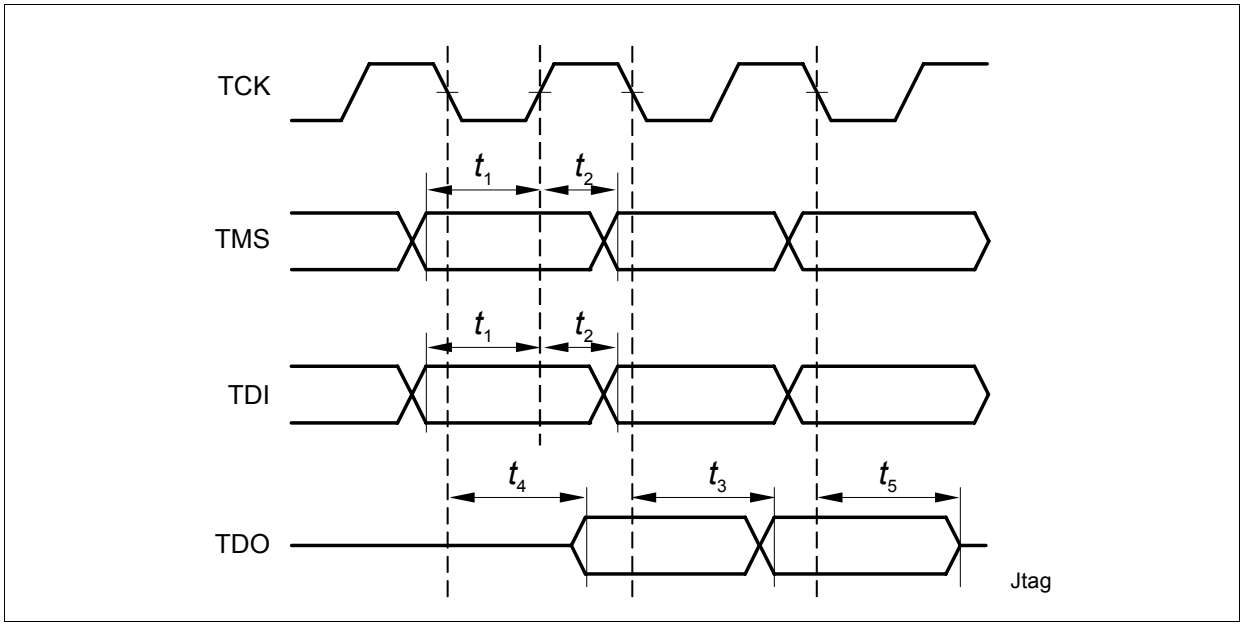
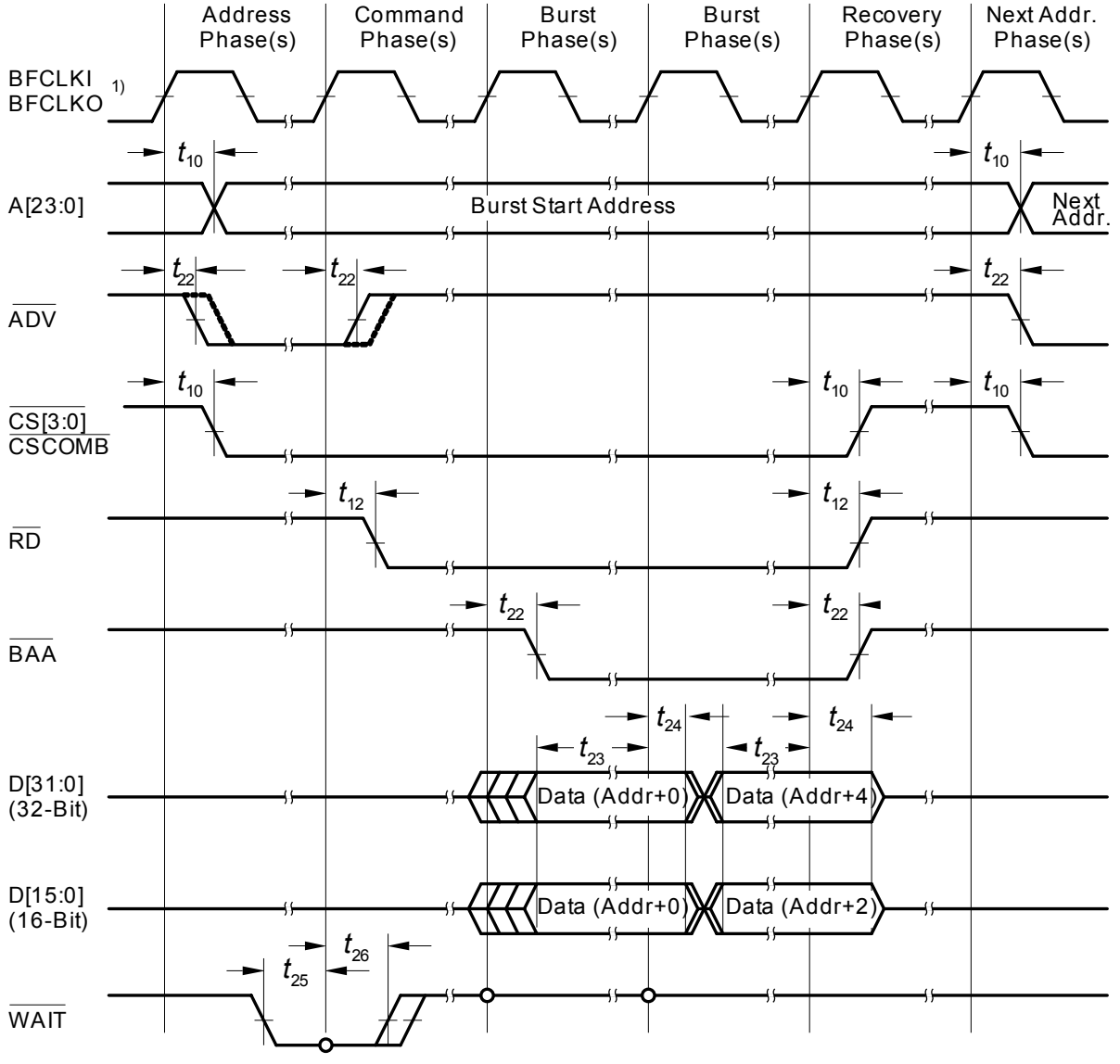


Figure 37 JTAG Timing

*Note: The JTAG module is fully compliant with IEEE1149.1-2000 with JTAG clock at 20 MHz. The JTAG clock at 40MHz is possible with the modified timing diagram shown in **Figure 37**.*



1) Output delays are always referenced to BCLKO. The reference clock for input characteristics depends on bit EBU_BFCON.FDBKEN.
EBU_BFCON.FDBKEN = 0:BFCLKO is the input reference clock.
EBU_BFCON.FDBKEN = 1:BFCLKI is the input reference clock (EBU clock feedback enabled).

BurstRD_4.vsd

Figure 40 EBU Burst Mode Read Timing

w w w . i n f i n e o n . c o m

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