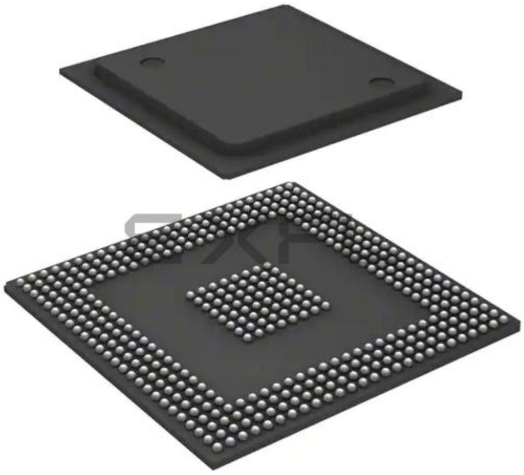

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	ASC, CANbus, EBI/EMI, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	123
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 44x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BGA
Supplier Device Package	PG-BGA-416
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1796256f150ebekxuma2

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions
P4		I/O	A1/A2	V_{DDP}	**Port 4** Port 4 is a 16-bit bi-directional general-purpose I/O port which can be alternatively used for GPTA I/O lines.
P4.0	AD10	I/O	A2[1)]		IN24 / OUT24 line of GPTA
P4.1	AE10	I/O	A2[1)]		IN25 / OUT25 line of GPTA
P4.2	AD11	I/O	A2[1)]		IN26 / OUT26 line of GPTA
P4.3	AE11	I/O	A2[1)]		IN27 / OUT27 line of GPTA
P4.4	AC12	I/O	A2[1)]		IN28 / OUT28 line of GPTA
P4.5	AD12	I/O	A2[1)]		IN29 / OUT29 line of GPTA
P4.6	AF10	I/O	A2[1)]		IN30 / OUT30 line of GPTA
P4.7	AE12	I/O	A2[1)]		IN31 / OUT31 line of GPTA
P4.8	AC13	I/O	A1		IN32 / OUT32 line of GPTA
P4.9	AF11	I/O	A1		IN33 / OUT33 line of GPTA
P4.10	AF12	I/O	A1		IN34 / OUT34 line of GPTA
P4.11	AD13	I/O	A1		IN35 / OUT35 line of GPTA
P4.12	AC14	I/O	A1		IN36 / OUT36 line of GPTA
P4.13	AE13	I/O	A1		IN37 / OUT37 line of GPTA
P4.14	AF13	I/O	A1		IN38 / OUT38 line of GPTA
P4.15	AD14	I/O	A1		IN39 / OUT39 line of GPTA

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions	
P5		I/O	A2	V_{DDP}	**Port 5** Port 5 is an 8-bit bi-directional general-purpose I/O port which can be alternatively used for ASC0/1 or MSC0/1 lines.	
P5.0	B13	I/O			RXD0A	ASC0 receiver input / output A
P5.1	A13	O			TXD0A	ASC0 transmitter output A
P5.2	A14	I/O			RXD1A	ASC1 receiver input / output A
P5.3	B14	O			TXD1A	ASC1 transmitter output A P5.3 is latched with the rising edge of $\overline{\text{PORST}}$ if BYPASS = 1 and stored in inverted state as bit OSC_CON.MOSC.
P5.4	C15	O			EN00	MSC0 device select output 0
		O			RREADY0B	MLI0 receive channel ready output B
P5.5	C14	I			SDI0	MSC0 serial data input
P5.6	B15	O			EN10	MSC1 device select output 0
		O			TVALID0B	MLI0 transmit channel valid output B
P5.7	A15	I			SDI1	MSC1 serial data input

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Class	Power Supply	Functions	
P9		I/O	A2	V_{DDP}	**Port 9** Port 9 is a 9-bit bi-directional general-purpose I/O port which can be alternatively used as GPTA or MSC0/1 I/O lines.	
P9.0	A19	I/O O			IN48/OUT48 EN12	I/O line of GPTA MSC1 device select output 2
P9.1	B19	I/O O			IN49/OUT49 EN11	I/O line of GPTA MSC1 device select output 1
P9.2	B20	I/O O			IN50/OUT50 SOP1B	I/O line of GPTA MSC1 serial data output
P9.3	A20	I/O O			IN51/OUT51 FCLP1	I/O line of GPTA MSC1 clock output
P9.4	D18	I/O O			IN52/OUT52 EN03	I/O line of GPTA MSC0 device select output 3
P9.5	D19	I/O O			IN53/OUT53 EN02	I/O line of GPTA MSC0 device select output 2
P9.6	C19	I/O O			IN54/OUT54 EN01	I/O line of GPTA MSC0 device select output 1
P9.7	D20	I/O O			IN55/OUT55 SOP0B	I/O line of GPTA MSC0 serial data output
P9.8	C20	O			FCLP0B	MSC0 clock output

- Data buffering supported
  - Code prefetch buffer
  - Read/write buffer
- External bus arbitration control capability for the EBU bus
- Automatic self-configuration on boot from external memory

3.6 Peripheral Control Processor

The Peripheral Control Processor (PCP2) in the TC1796 performs tasks that would normally be performed by the combination of a DMA controller and its supporting CPU interrupt service routines in a traditional computer system. It could easily be considered as the host processor's first line of defence as an interrupt-handling engine. The PCP2 can off-load the CPU from having to service time-critical interrupts. This provides many benefits, including:

- Avoiding large interrupt-driven task context-switching latencies in the host processor
- Reducing the cost of interrupts in terms of processor register and memory overhead
- Improving the responsiveness of interrupt service routines to data-capture and data-transfer operations
- Easing the implementation of multitasking operating systems.

The PCP2 has an architecture that efficiently supports DMA-type transactions to and from arbitrary devices and memory addresses within the TC1796 and also has reasonable stand-alone computational capabilities.

The PCP2 in the TC1796 contains an improved version of the TC1775's PCP with the following enhancements:

- Optimized context switching
- Support for nested interrupts
- Enhanced instruction set
- Enhanced instruction execution speed
- Enhanced interrupt queueing

The PCP2 is made up of several modular blocks as follows (see **Figure 5**):

- PCP2 Processor Core
- Code Memory (CMEM)
- Parameter Memory (PRAM)
- PCP2 Interrupt Control Unit (PICU)
- PCP2 Service Request Nodes (PSRN)
- System bus interface to the Flexible Peripheral Interface (FPI Bus)

Note: Although the polynomial above is used for generation, the generation algorithm differs from the one that is used by the Ethernet protocol.

3.8 Interrupt System

The TC1796 interrupt system provides a flexible and time-efficient means for processing interrupts. An interrupt request can be serviced either by the CPU or by the Peripheral Control Processor (PCP). These units are called “Service Providers”. Interrupt requests are called “Service Requests” rather than “Interrupt Requests” in this document because they can be serviced by either of the Service Providers.

Each peripheral in the TC1796 can generate service requests. Additionally, the Bus Control Units, the Debug Unit, the PCP, and even the CPU itself can generate service requests to either of the two Service Providers.

As shown in **Figure 7**, each TC1796 unit that can generate service requests is connected to one or more Service Request Nodes (SRN). Each SRN contains a Service Request Control Register. Two arbitration buses connect the SRNs with two Interrupt Control Units, which handle interrupt arbitration among competing interrupt service requests, as follows:

- The Interrupt Control Unit (ICU) arbitrates service requests for the CPU and administers the CPU Interrupt Arbitration Bus.
- The Peripheral Interrupt Control Unit (PICU) arbitrates service requests for the PCP2 and administers the PCP2 Interrupt Arbitration Bus.

The PCP2 can make service requests directly to itself (via the PICU), or it can make service requests to the CPU. The Debug Unit can generate service requests to the PCP2 or the CPU. The CPU can make service requests directly to itself (via the ICU), or it can make service requests to the PCP. The CPU Service Request Nodes are activated through software.

Depending on the selected system clock frequency f_{SYS}, the number of f_{SYS} clock cycles per arbitration cycle must be selected as follows:

- $f_{SYS} < 60$MHz: ICR.CONECYC = 1 and PCP_ICR.CONECYC = 1
- $f_{SYS} > 60$MHz: ICR.CONECYC = 0 and PCP_ICR.CONECYC = 0

or can be received from an external master (Slave Mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data is double-buffered. A shift clock generator provides the SSC with a separate serial clock signal. One slave select input is available for Slave Mode operation. Eight programmable slave select outputs (chip selects) are supported in Master Mode. The I/O lines of the SSC0 module are connected to dedicated device pins while the SSC1 module I/O lines are wired with general purpose I/O port lines.

Features

- Master and Slave Mode operation
  - Full-duplex or half-duplex operation
  - Automatic pad control possible
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: Idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Baud rate generation from 37.5 Mbit/s to 572.2 Bit/s (@ 75 MHz module clock)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)
- Flexible SSC pin configuration
- One slave select input $\overline{\text{SLSI}}$ in slave mode
- Eight programmable slave select outputs SLSO in Master Mode
  - Automatic SLSO generation with programmable timing
  - Programmable active level and enable control
- SSC0 with 8-stage receive FIFO (RXFIFO) and 8-stage transmit FIFO (TXFIFO)
  - Independent control of RXFIFO and TXFIFO
  - 2- to 16-bit FIFO data width
  - Programmable receive/transmit interrupt trigger level
  - Receive and Transmit FIFO filling level indication
  - Overrun error generation
  - Underflow error generation

I/O Sharing Unit

- Interconnecting inputs and outputs from internal clocks, FPC, GTC, LTC, ports, and MSC interface.

3.14.2 Functionality of LTCA2

One Local Timer Cells Area provides a set of Local Timer Cells.

- 64 Local Timer Cells (LTCs)
  - Three basic operating modes (Timer, Capture and Compare) for 63 units.
  - Special compare modes for one unit
  - 16-bit data width
  - f_{GPTA} maximum resolution
  - $f_{GPTA}/2$ maximum input signal frequency

The A/D converters operate by the method of the successive approximation. A multiplexer selects between up to 32 analog inputs that can be connected with the 16 conversion channels in each ADC module. An automatic self-calibration adjusts the ADC modules to changing temperatures or process variations.

External Clock control, address decoding, and service request (interrupt) control is managed outside the ADC module kernel. A synchronization bridge is used for synchronization of two ADC modules. External trigger conditions are controlled by an External Request Unit. This unit generates the control signals for auto-scan control (ASGT), software trigger control (SW0TR, SW0GT), the event trigger control (ETR, EGT), queue control (QTR, QGT), and timer trigger control (TTR, TGT).

Features

- 8-bit, 10-bit, 12-bit A/D conversion
- Minimum conversion times (without sample time, @ 75 MHz module clock):
  - 1.05 μs @ 8-bit resolution
  - 1.25 μs @ 10-bit resolution
  - 1.45 μs @ 12-bit resolution
- Extended channel status information on request source
- Successive approximation conversion method
- Total Unadjusted Error (TUE) of ±2 LSB @ 10-bit resolution
- Integrated sample & hold functionality
- Direct control of up to 16(32) analog input channels per ADC
- Dedicated control and status registers for each analog channel
- Powerful conversion request sources
- Selectable reference voltages for each channel
- Programmable sample and conversion timing schemes
- Limit checking
- Flexible ADC module service request control unit
- Synchronization of the two on-chip A/D converters
- Automatic control of external analog multiplexers
- Equidistant samples initiated by timer
- External trigger and gating inputs for conversion requests
- Power reduction and clock control feature
- On-chip die temperature sensor output voltage measurement via ADC1

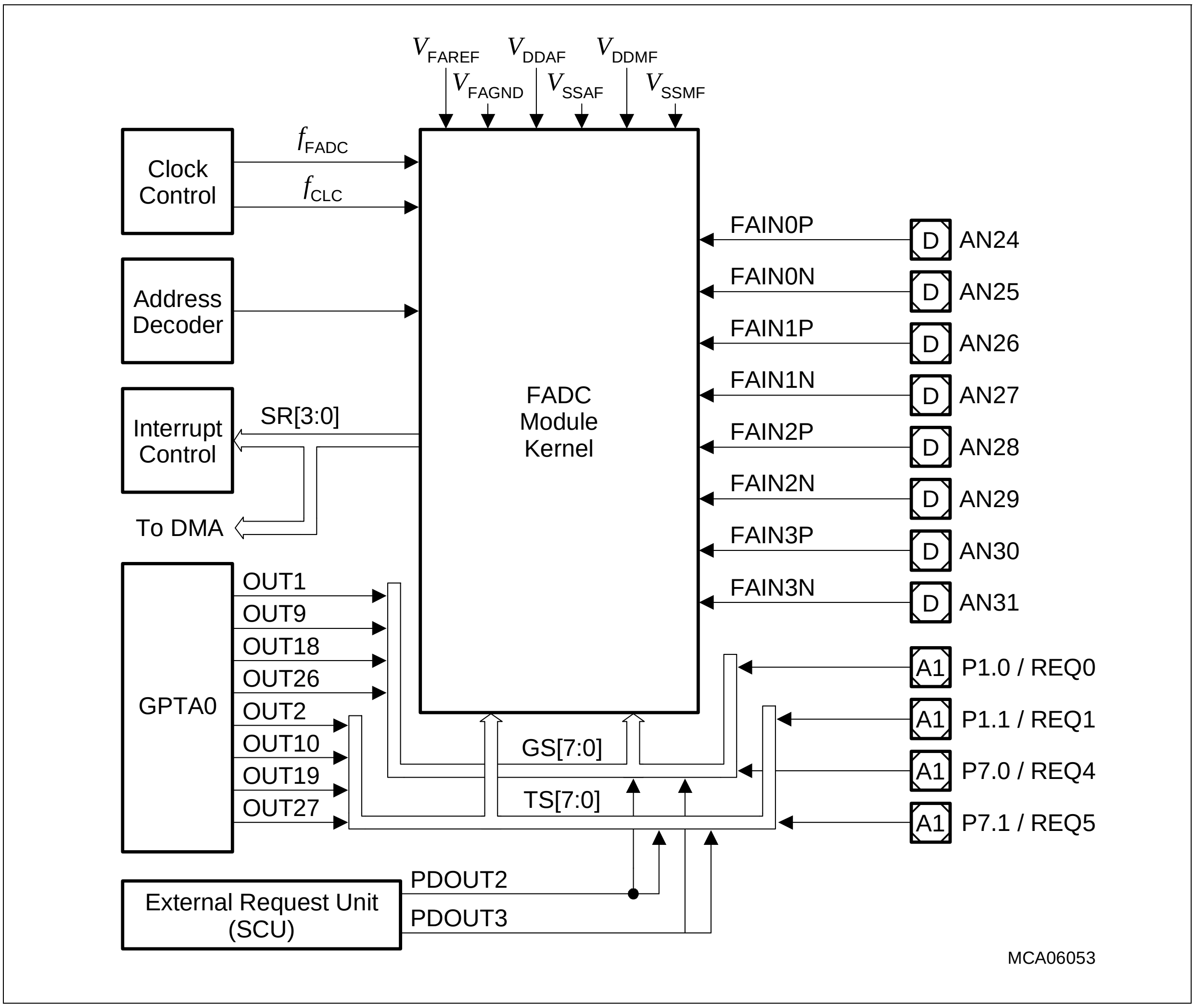

Figure 16 Block Diagram of the FADC Module

Features

- Extreme fast conversion: 21 cycles of f_{FADC} (= 280ns @ f_{FADC} = 75 MHz)
- 10-bit A/D conversion
  – Higher resolution by averaging of consecutive conversions is supported
- Successive approximation conversion method
- Four differential input channels
- Offset and gain calibration support for each channel
- Differential input amplifier with programmable gain of 1, 2, 4 and 8 for each channel
- Free-running (Channel Timers) or triggered conversion modes
- Trigger and gating control for external signals
- Built-in Channel Timers for internal triggering
- Channel timer request periods independently selectable for each channel
- Selectable, programmable anti aliasing and data reduction filter block

3.22 On-Chip Debug Support

Figure 18 shows a block diagram of the TC1796 OCDS system.

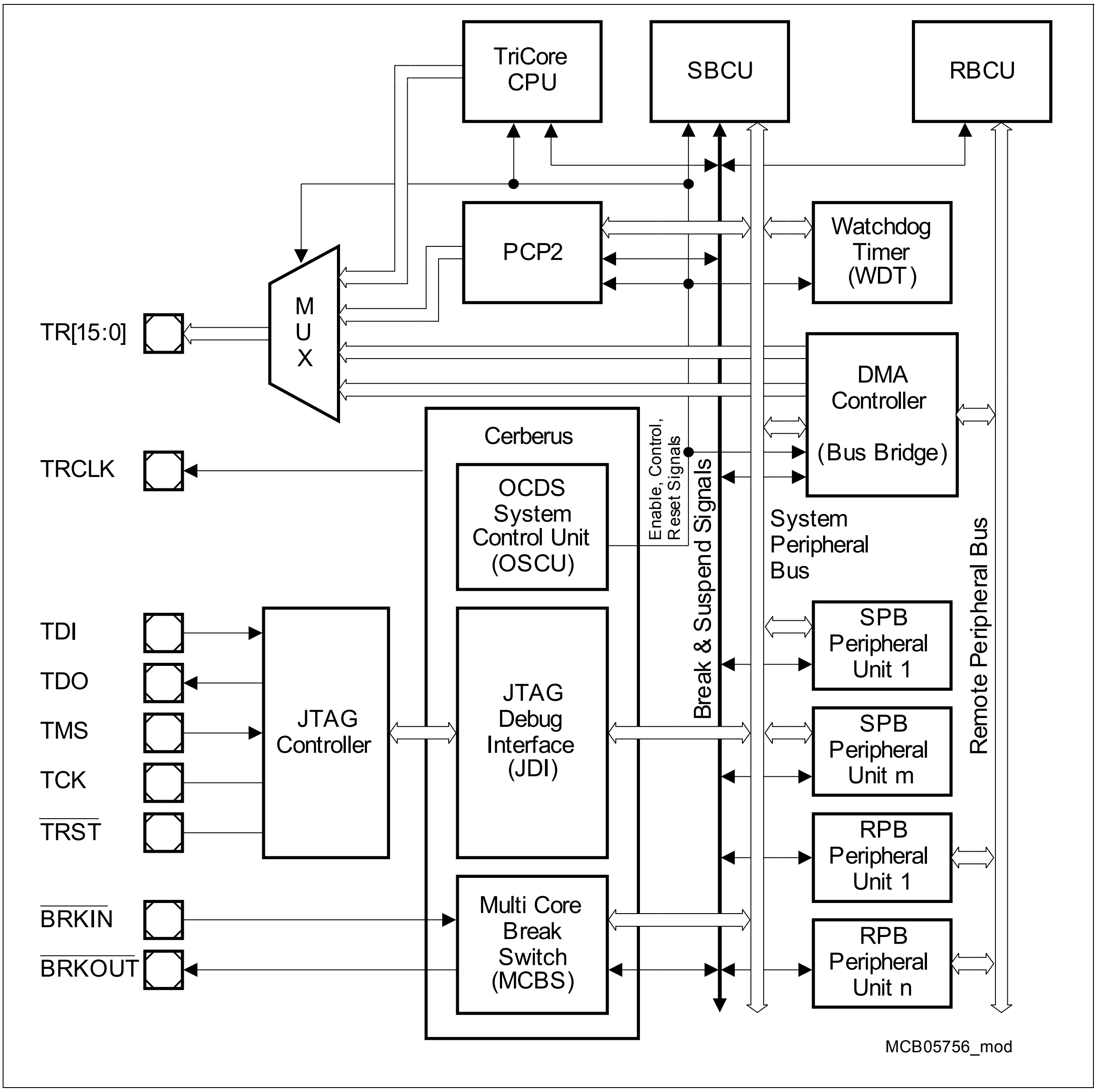

Figure 18 OCDS System Block Diagram

The TC1796 basically supports three levels of debug operation:

- OCDS Level 1 debug support
- OCDS Level 2 debug support
- OCDS Level 3 debug support

are derived from f_{VCO} only by the K-Divider. In this mode, the system clock f_{SYS} can be equal to f_{CPU} or $f_{CPU}/2$.

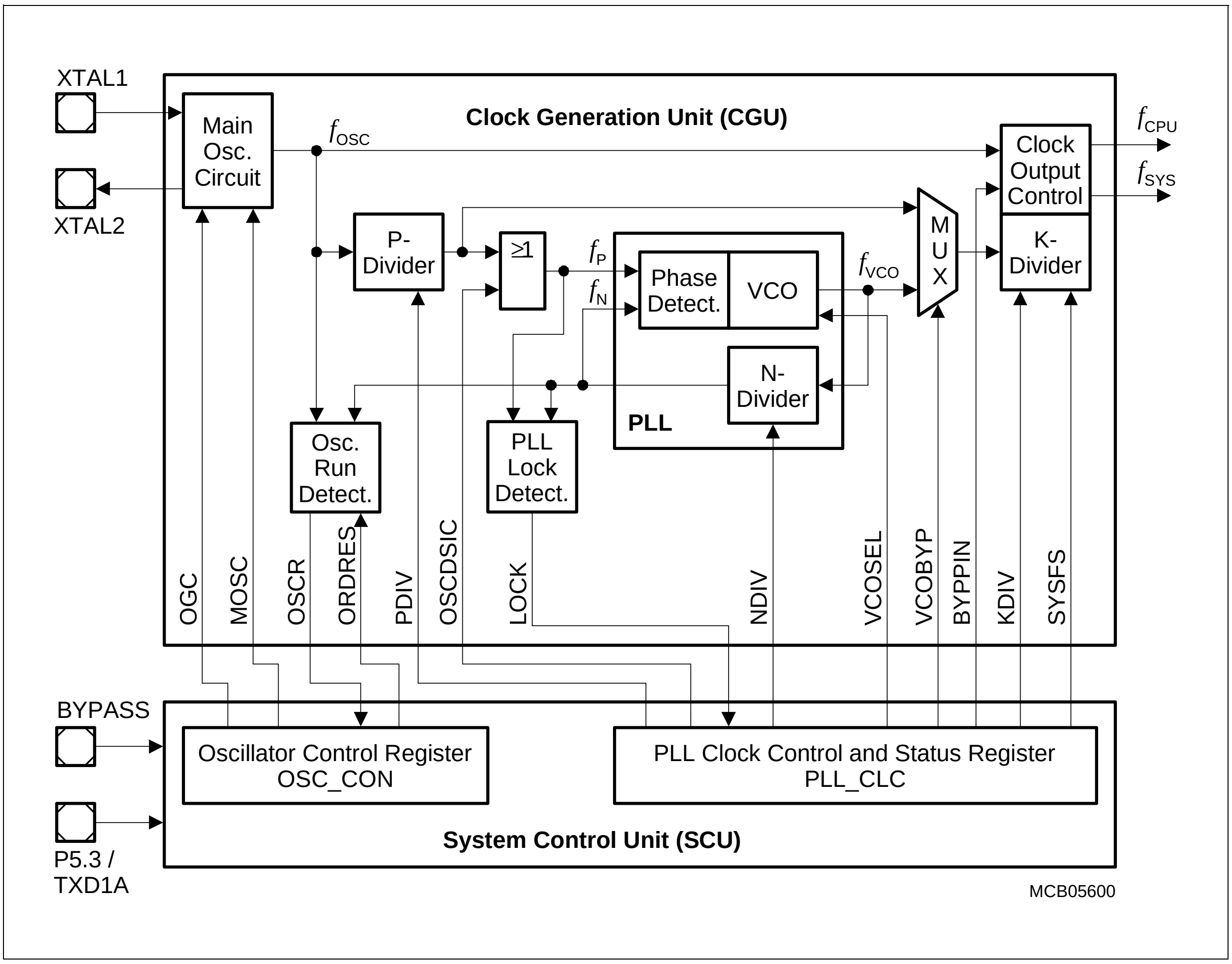

Figure 19 Clock Generation Unit

Recommended Oscillator Circuits

The oscillator circuit, a Pierce oscillator, is designed to work with both, an external crystal oscillator or an external stable clock source. It basically consists of an inverting amplifier and a feedback element with XTAL1 as input, and XTAL2 as output.

When using a crystal, a proper external oscillator circuitry must be connected to both pins, XTAL1 and XTAL2. The crystal frequency can be within the range of 4 MHz to 25 MHz. Additionally are necessary, two load capacitances C_{X1} and C_{X2}, and depending on the crystal type a series resistor R_{X2} to limit the current. A test resistor R_Q may be temporarily inserted to measure the oscillation allowance (negative resistance) of the oscillator circuitry. R_Q values are typically specified by the crystal vendor. The C_{X1} and C_{X2} values shown in **Figure 20** can be used as starting points for the negative resistance evaluation and for non-productive systems. The exact values and related operating range are dependent on the crystal frequency and have to be determined and

Table 12 Operating Condition Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Absolute sum of short circuit currents of the device	$\Sigma\lvert I_{SC}\rvert$	SR	–	–	100	mA	See note[10)]
External load capacitance	C_L	SR	–	–	–	pF	Depending on pin class. See DC characteristics

1) Digital supply voltages applied to the TC1796 must be static regulated voltages which allow a typical voltage swing of ±5%.

2) V_{DDOSC} and V_{SSOSC} are not bonded externally in the BC and BD steps of TC1796. An option for bonding them in future steps and products is kept open.

3) Voltage overshoot up to 1.7 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h.

4) Voltage overshoot to 4 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h

5) The V_{DDSB} must be properly connected and supplied with power. If not, the TC1796 will not operate. In case of a stand-by operation, the core voltage must not float, but must be pulled low, in order to avoid internal cross-currents.

6) This applies only during power down state. During normal SRAM operation regular V_{DD} has to be applied.

7) The TC1796 uses a static design, so the minimum operation frequency is 0 MHz. Due to test time restriction no lower frequency boundary is tested, however.

8) The PLL jitter characteristics add to this value according to the application settings. See the PLL jitter parameters.

9) Applicable for digital outputs.

10) See additional document “TC1796 Pin Reliability in Overload“ for overload current definitions.

Table 13 Pin Groups for Overload/Short-Circuit Current Sum Parameter

Group	Pins
1	P4.[7:0]
2	P4.[14:8]
3	P4.15, SLSO[1:0], SCLK0, MTSR0, MRST0, $\overline{\text{SLSI0}}$
4	$\overline{\text{WAIT}}$, $\overline{\text{HOLD}}$, $\overline{\text{BC[3:0]}}$, $\overline{\text{HLDA}}$, MR/$\overline{\text{W}}$, $\overline{\text{BAA}}$, $\overline{\text{CSCOMB}}$
5	$\overline{\text{CS[3:0]}}$, $\overline{\text{RD}}$, RD/$\overline{\text{WR}}$, $\overline{\text{BREQ}}$, $\overline{\text{ADV}}$, BFCLKO
6	BFCLKI, D[31:24]
7	D[23:16]
8	D[15:8]

Table 15 ADC Characteristics (cont'd) (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain error[11)5)]	TUE_{GAIN} CC	–	±0.5	±3.5	LSB	12-bit conversion [12)9)]
Offset error[11)5)]	TUE_{OFF} CC	–	±1.0	±4.0	LSB	12-bit conversion [12)9)]
Input leakage current at analog inputs AN0, AN1, AN4 to AN7, AN24 to AN31. see **Figure 24** [13) 14)]	I_{OZ1} CC	-1000	–	300	nA	(0% V_{DDM}) < V_{IN} < (2% V_{DDM})
		-200	–	400	nA	(2% V_{DDM}) < V_{IN} < (95% V_{DDM})
		-200	–	1000	nA	(95% V_{DDM}) < V_{IN} < (98% V_{DDM})
		-200	–	3000	nA	(98% V_{DDM}) < V_{IN} < (100% V_{DDM})
Input leakage current at the other analog inputs, that is AN2, AN3, AN8 to AN23, AN32 to AN43 see **Figure 24** [14)]	I_{OZ1} CC	-1000	–	200	nA	(0% V_{DDM}) < V_{IN} < (2% V_{DDM})
		-200	–	300	nA	(2% V_{DDM}) < V_{IN} < (95% V_{DDM})
		-200	–	1000	nA	(95% V_{DDM}) < V_{IN} < (98% V_{DDM})
		-200	–	3000	nA	(98% V_{DDM}) < V_{IN} < (100% V_{DDM})
Input leakage current at V_{AREF}	I_{OZ2} CC	–	–	±1	μA	0 V < V_{AREF} < V_{DDM}, no conversion running
Input current at $V_{AREF0/1}$ [17)]	I_{AREF} CC	–	35	75	μA rms	0 V < V_{AREF} < V_{DDM} [15)]
Total capacitance of the voltage reference inputs[16)17)]	$C_{AREFTOT}$ CC	–	–	25	pF	[9)]
Switched capacitance at the positive reference voltage input[17)]	C_{AREFSW} CC	–	15	20	pF	[9)18)]

4.2.3 Fast Analog to Digital Converter (FADC)

Table 17 FADC Characteristics (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DNL error	E_{DNL}	CC	–	–	±1	LSB	[10]
INL error	E_{INL}	CC	–	–	±4	LSB	[10]
Gradient error[1)10)]	E_{GRAD}	CC	–	–	±3	%	With calibration, gain 1, 2[2)]
	E_{GRAD}	CC	–	–	±5	%	Without calibration gain 1, 2, 4
	E_{GRAD}	CC	–	–	±6	%	Without calibration gain 8
Offset error[10)]	E_{OFF}[3)]	CC	–	–	±20[4)]	mV	With calibration[2)]
			–	–	±60[4)]	mV	Without calibration
Reference error of internal $V_{FAREF}/2$	E_{REF}	CC	–	–	±60	mV	–
Analog supply voltages	V_{DDMF}	SR	3.13	–	3.47[5)]	V	–
	V_{DDAF}	SR	1.42	–	1.58[6)]	V	–
Analog ground voltage	V_{SSAF}	SR	-0.1	–	0.1	V	–
Analog reference voltage	V_{FAREF}	SR	3.13	–	3.47[5)7)]	V	Nominal 3.3 V
Analog reference ground	V_{FAGND}	SR	V_{SSAF} - 0.05V	–	V_{SSAF} +0.05V	V	–
Analog input voltage range	V_{AINF}	SR	V_{FAGND}	–	V_{DDMF}	V	–
Analog supply currents	I_{DDMF}	SR	–	–	9	mA	–
	I_{DDAF}	SR	–	–	17	mA	[8)]
Input current at each V_{FAREF}	I_{FAREF}	CC	–	–	150	μA rms	Independent of conversion
Input leakage current at V_{FAREF}[9)]	I_{FOZ2}	CC	–	–	±500	nA	$0 V < V_{IN} < V_{DDMF}$
Input leakage current at V_{FAGND}	I_{FOZ3}	CC	–	–	±8	μA	$0 V < V_{IN} < V_{DDMF}$

4.3 AC Parameters

All AC parameters are defined with the temperature compensation disabled. That means, keeping the pads constantly at maximum strength.

4.3.1 Testing Waveforms

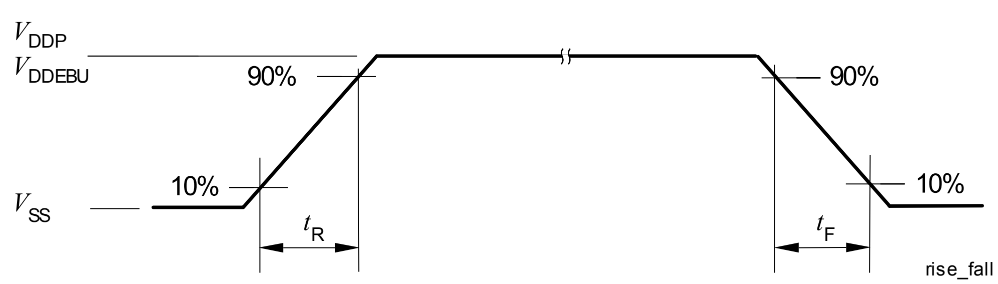

Figure 26 Rise/Fall Time Parameters

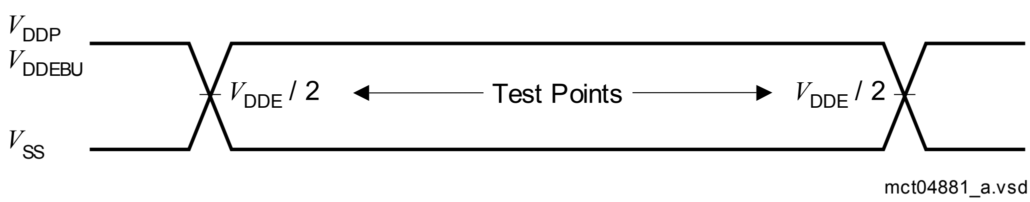

Figure 27 Testing Waveform, Output Delay

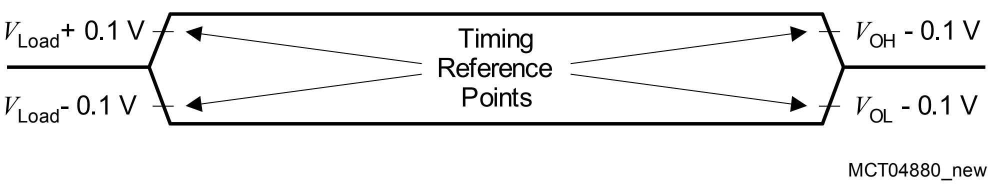

Figure 28 Testing Waveform, Output High Impedance

4.3.8 JTAG Interface Timing

Operating Conditions apply, CL = 50 pF

Table 27 TCK Clock Timing Parameter

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TCK clock period[1)]	t_{TCK}	SR	25	–	–	ns	–
TCK high time	t_1	SR	10	–	–	ns	–
TCK low time	t_2	SR	10	–	–	ns	–
TCK clock rise time	t_3	SR	–	–	4	ns	–
TCK clock fall time	t_4	SR	–	–	4	ns	–

1) f_{TCK} should be lower or equal to f_{SYS}.

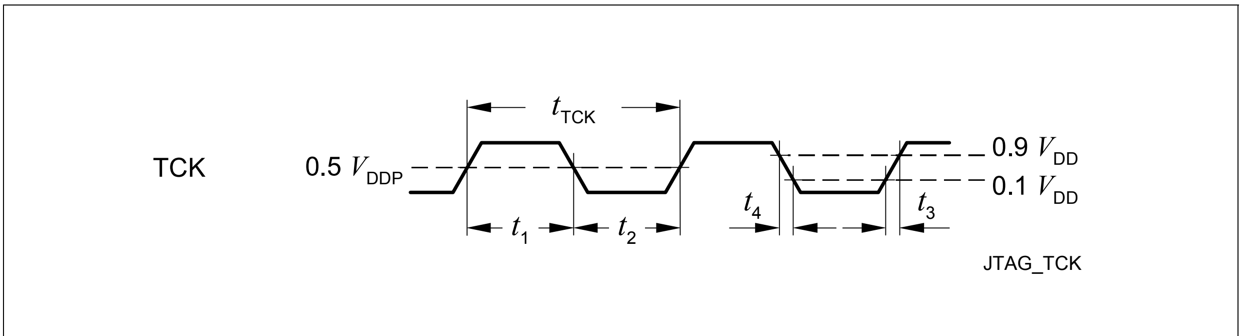

Figure 36 TCK Clock Timing

4.3.9 EBU Demultiplexed Timing

V_{SS} = 0 V; V_{DD} = 1.5 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%, Class B pins;
T_A = -40 °C to +125 °C; C_L = 35 pF;

Table 29 EBU Demultiplexed Timing Parameters[1)]

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Output delay from BFCLKO rising edge[2)]	t_{10}	CC	0	–	5	ns	–
$\overline{\text{RD}}$ active/inactive after BFCLKO rising edge[2)]	t_{12}	CC	0	–	3	ns	–
Data setup to BFCLKO rising edge[2)]	t_{13}	SR	8.5	–	–	ns	–
Data hold from BFCLKO rising edge[2)]	t_{14}	SR	0	–	–	ns	–
$\overline{\text{WAIT}}$ setup (low or high) to BFCLKO rising edge[2)]	t_{15}	SR	3	–	–	ns	–
$\overline{\text{WAIT}}$ hold (low or high) from BFCLKO rising edge[2)]	t_{16}	SR	2	–	–	ns	–
Data hold after RD/$\overline{\text{WR}}$ rising edge	t_{17}	SR	0	–	–	ns	–

1) Not subject to production test, verified by design/characterization.

2) Valid for BFCON.EXTCLOCK = 00_B.

4.3.9.2 Demultiplexed Write Timing

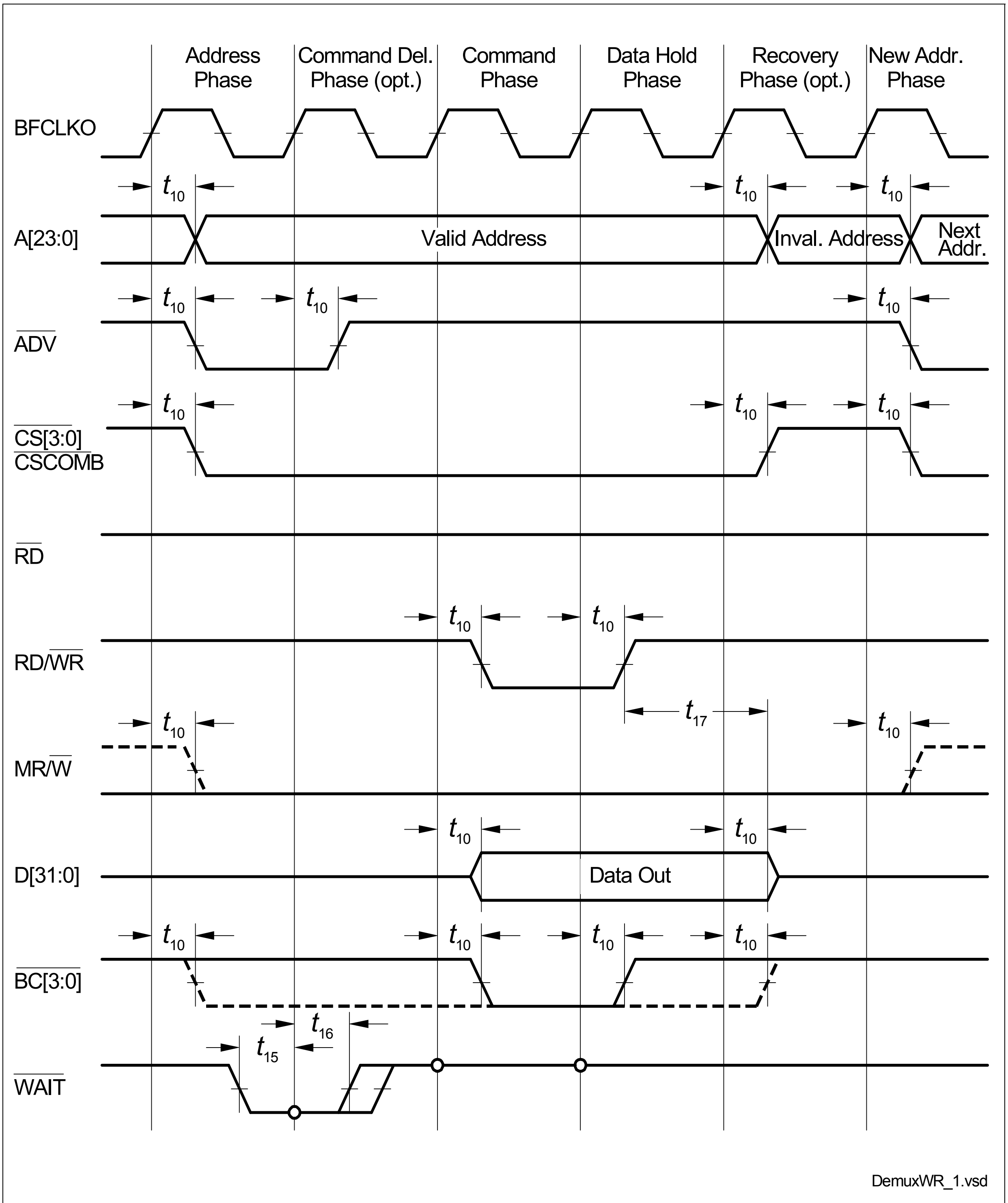

Figure 39 EBU Demultiplexed Write Timing

4.3.11 EBU Arbitration Signal Timing

V_{SS} = 0 V; V_{DD} = 1.5 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%, Class B pins;
T_A = -40°C to +125 °C; C_L = 35 pF;

Table 31 EBU Arbitration Signal Timing Parameters[1)]

Parameter	Symbol		Values			Unit	Note / Test Con dition
			Min.	Typ.	Max.		
Output delay from CLKOUT rising edge	t_{27}	CC	–	–	3	ns	–
Data setup to CLKOUT falling edge	t_{28}	SR	8	–	–	ns	–
Data hold from CLKOUT falling edge	t_{29}	SR	2	–	–	ns	–

1) Not subject to production test, verified by design/characterization.

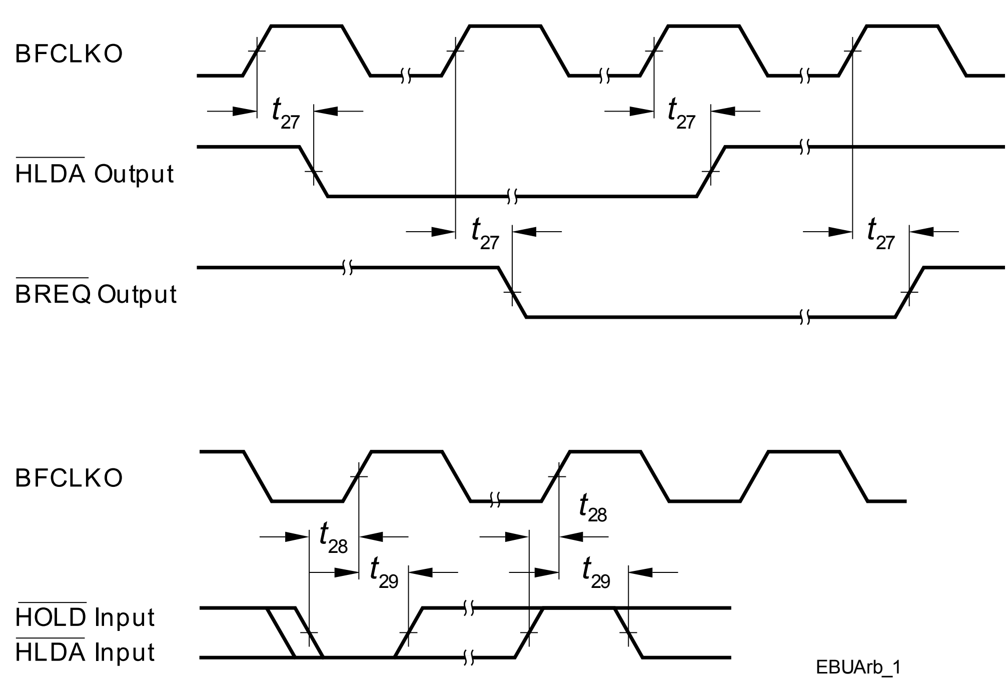

Figure 41 EBU Arbitration Signal Timing

4.3.12 Peripheral Timings

Note: Peripheral timing parameters are not subject to production test. They are verified by design/characterization.

4.3.12.1 Micro Link Interface (MLI) Timing

Table 32 MLI Timing Parameters (Operating Conditions apply), C_L = 50 pF

Parameter	Symbol		Values			Unit	Note / Test Con dition
			Min.	Typ.	Max.		
TCLK clock period[1)2)]	t_{30}	CC	2[3)]	–	–	1 / f_{SYS}	–
RCLK clock period	t_{31}	SR	1	–	–	1 / f_{SYS}	–
MLI outputs delay from TCLK rising edge	t_{35}	CC	0	–	8	ns	–
MLI inputs setup to RCLK falling edge	t_{36}	SR	4	–	–	ns	–
MLI inputs hold to RCLK falling edge	t_{37}	SR	4	–	–	ns	–
RREADY output delay from RCLK falling edge	t_{38}	CC	0	–	8	ns	–

1) TCLK signal rise/fall times are the same as the A2 Pads rise/fall times.

2) TCLK high and low times can be minimum 1 × T_{MLI}.

3) When f_{SYS} = 75 MHz, t_{30} = 26,67ns