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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z51f3220skx

2. Block Diagram

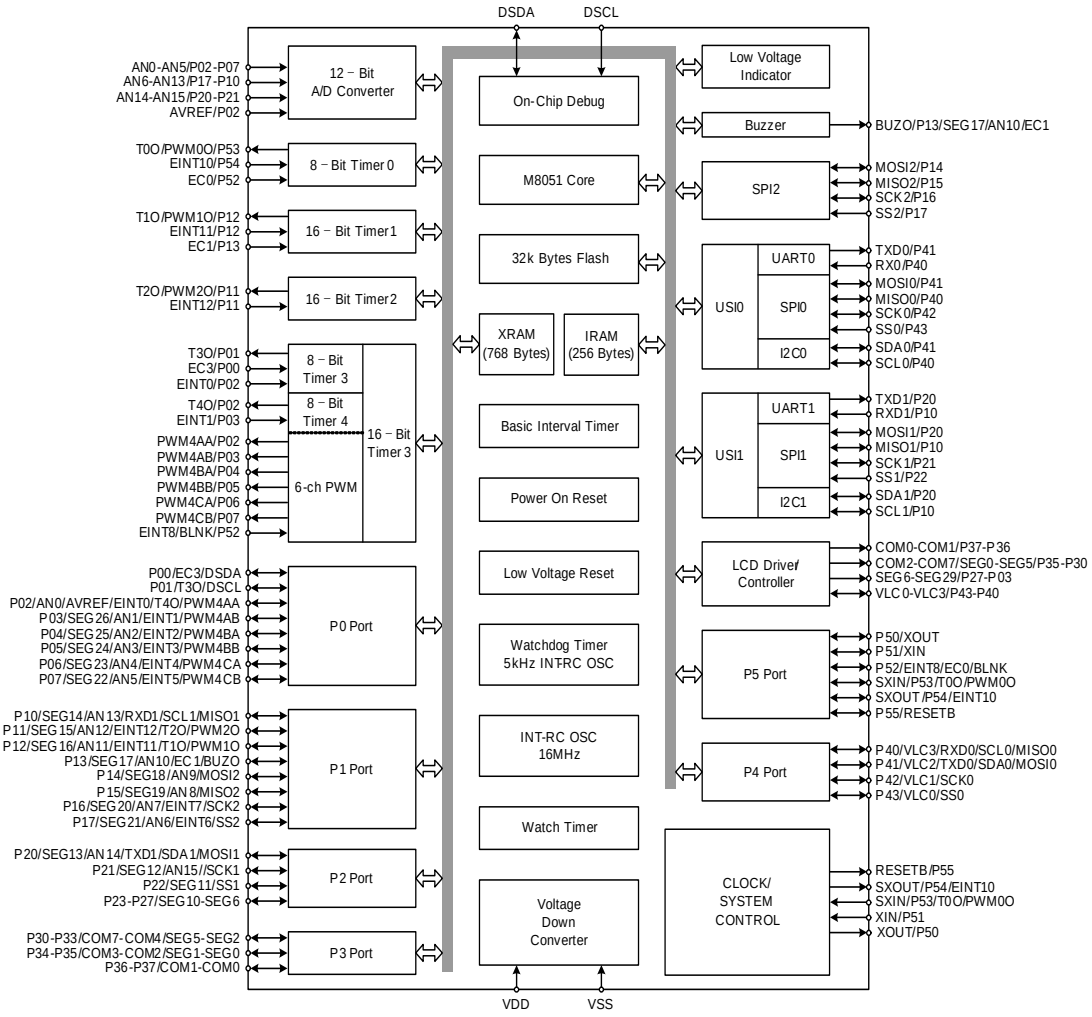


Figure 2.1 Block Diagram

NOTE) The P14–P17, P23–P25, P34–P37, and P43 are not in the 32-pin package.

6. Port Structures

6.1 General Purpose I/O Port

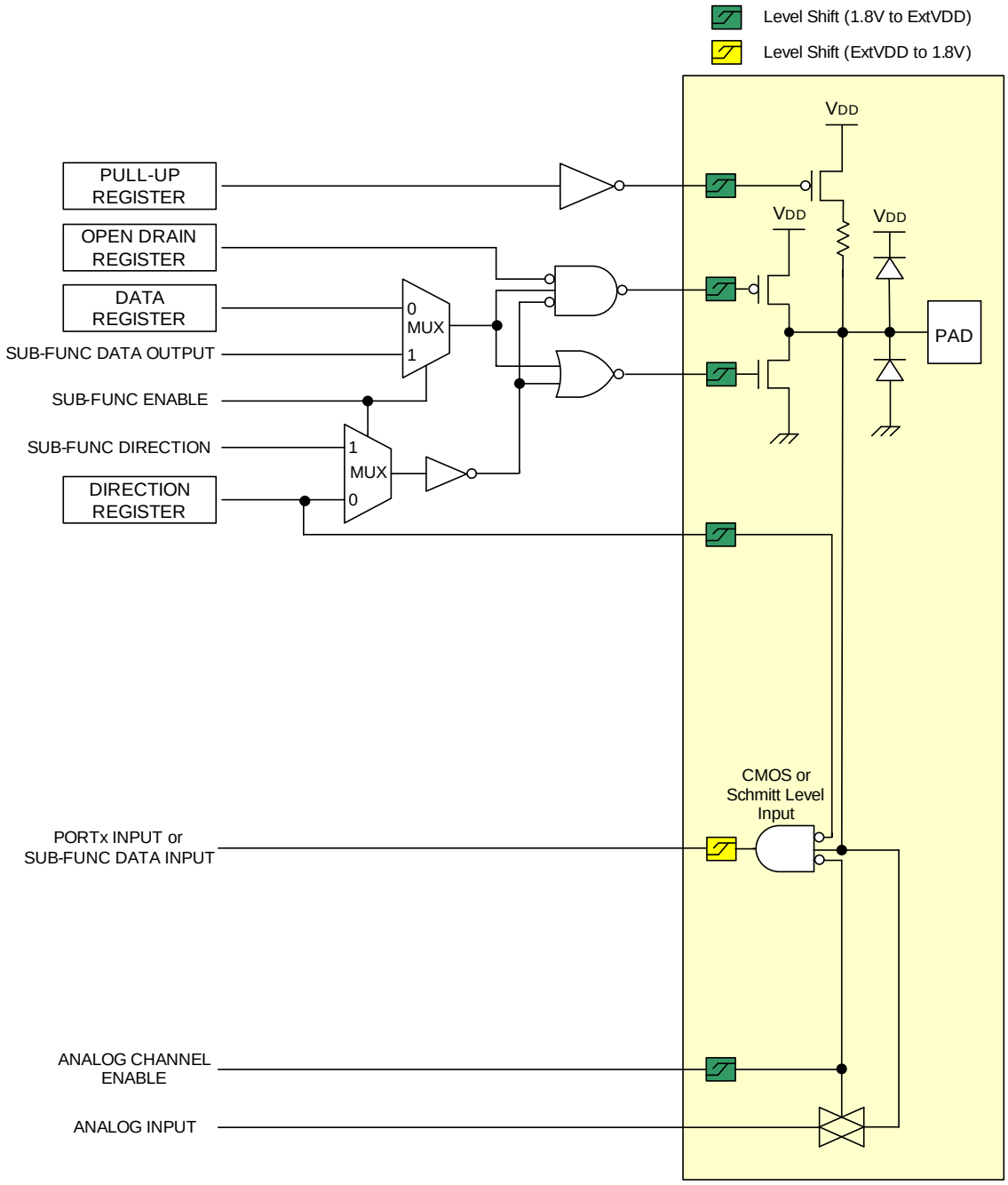


Figure 6.1 General Purpose I/O Port

8.4.2 SFR Map

Table 8-3 SFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
80H	P0 Data Register	P0	R/W	0	0	0	0	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0
84H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0
85H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0
86H	Low Voltage Indicator Control Register	LVICR	R/W	–	–	0	0	0	0	0	0
87H	Power Control Register	PCON	R/W	0	–	–	–	0	0	0	0
88H	P1 Data Register	P1	R/W	0	0	0	0	0	0	0	0
89H	Watch Timer Data Register	WTDR	W	0	1	1	1	1	1	1	1
	Watch Timer Counter Register	WTCNT	R	–	0	0	0	0	0	0	0
8AH	System and Clock Control Register	SCCR	R/W	–	–	–	–	–	–	0	0
8BH	Basic Interval Timer Control Register	BITCR	R/W	0	0	0	–	0	0	0	1
8CH	Basic Interval Timer Counter Register	BITCNT	R	0	0	0	0	0	0	0	0
8DH	Watch Dog Timer Control Register	WDTCR	R/W	0	0	0	–	–	–	0	0
8EH	Watch Dog Timer Data Register	WDTDR	W	1	1	1	1	1	1	1	1
	Watch Dog Timer Counter Register	WDTCNT	R	0	0	0	0	0	0	0	0
8FH	BUZZER Data Register	BUZDR	R/W	1	1	1	1	1	1	1	1
90H	P2 Data Register	P2	R/W	0	0	0	0	0	0	0	0
91H	P0 Open-drain Selection Register	P0OD	R/W	0	0	0	0	0	0	0	0
92H	P1 Open-drain Selection Register	P1OD	R/W	0	0	0	0	0	0	0	0
93H	P2 Open-drain Selection Register	P2OD	R/W	0	0	0	0	0	0	0	0
94H	P4 Open-drain Selection Register	P4OD	R/W	–	–	–	–	0	0	0	0
95H	P5 Pull-up Resistor Selection Register	P5PU	R/W	–	–	0	0	0	0	0	0
96H	Watch Timer Control Register	WTCR	R/W	0	–	–	0	0	0	0	0
97H	BUZZER Control Register	BUZCR	R/W	–	–	–	–	–	0	0	0
98H	P3 Data Register	P3	R/W	0	0	0	0	0	0	0	0
99H	LCD Driver Control Low Register	LCDCRL	R/W	–	–	0	0	0	0	0	0
9AH	LCD Driver Control High Register	LCDCRH	R/W	–	–	–	0	–	–	0	0
9BH	LCD Contrast Control register	LCDCCR	R/W	0	–	–	–	0	0	0	0
9CH	A/D Converter Control Low Register	ADCCRL	R/W	0	0	0	0	0	0	0	0
9DH	A/D Converter Control High Register	ADCCRH	R/W	0	–	0	0	0	0	0	0
9EH	A/D Converter Data Low Register	ADCDRL	R	x	x	x	x	x	x	x	x
9FH	A/D Converter Data High Register	ADCDRH	R	x	x	x	x	x	x	x	x

11.8 Timer 3, 4

11.8.1 Overview

Timer 3 and timer 4 can be used either two 8-bit timer/counter or one 16-bit timer/counter with combine them. Each 8-bit timer/event counter module has multiplexer, comparator, 8-bit timer data register, 8-bit counter register, control register and capture data register (T3CNT, T3DR, T3CAPR, T3CR, T4CNT, T4DR, T4CAPR, T4CR). For PWM, it has PWM register (T4PPRL. T4PPRH, T4ADRL, T4ADRH, T4BDRL, T4BDRH, T4CDRL, T4CDRH, T4DLYA, T4DLYB, T4DLYC).

It has five operating modes:

- 8-bit timer/counter mode
- 8-bit capture mode
- 16-bit timer/counter mode
- 16-bit capture mode
- 10-bit PWM mode

The timer/counter 3 and 4 can be clocked by an internal or an external clock source (EC3). The clock source is selected by clock selection logic which is controlled by the clock selection bits (T3CK[2:0], T4CK[3:0]). Also the timer/counter 4 can use more clock sources than timer/counter 3.

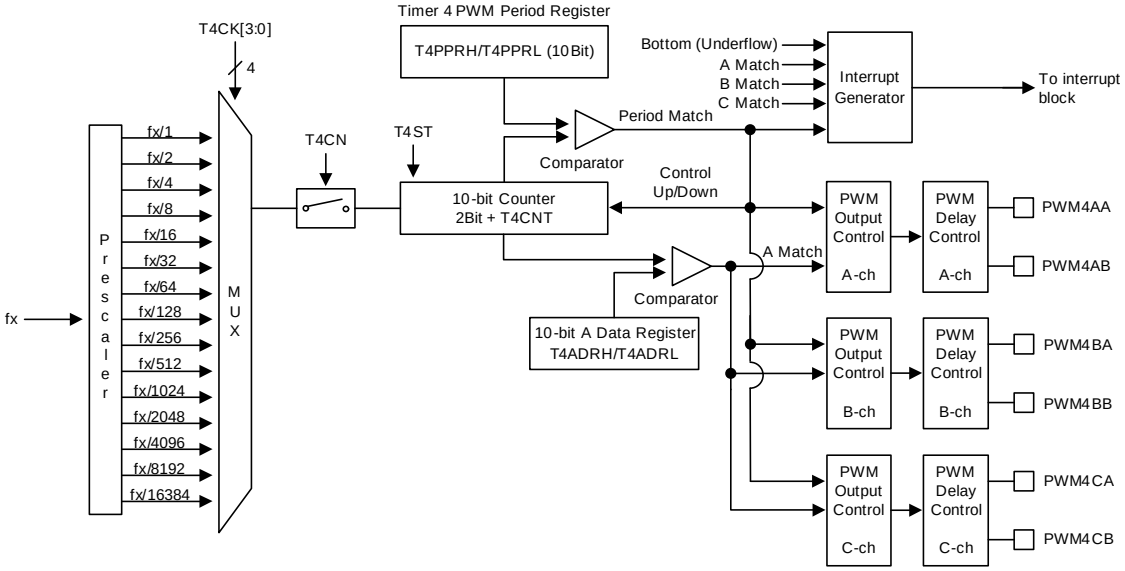
- TIMER 3 clock source: $f_X/2$, 4, 8, 32, 128, 512, 2048 and EC3
- TIMER 4 clock source: $f_X/1$, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384 and T3 clock

In the capture mode, by EINT0/EINT1, the data is captured into input capture data register (T3CAPR, T4CAPR).
In 8-bit timer/counter 3/4 mode, whenever counter value is equal to T3DR/T4DR, T3O/T4O port toggles. Also In 16-bit timer/counter 3 mode,
The timer 3 outputs the comparison result between counter and data register through T3O port. The PWM wave form to PWMAA, PWMAB, PWMBA, PWMBB, PWMCA, PWMCB Port (6-channel) in the PWM mode.

Table 11-11 Timer 3, 4 Operating Modes

16BIT	T3MS	T4MS	PWM4E	T3CK[2:0]	T4CK[3:0]	Timer 3	Timer 4
0	0	0	0	XXX	XXXX	8 Bit Timer/Counter Mode	8 Bit Timer/Counter Mode
0	1	1	0	XXX	XXXX	8 Bit Capture Mode	8 Bit Capture Mode
1	0	0	0	XXX	XXXX	16 Bit Tmer/Counter Mode	
1	1	1	0	XXX	XXXX	16 Bit Capture Mode	
0	X	X	1	XXX	XXXX	10 Bit PWM Mode	

T4CR	16BIT	T4MS	T4CN	T4ST	T4CK3	T4CK2	T4CK1	T4CK0	ADDRESS:1002H (ESFR) INITIAL VALUE: 0000_0000B
	0	X	X	X	X	X	X	X	
T4PCR1	PWM4E	ESYNC	BMOD	PHLT	UPDT	UALL	NOPS1	NOPS0	ADDRESS:1003H (ESFR) INITIAL VALUE: 0000_0000B
	1	X	X	X	X	X	X	X	
T4PCR2	FORCA	–	PAAOE	PABOE	PBAOE	PBBOE	PCAOE	PCBOE	ADDRESS:1004H (ESFR) INITIAL VALUE: 0000_0000B
	1	–	X	X	X	X	X	X	
T4PCR3	HZCLR	POLBO	POLAA	POLAB	POLBA	POLBB	POLCA	POLCB	ADDRESS:1005H (ESFR) INITIAL VALUE: 0000_0000B
	X	X	X	X	X	X	X	X	



NOTE: Do not set to “1111b” in the T4CK[3:0], when two 8-bit timer 3/4 modes.

Figure 11.35 10-Bit PWM Mode (Force All-ch)

T4PCR1 (Timer 4 PWM Control Register 1) : 1003H (ESFR)

7	6	5	4	3	2	1	0
PWM4E	ESYNC	BMOD	PHLT	UPDT	UALL	NOPS1	NOPS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

PWM4E Control Timer 4 Mode

0 Select timer/counter or capture mode of Timer 4

1 Select 10-bit PWM mode of Timer 4

ESYNC Select the Operation of External Sync with the BLNK pin

0 Disable external sync operation

1 Enable external sync operation
(The all PWM4xA/PWM4xB pins are high-impedance outputs on rising edge of the BLNK input pin. Where x= A, B and C)

BMOD Control Back-to-Back Mode Operation

0 Disable back-to-back mode (up count only)

1 Enable back-to-back mode (up/down count only)

PHLT Control Timer 4 PWM Operation

0 Run 10-bit PWM

1 Stop 10-bit PWM (counter hold and output disable)

UPDT Select the Update Timer of T4PPR/T4ADR/T4BDR/T4CDR

0 Update at period match of T4CNT and T4PPR

1 Update at any time when written

UALL Control Update All Duty Registers (T4ADR/T4BDR/T4CDR)

0 Write a duty register separately

1 Wrtie all duty registers via Timer 4 PWM A dury register (T4ADR)

NOPS[1:0] Select on-Overlap Prescaler

NOPS1	NOPS0	Description
0	0	$f_{PWM}/1$
0	1	$f_{PWM}/2$
1	0	$f_{PWM}/4$
1	1	$f_{PWM}/8$

NOTE) Where the f_{PWM} is the clock frequency of the Timer 4 PWM.

The process for detecting stop bit is like clock and data recovery process. That is, if 2 or more samples of 3 center values have high level, correct stop bit is detected, else a frame error (FE0) flag is set. After deciding whether the first stop bit is valid or not, the Receiver goes to idle state and monitors the RXD0 line to check a valid high to low transition is detected (start bit detection).

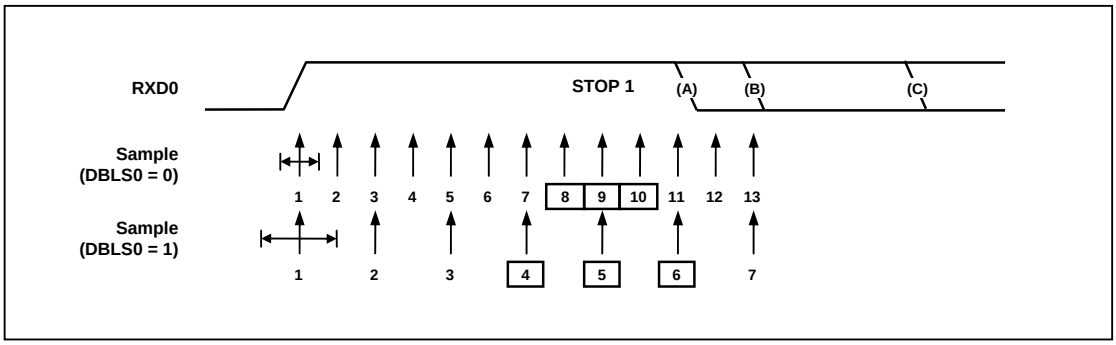


Figure 11.63 Stop Bit Sampling and Next Start Bit Sampling (USI0)

11.13.4 USI1 Clock Generation

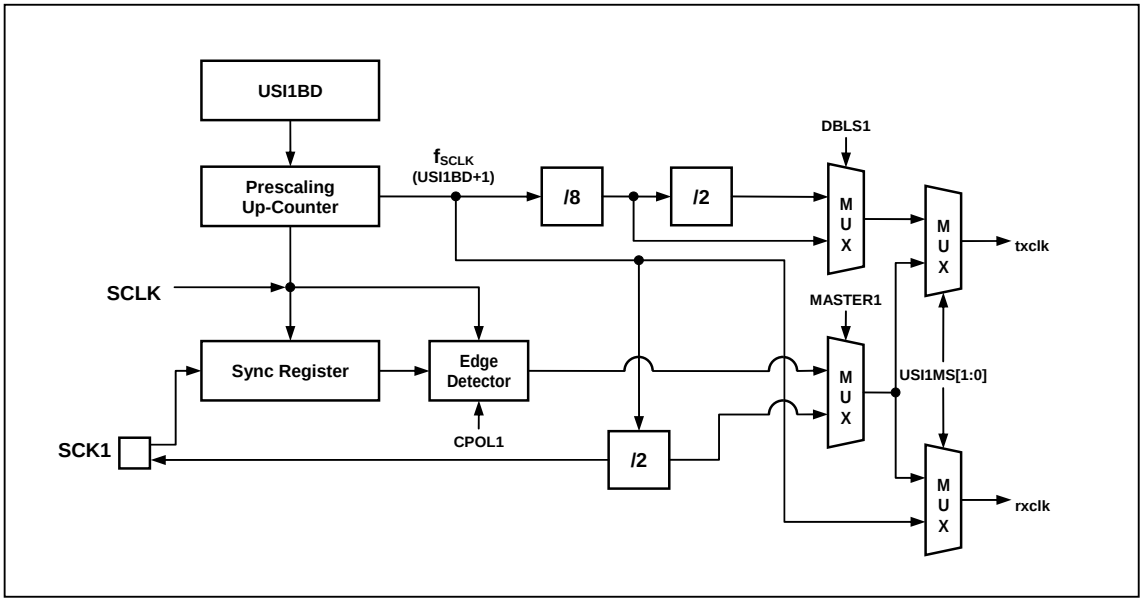


Figure 11.79 Clock Generation Block Diagram (USI1)

The clock generation logic generates the base clock for the transmitter and receiver. The USI1 supports four modes of clock operation and those are normal asynchronous, double speed asynchronous, master synchronous and slave synchronous mode. The clock generation scheme for master SPI and slave SPI mode is the same as master synchronous and slave synchronous operation mode. The USI1MS[1:0] bits in USI1CR1 register selects asynchronous or synchronous operation. Asynchronous double speed mode is controlled by the DBLS1 bit in the USI1CR2 register. The MASTER1 bit in USI1CR3 register controls whether the clock source is internal (master mode, output pin) or external (slave mode, input pin). The SCK1 pin is active only when the USI1 operates in synchronous or SPI mode.

Following table shows the equations for calculating the baud rate (in bps).

Table 11-22 Equations for Calculating USI1 Baud Rate Register Setting

Operating Mode	Equation for Calculating Baud Rate
Asynchronous Normal Mode (DBLS1=0)	$\text{Baud Rate} = \frac{\text{fx}}{16(\text{USI1BD}+1)}$
Asynchronous Double Speed Mode (DBLS1=1)	$\text{Baud Rate} = \frac{\text{fx}}{8(\text{USI1BD}+1)}$
Synchronous or SPI Master Mode	$\text{Baud Rate} = \frac{\text{fx}}{2(\text{USI1BD}+1)}$

11.13.7 USI1 UART Data format

A serial frame is defined to be one character of data bits with synchronization bits (start and stop bits), and optionally a parity bit for error detection.

The UART supports all 30 combinations of the following as valid frame formats.

- 1 start bit
- 5, 6, 7, 8 or 9 data bits
- no, even or odd parity bit
- 1 or 2 stop bits

A frame starts with the start bit followed by the least significant data bit (LSB). Then the next data bits, up to nine, are succeeding, ending with the most significant bit (MSB). If parity function is enabled, the parity bit is inserted between the last data bit and the stop bit. A high-to-low transition on data pin is considered as start bit. When a complete frame is transmitted, it can be directly followed by a new frame, or the communication line can be set to an idle state. The idle means high state of data pin. The following figure shows the possible combinations of the frame formats. Bits inside brackets are optional.

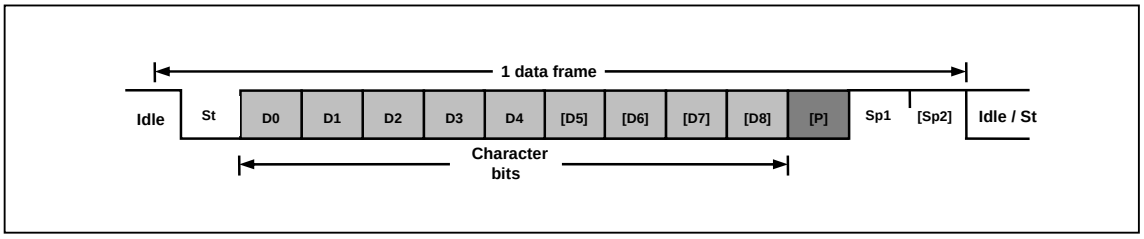


Figure 11.81 Frame Format (USI1)

1 data frame consists of the following bits

- Idle No communication on communication line (TXD0/RXD0)
- St Start bit (Low)
- Dn Data bits (0~8)
- Parity bit ---------- Even parity, Odd parity, No parity
- Stop bit(s) ---------- 1 bit or 2 bits

The frame format used by the UART is set by the USI1S[2:0], USI1PM[1:0] bits in USI1CR1 register and USI1SB bit in USI1CR3 register. The Transmitter and Receiver use the same setting.

11.13.8 USI1 UART Parity bit

The parity bit is calculated by doing an exclusive-OR of all the data bits. If odd parity is used, the result of the exclusive-O is inverted. The parity bit is located between the MSB and first stop bit of a serial frame.

$P_{even} = D_{n-1} \wedge \ldots \wedge D_3 \wedge D_2 \wedge D_1 \wedge D_0 \wedge 0$

$P_{odd} = D_{n-1} \wedge \ldots \wedge D_3 \wedge D_2 \wedge D_1 \wedge D_0 \wedge 1$

P_{even} : Parity bit using even parity

P_{odd} : Parity bit using odd parity

D_n : Data bit n of the character

USI1CR1 (USI1 Control Register 1: For UART, SPI, and I2C mode) : E9H

7	6	5	4	3	2	1	0
USI1MS1	USI1MS0	USI1PM1	USI1PM0	USI1S2	USI1S1 ORD1	USI1S0 CPHA1	CPOL1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

USI1MS[1:0] Selects operation mode of USI1

USI1MS1	USI1MS0	Operation mode
0	0	Asynchronous Mode (UART)
0	1	Synchronous Mode
1	0	I2C mode
1	1	SPI mode

USI1PM[1:0] Selects parity generation and check methods (only UART mode)

USI1PM1	USI1PM0	Parity
0	0	No Parity
0	1	Reserved
1	0	Even Parity
1	1	Odd Parity

USI1S[2:0] When in asynchronous or synchronous mode of operation, selects the length of data bits in frame

USI1S2	USI1S1	USI1S0	Data Length
0	0	0	5 bit
0	0	1	6 bit
0	1	0	7 bit
0	1	1	8 bit
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	9 bit

ORD1 This bit in the same bit position with USI1S1. The MSB of the data byte is transmitted first when set to '1' and the LSB when set to '0' (onl SPI mode)

0	LSB-first
1	MSB-first

CPOL1 This bit determines the clock polarity of ACK in synchronous or SPI mode.

0	TXD change@Rising Edge, RXD change@Falling Edge
1	TXD change@Falling Edge, RXD change@Rising Edge

CPHA1 This bit is in the same bit position with USI1S0. This bit determines if data are sampled on the leading or trailing edge of SCK1 (only SPI mode).

CPOL1	CPHA1	Leading edge	Trailing edge
0	0	Sample (Rising)	Setup (Falling)
0	1	Setup (Rising)	Sample (Falling)
1	0	Sample (Falling)	Setup (Rising)
1	1	Setup (Falling)	Sample (Rising)

USI1CR3 (USI1 Control Register 3: For UART, SPI, and I2C mode) : EBH

7	6	5	4	3	2	1	0
MASTER1	LOOPS1	DISSCK1	USI1SSEN	FXCH1	USI1SB	USI1TX8	USI1RX8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Initial value : 00H

MASTER1 Selects master or slave in SPI and synchronous mode operation and controls the direction of SCK1 pin

0 Slave mode operation (External clock for SCK1).

1 Master mode operation(Internal clock for SCK1).

LOOPS1 Controls the loop back mode of USI1 for test mode (only UART and SPI mode)

0 Normal operation

1 Loop Back mode

DISSCK1 In synchronous mode of operation, selects the waveform of SCK1 output

0 ACK is free-running while UART is enabled in synchronous master mode

1 ACK is active while any frame is on transferring

USI1SSEN This bit controls the SS1 pin operation (only SPI mode)

0 Disable

1 Enable (The SS1 pin should be a normal input)

FXCH1 SPI port function exchange control bit (only SPI mode)

0 No effect

1 Exchange MOSI1 and MISO1 function

USI1SB Selects the length of stop bit in asynchronous or synchronous mode of operation.

0 1 Stop Bit

1 2 Stop Bit

USI1TX8 The ninth bit of data frame in asynchronous or synchronous mode of operation. Write this bit first before loading the USI1DR register

0 MSB (9^{th} bit) to be transmitted is '0'

1 MSB (9^{th} bit) to be transmitted is '1'

USI1RX8 The ninth bit of data frame in asynchronous or synchronous mode of operation. Read this bit first before reading the receive buffer (only UART mode).

0 MSB (9^{th} bit) received is '0'

1 MSB (9^{th} bit) received is '1'

11.15 LCD Driver

11.15.1 Overview

The LCD driver is controlled by the LCD Control Register (LCDCRH/L). The LCLK[1:0] determines the frequency of COM signal scanning of each segment output. A RESET clears the LCD control register LCDCRH and LCDCRL values to logic ‘0’.

The LCD display can continue operating during IDLE and STOP modes if a sub-frequency clock is used as system clock source.

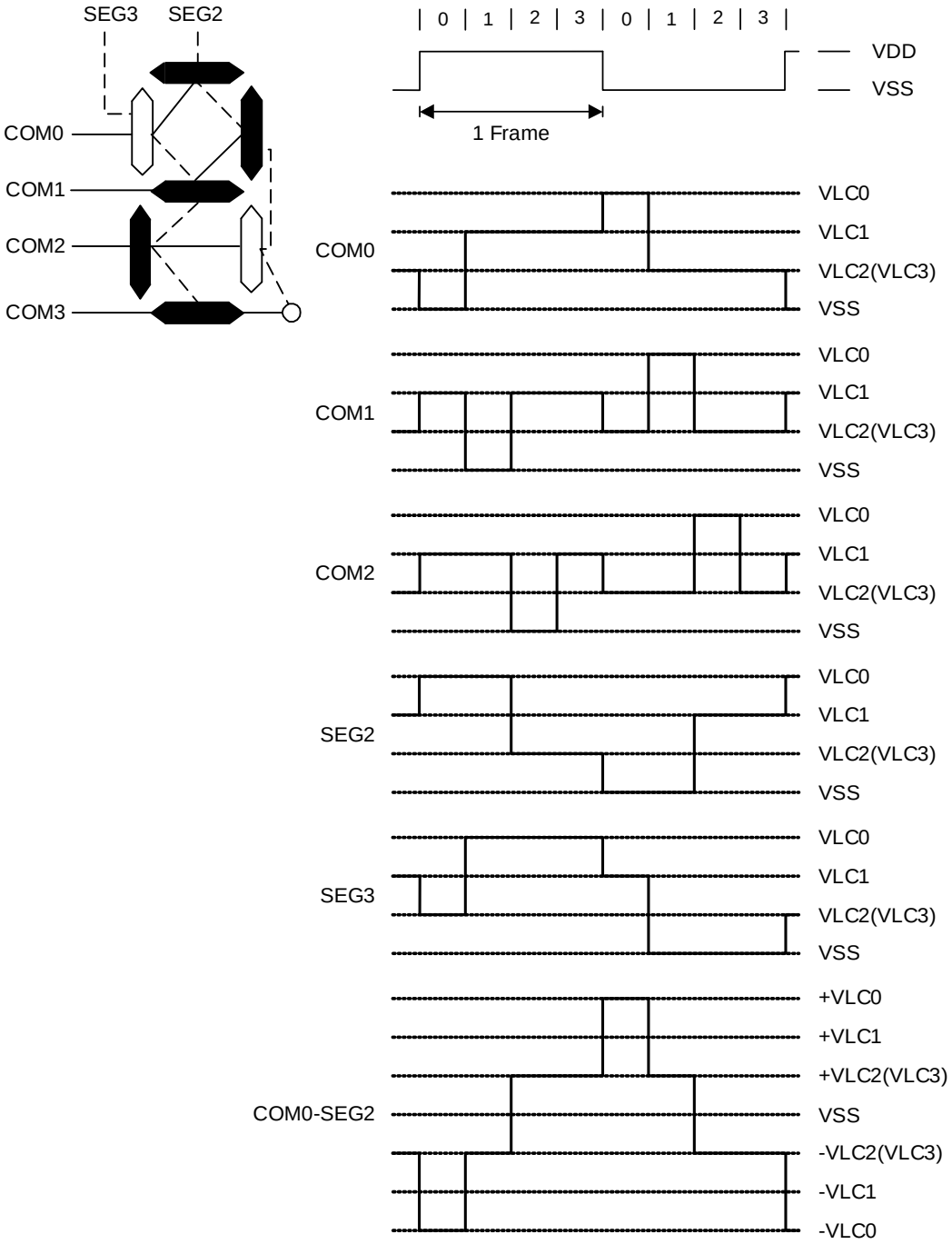
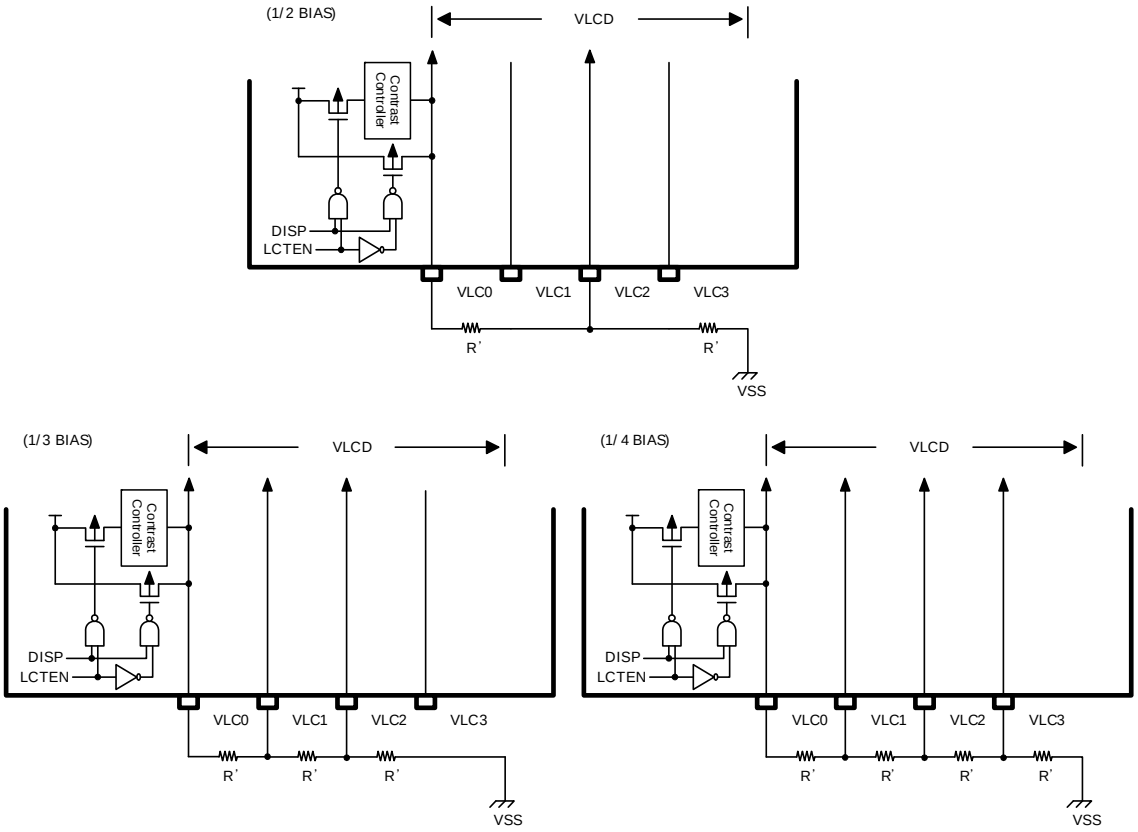


Figure 11.102 LCD Signal Waveforms (1/4Duty, 1/3Bias)



NOTES)

1. When the external resistor bias is selected, the internal resistors for bias are disconnected.
2. When the external resistor bias is selected, the dividing resistors should be connected like the above figure and the needed bias pins should be selected as the LCD bias function pins (VLC0, VLC1, VLC2, and VLC3) by P4FSR register.

- When it is 1/2 bias, the P43/VLC0 and P41/VLC2 pins should be selected as VLC0 and VLC2 functions. The other pins can be used for normal I/O.
- When it is 1/3 bias, the P43/VLC0, P42/VLC1, and P41/VLC2 pins should be selected as VLC0, VLC1, and VLC2 functions. Another pin can be used for normal I/O.
- When it is 1/4 bias, the P43/VLC0, P42/VLC1, P41/VLC2, and P40/VLC3 pins should be selected as VLC0, VLC1, VLC2, and VLC3 functions

Figure 11.105 External Resistor Bias Connection

13. RESET

13.1 Overview

The following is the hardware setting value.

Table 13-1 Reset State

On Chip Hardware	Initial Value
Program Counter (PC)	0000h
Accumulator	00h
Stack Pointer (SP)	07h
Peripheral Clock	On
Control Register	Refer to the Peripheral Registers

13.2 Reset Source

The Z51F3220 has five types of reset sources. The following is the reset sources.

- External RESETB
- Power ON RESET (POR)
- WDT Overflow Reset (In the case of WDTEN = `1`)
- Low Voltage Reset (In the case of LVREN = `0 `)
- OCD Reset

13.3 RESET Block Diagram

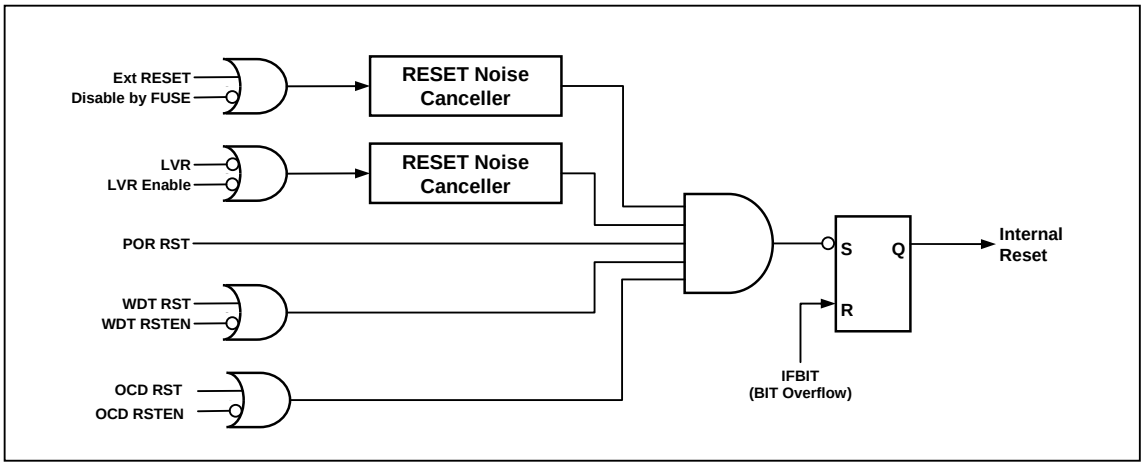


Figure 13.1 RESET Block Diagram

14.2.3 Connection of Transmission

Two-pin interface connection uses open-drain (wire-AND bidirectional I/O).

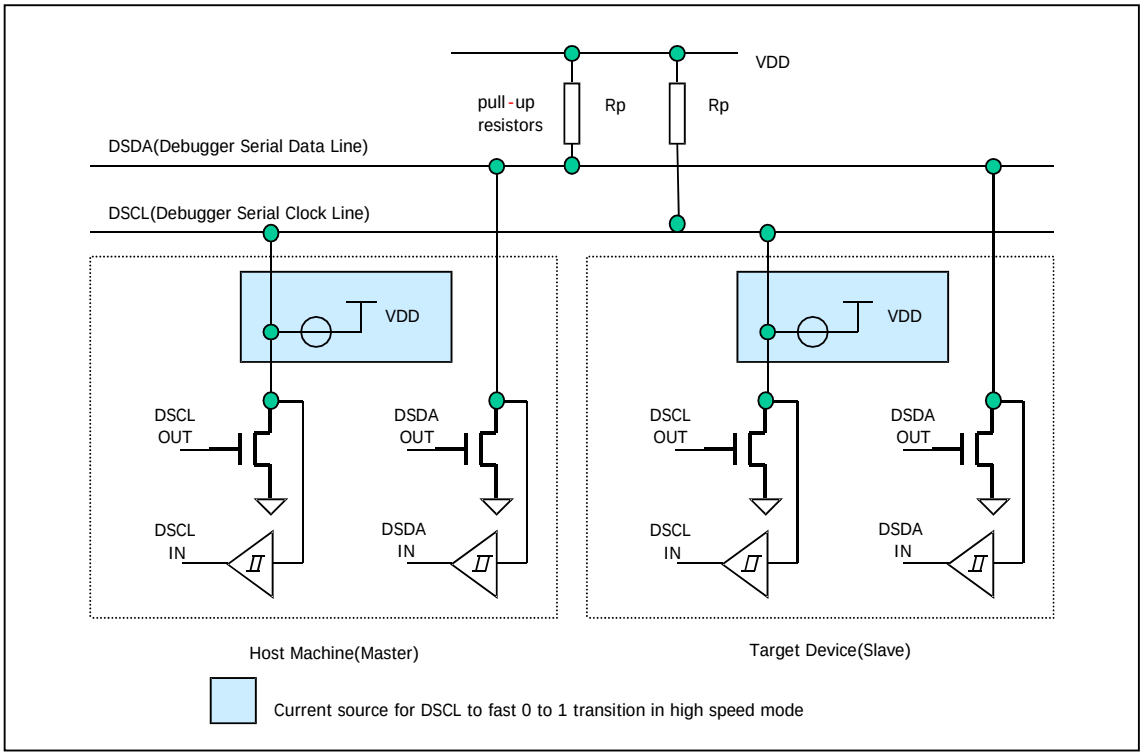


Figure 14.8 Connection of Transmission

16. Configure Option

16.1 Configure Option Control

The data for configure option should be written in the configure option area (003EH – 003FH) by programmer (Writer tools).

CONFIGURE OPTION 1 : ROM Address 003FH

7	6	5	4	3	2	1	0
R_P	HL	–	–	–	–	–	RSTS

Initial value : 00H

R_P Read Protection
- 0 Disable “Read protection”
- 1 Enable “Read protection”

HL Hard-Lock
- 0 Disable “Hard-lock”
- 1 Enable “Hard-lock”

RSTS RESETB Select
- 0 P55 port
- 1 RESETB port with a pull-up resistor

CONFIGURE OPTION 2: ROM Address 003EH

7	6	5	4	3	2	1	0
–	–	–	–	–	PAEN	PASS1	PASS0

Initial value : 00H

PAEN Protection Area Enable/Disable
- 0 Disable Protection (Erasable by instruction)
- 1 Enable Protection (Not erasable by instruction)

PASS [1:0] Protection Area Size Select

PASS1	PASS0	Description
0	0	3.8k Bytes (Address 0100H – 0FFFH)
0	1	1.7k Bytes (Address 0100H – 07FFH)
1	0	768 Bytes (Address 0100H – 03FFH)
1	1	256 Bytes (Address 0100H – 01FFH)

- If you use input bit port for compare jump instruction, you have to copy the input port as internal paramet er or carry bit and then use compare jump instruction.

```
bit tt;
while(1){
  tt=P00;
  if (tt==0){ P10=1;}
  else {P10=0;}
  P11^=1;
}
```

```
zzz:  MOV   C,080.0     ; input port use internal parameter
      MOV   020.0, C    ; move
      JB    020.0, xxx  ; compare
      SETB  088.0
      SJMP  yyy
xxx:  CLR   088.0
yyy:  MOV   C,088.1
      CPL   C
      MOV   088.1,C
      SJMP  zzz
```