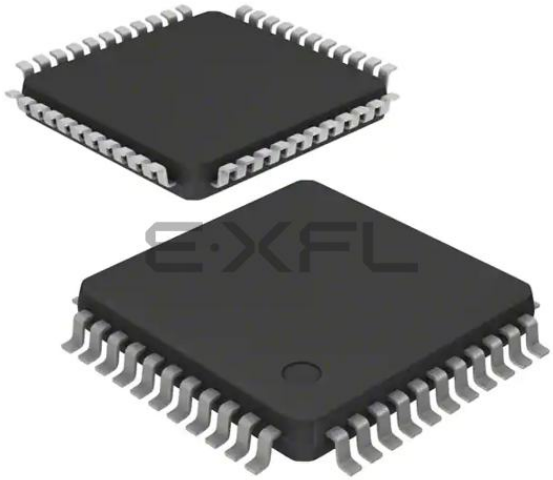

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e6116asg

Table of Contents

List of Tables

- Auto Latches
- High-voltage protection on high-voltage inputs
- RAM and EPROM Protect
- EPROM:
  - 16KB Z86E61
  - 32KB Z86E63

- 256-byte Register File:
  - 236 bytes of General-Purpose RAM
  - 16 bytes of Control and Status registers
  - 4 bytes for ports

- Two programmable 8-bit Counter/Timers, each with 6-bit programmable prescaler
- Six vectored priority interrupts from eight different sources
- On-chip oscillator that accepts a crystal ceramic resonator, LC or external clock drive

To unburden the system from coping with real-time tasks such as counting/timing and serial data communication, the Z86E61/Z86E63 MCU offers two on-chip counter/timers with a large number of user selectable modes. See the block diagram in Figure 1.

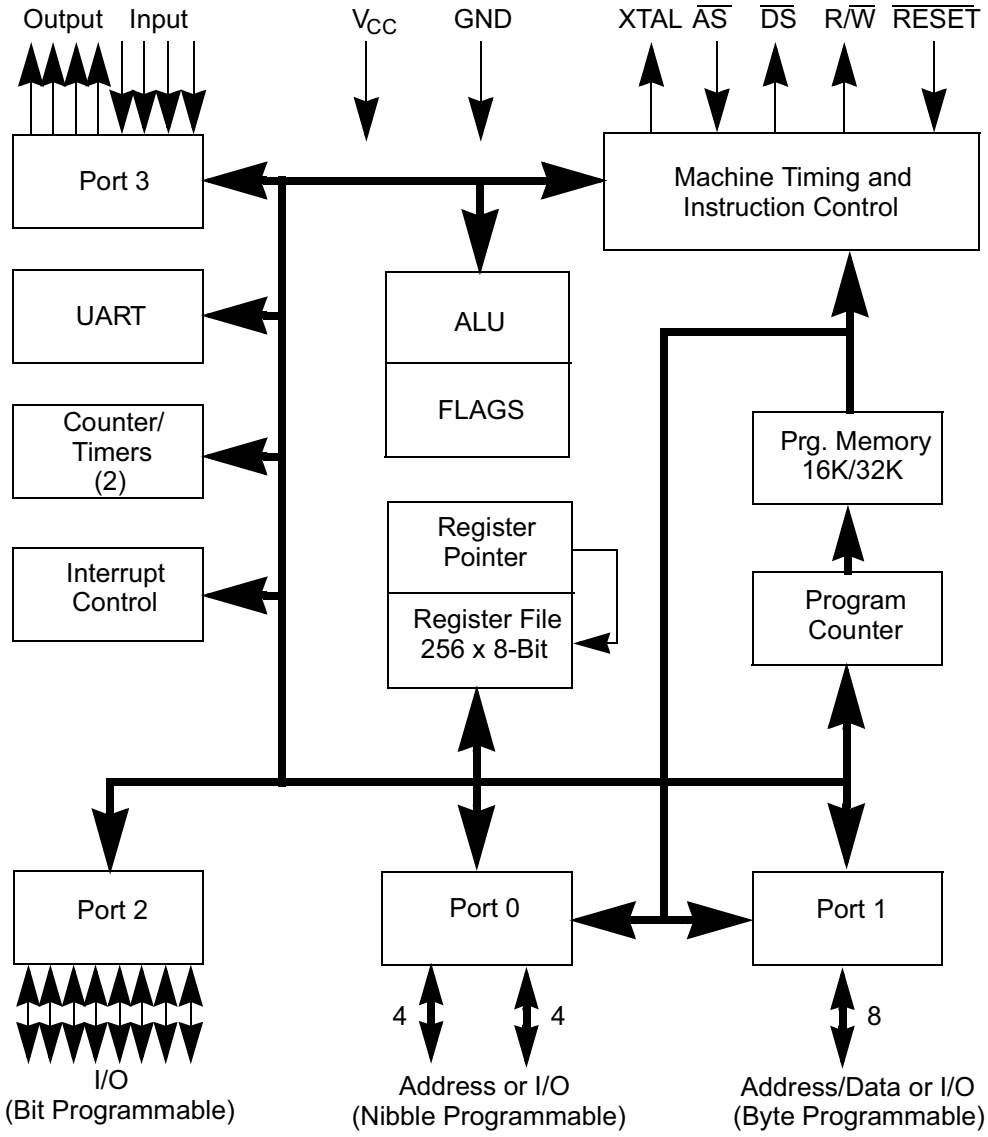


Figure 1. Z86E61/Z86E63 MCU Functional Block Diagram

Power connections follow the conventional descriptions listed in Table 24.

Table 24. Power Connection Conventions

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Figure 4 shows the pin-outs for the 44-pin LQFP Standard Mode package; Table 27 describes each pin.

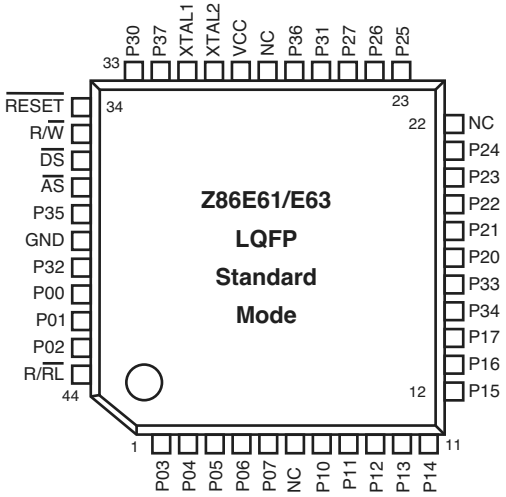


Figure 4. Z86E61/Z86E63 LQFP Pin Diagram, Standard Mode

Table 27. Z86E61/Z86E63 LQFP Pin Description, Standard Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{RESET}}$	Reset	Input
R/$\overline{\text{W}}$	Read/Write	Output
$\overline{\text{DS}}$	Data Strobe	Output
$\overline{\text{AS}}$	Address Strobe	Output
P00–P07 Port 0	8-bit General I/O	Input/Output
P10–P17 Port 1	8-bit General I/O	Input/Output
P20–P27 Port 2	8-bit General I/O	Input/Output
P30–P33 Port 3	4-bit Input	Input
P34–P37 Port 3	4-bit Output	Output
R/$\overline{\text{RL}}$	ROM/ROMless Control	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Pin Descriptions

This section describes the major Z86E61/Z86E63 MCU pin signals and ports.

ROMless (Input, Active Low)

Connecting this pin to GND disables the internal ROM and forces the device to function as a Z86C91 ROMless Z8 (see the Z86C91 product specification for more information). When pulled High to V_{CC}, the device functions as a normal Z86E61/Z86E63 EPROM version. This pin is only available on the 44-pin versions of the Z86E61/Z86E63 MCU.

DS (Output, Active Low)

Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of DS. For WRITE operations, the falling edge of DS indicates that output data is valid.

AS (Output, Active Low)

Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of AS. Under program control, AS can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL2, XTAL1

Crystal 2, Crystal 1 (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R/W (Output, Write Low)

The Read/Write signal is Low when the MCU is writing to the external program or data memory.

RESET (Input, Active Low)

To avoid asynchronous and noisy reset problems, the Z86E61/Z86E63 MCU is equipped with a reset filter of four external clocks (4TpC). If the external RESET signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external RESET, whichever is longer. During the reset cycle, DS is held active Low while AS cycles at a rate of TpC/2. When RESET is deactivated, program execution begins at location `000Ch`. Power-up reset time must be held low for 50 ms, or until V_{CC} is stable, whichever is longer.

open-drain output. Port 2 is always available for I/ 0 operation. When used as an I/0 port, Port 2 can be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines DAV2 and RDY2. The handshake signal assignment for Port 3 lines, P31 and P36, is dictated by the direction (input or output) assigned to P27; see Figure 10 and Table 31 on page 16).

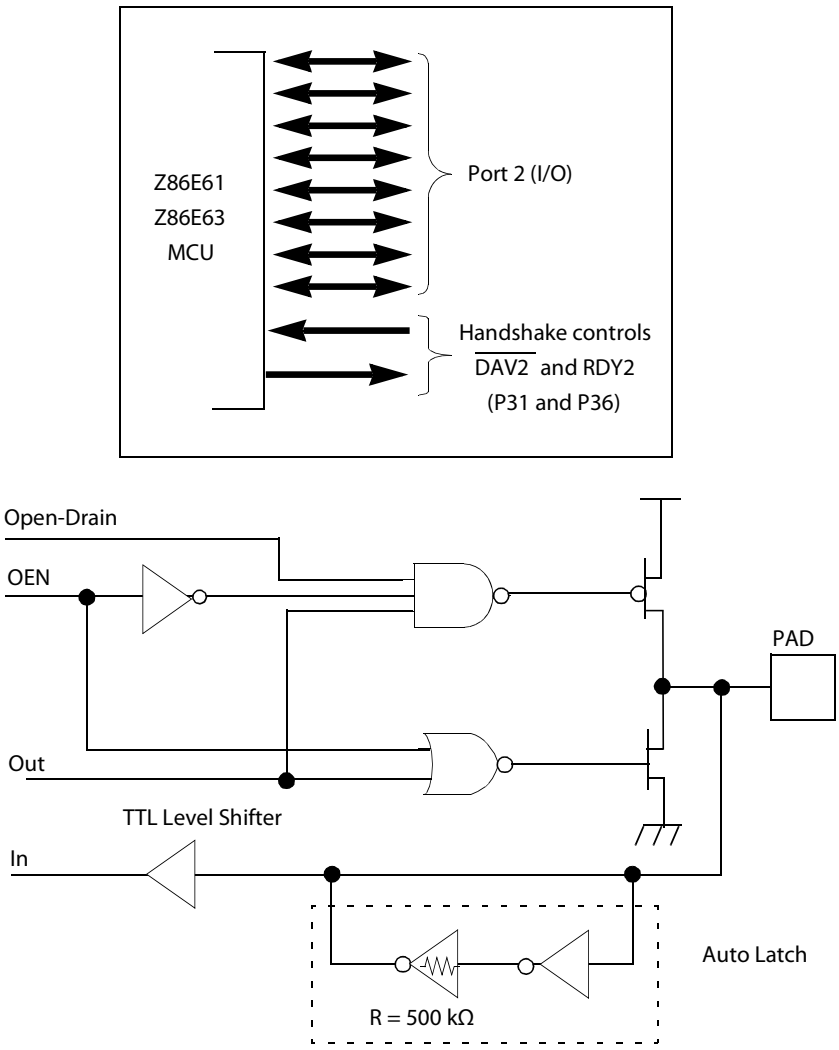


Figure 10. Port 2 Configuration

UART Operation. Port 3 lines, P37 and P30, are programmed as serial I/0 lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/ Timer0.

The Z86E61/Z86E63 MCU automatically adds a start bit and two stop bits to transmitted data; see Figure 12. Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits, and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

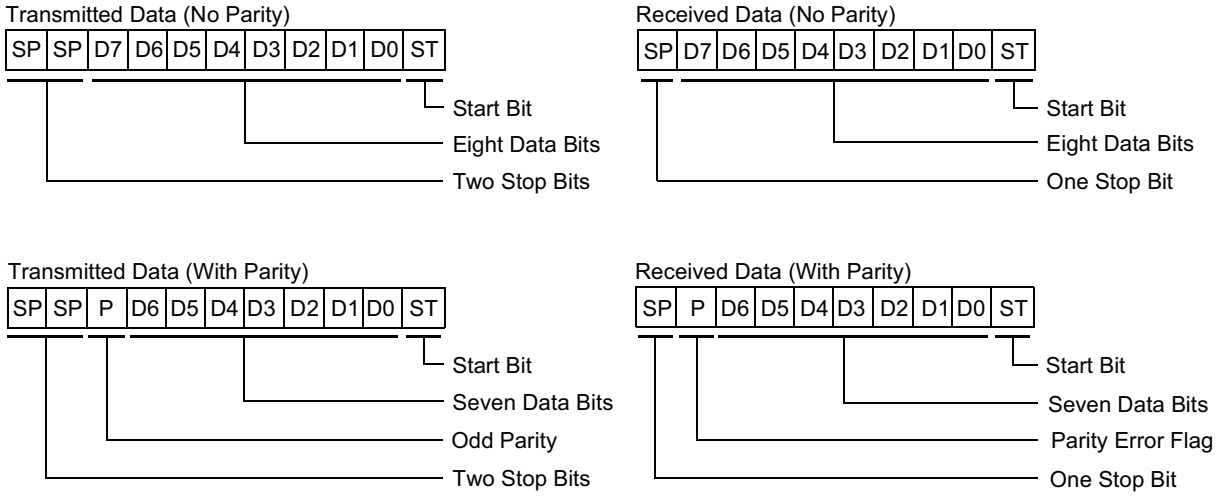


Figure 12. Serial Data Formats

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not driven by any source.

Note: P33–P30 inputs differ from the Z86C61/C63 in that there is no clamping diode to V_{CC} because of the EPROM high voltage detection circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM Mode.

Table 33. Timing of Programming Waveforms (Continued)

Parameters	Name	Min	Max	Unit
7	Data Hold Time	2		µs
8	$\overline{OE}$ Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	$\overline{PGM}$ Setup Time	2		µs
14	Address to $\overline{OE}$ Setup Time	2		µs
15	Option Program Pulse Width	78		ms

User MODE 1: EPROM Read

The Z86E61/Z86E63 EPROM read cycle is provided so that the user may read the Z86E61/Z86E63 MCU as a standard 27128 (Z86E61) or 27256 (Z86E63) EPROM. This is accomplished by driving the EPM pin (P32) to V_H and activating CE and OE. PGM remains inactive. This mode is not valid after execution of an EPROM protect cycle.

Timing for the EPROM read cycle is shown in Figure 20.

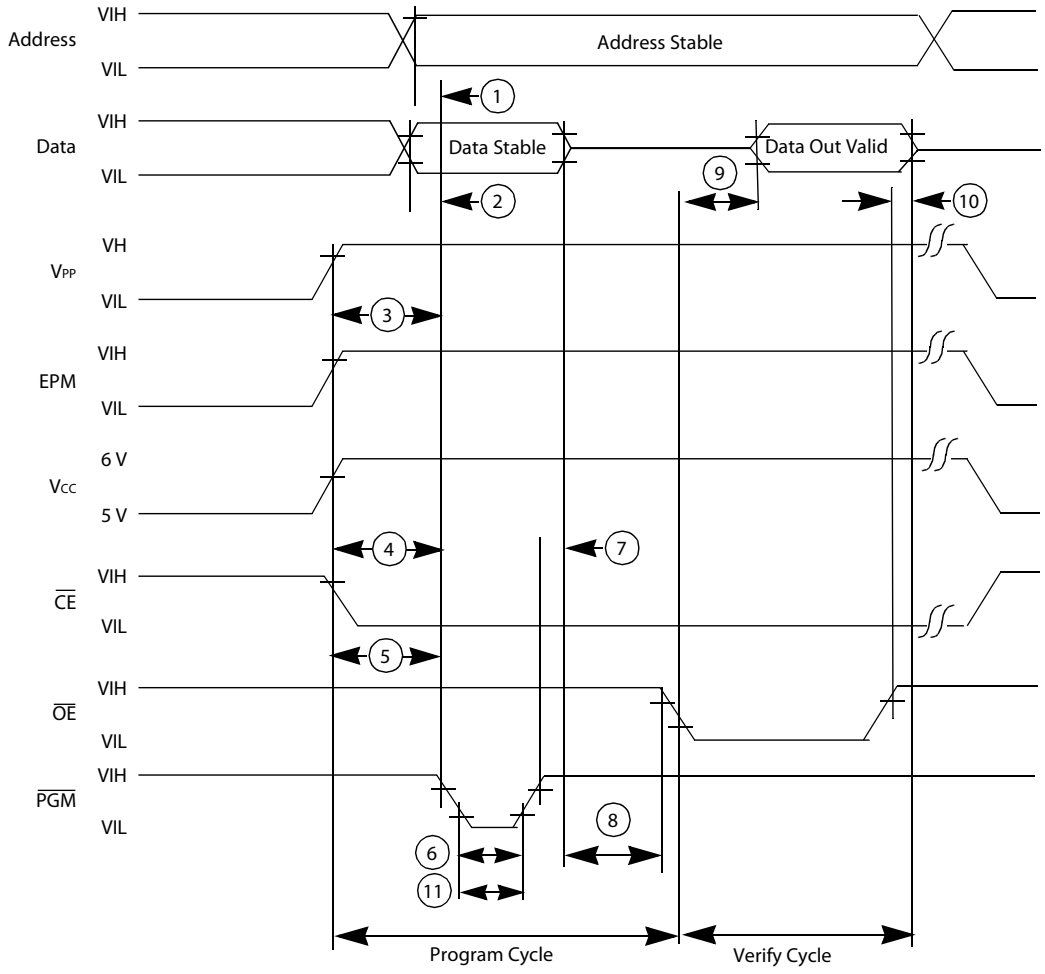


Figure 21. EPROM Program and Verify Timing

User Mode 3: PROM Verify

The Program Verify cycle is used as part of the intelligent programming algorithm to insure data integrity under worst-case conditions. It differs from the EPROM Read cycle in that V_{PP} is active and V_{CC} must be driven to 6.0V. Timing is shown in Figure 21.

User Modes 4 and 5: EPROM and RAM Protect

To extend program security, EPROM and RAM protect cycles are provided for the Z86E61/Z86E63 MCU. Execution of the EPROM protect cycle prohibits proper execution of the EPROM Read, EPROM Verify, and EPROM programming cycles. Execution of the RAM protect cycle disables accesses to the upper 128 bytes of register memory (excluding

mode and configuration registers), but first the user's program must set bit 6 of the IMR (R251). Timing is shown in Figure 22.

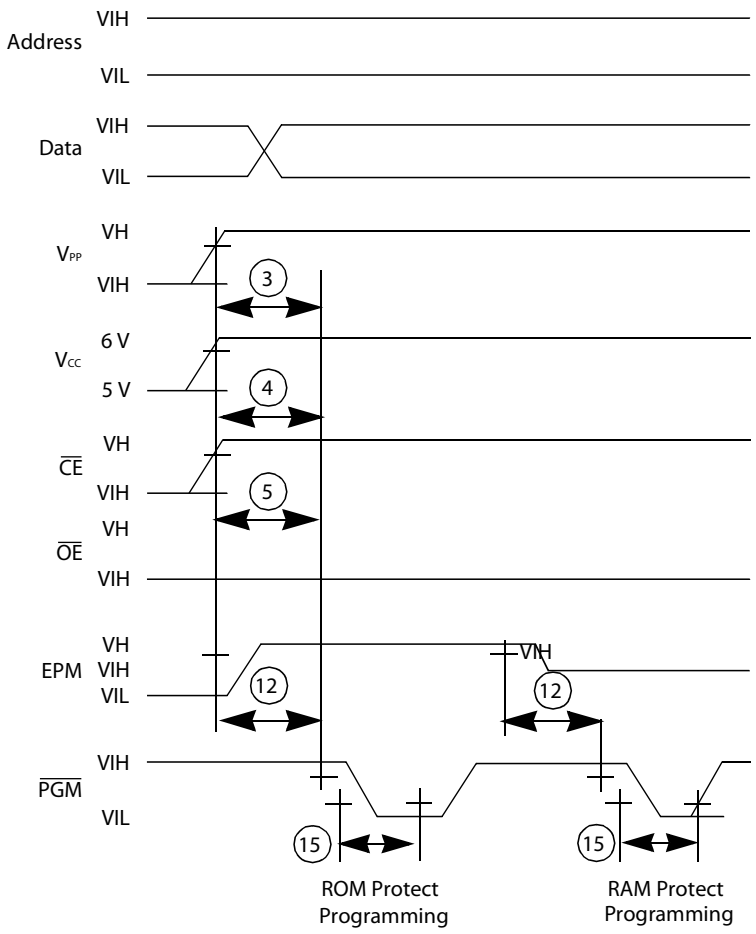


Figure 22. Programming EPROM and RAM Protect

Z86E63 Signal Description for EPROM Program/Read

The following signals are required to correctly program or read the Z86E63 device.

ADDR

The address must remain stable throughout the program read cycle. On both the Z86E61 and Z86E63 MCUs, all A0–A14 address lines must be driven at all times.

Additional timing characteristics are shown in Figure 30 and described in Table 39.

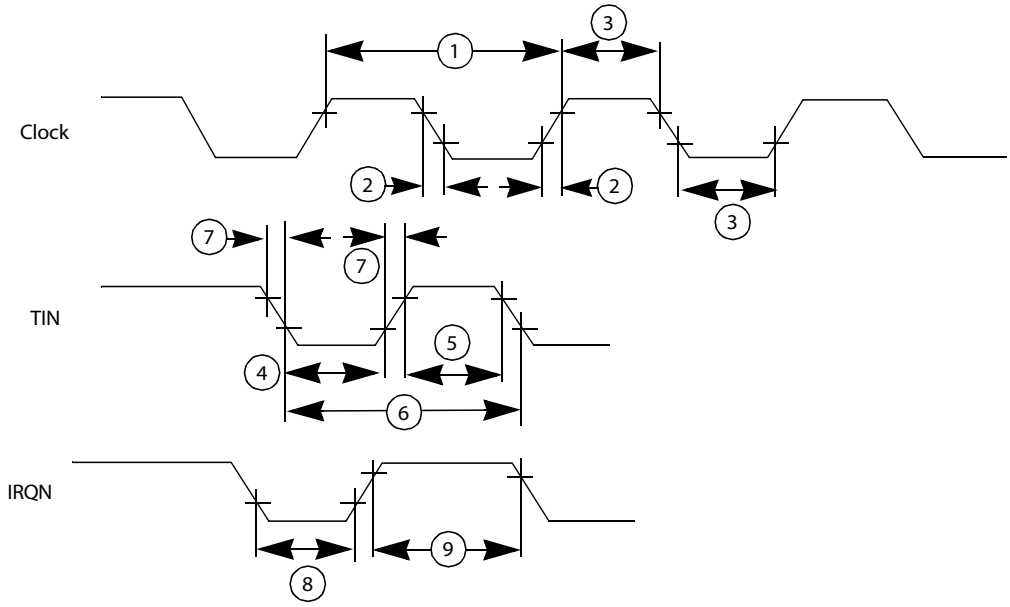


Figure 30. Additional Timing

Table 39. Additional Timing

			TA = 0°C to +70°C					
			16MHz[1]		20MHz			
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	62.5	1000	50	1000	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times		10		15	ns	1
3	TwC	Input Clock Width	21		37		ns	1
4	$TwT_{IN}L$	Timer Input Low Width	50		75		ns	2
5	$TwT_{IN}H$	Timer Input High Width	5TpC		5TpC			2
6	TpT_{IN}	Timer Input Period	8TpC		8TpC			2
7	TrT_{IN},TfT_{IN}	Timer Input Rise & Fall times	100		100		ns	2

Notes:
1. Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
3. Interrupt request through Port 3 (P33–P31).
4. Interrupt request through Port 30.
5. Interrupt references request through Port 3.

Table 39. Additional Timing (Continued)

			TA = 0°C to +70°C					
			16MHz[1]		20MHz			
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
8A	TwIL	Interrupt Request Input Low Times	70		50		ns	2,3
8B	TwIL	Interrupt Request Input Low Times	5TpC		5TpC			2,4
9	TwIH	Interrupt Request Input High Times	5TpC		5TpC			2,5

Notes:
1. Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
3. Interrupt request through Port 3 (P33–P31).
4. Interrupt request through Port 30.
5. Interrupt references request through Port 3.

Control Registers

Figures 31 through 46 provide brief bit descriptions of each of the Z86E61/Z86E63 MCU's control registers.

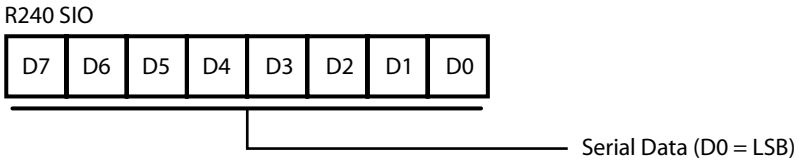


Figure 31. Serial I/O Register (F0H: Read/Write)

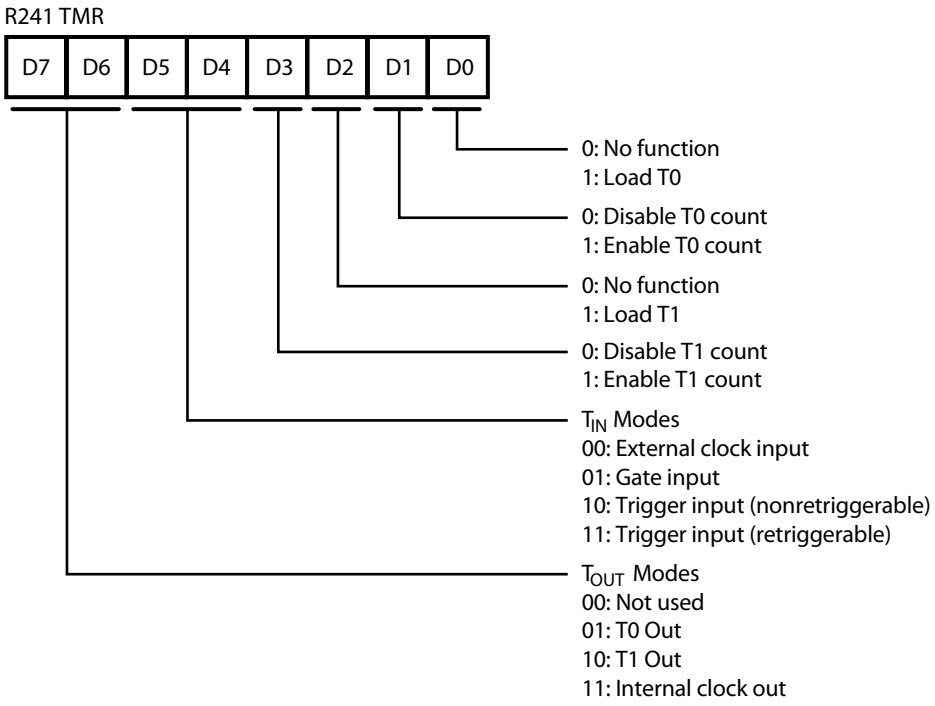


Figure 32. Timer Mode Register (F1H: Read/Write)

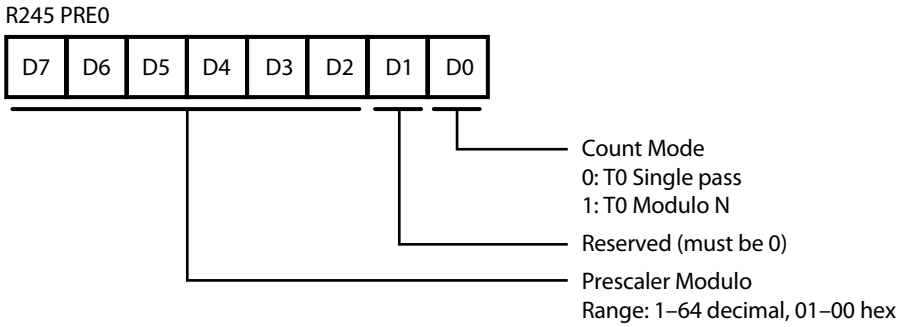


Figure 36. Prescaler 0 Register (F5H: Write Only)

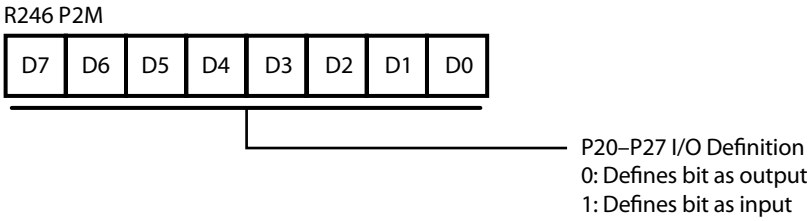


Figure 37. Port 2 Mode Register (F6H: Write Only)

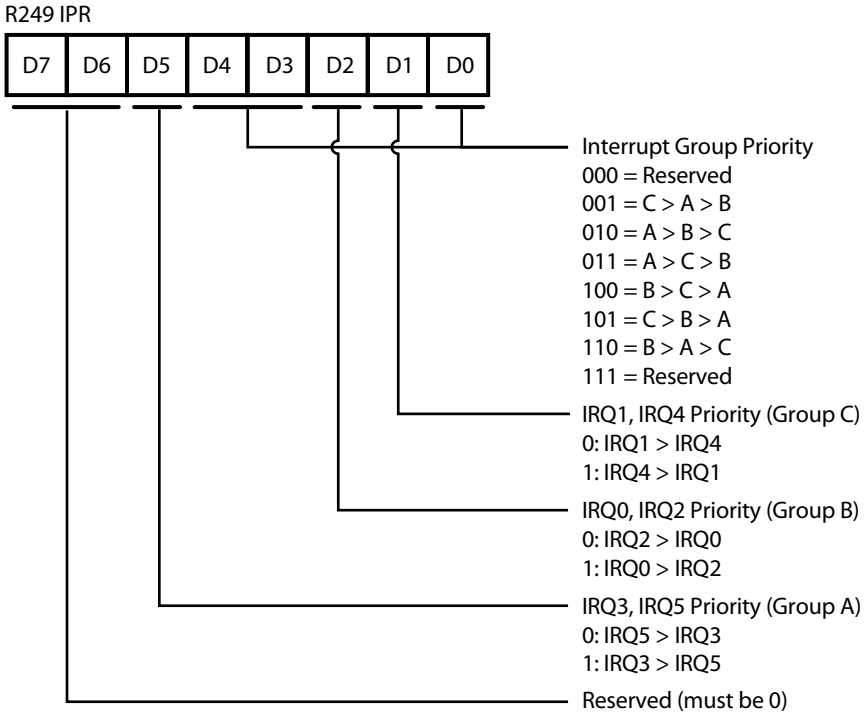


Figure 40. Interrupt Priority Register (F9H: Write Only)

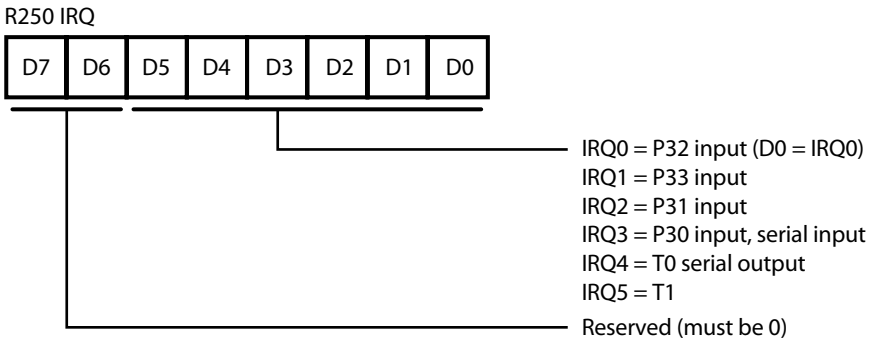


Figure 41. Interrupt Request Register (FAH: Read/Write)

Instruction Formats

Figure 47 shows the one-, two- and three-byte formats used in the Z8 instruction set.

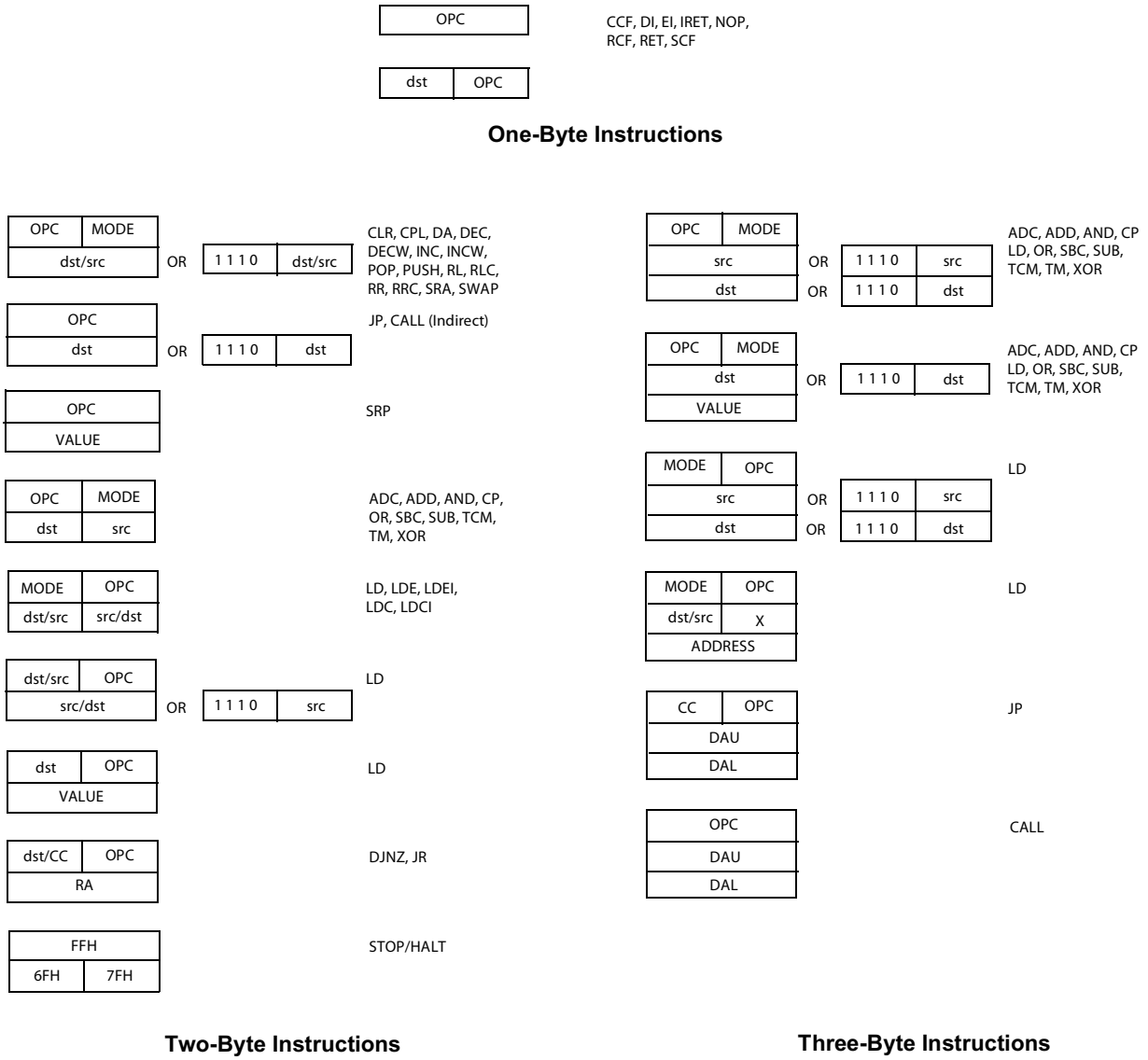


Figure 47. Instruction Formats

Table 45. Instruction Summary (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Op Code Byte (Hex)	Flags Affected C	Z	S	V	D	H
DJNZ r, dst r ← r – 1 if r ≠ 0 PC ← PC + dst Range: +127, –128	RA		rA r = 0 – F	–	–	–	–	–	–
EI IRM(7) ← 1			BF	*	*	*	*	*	*
HALT			7F	–	–	–	–	–	–
INC dst dst ← dst + 1	r R IR		rE r = 0 – F 20 21	–	*	*	*	–	–
INCW dst dst ← dst + 1	RR IR		A0 A1	–	*	*	*	–	–
IRET FLAGS ← @SP; SP ← SP + 1 PC ← @SP; SP ← SP + 2; IMR(7) ← 1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC ← dst	DA IRR		cD c = 0 – F 30	–	–	–	–	–	–
JR cc, dst if cc is true, PC ← PC + dst Range: +127, –128	RA		cB c = 0 – F	–	–	–	–	–	–

Note: These instructions have an identical set of addressing modes, which are encoded for brevity. The first Op Code nibble is found in this instruction set table. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found on the left of the applicable addressing mode pair in the Op Code Map in Figure 48.

For example, the op code of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Part Number Suffix Designations

Zilog part numbers consist of a number of components. For the Z86E61/Z86E63 MCU, these components are:

Environmental Flow
G = Lead-Free Packaging

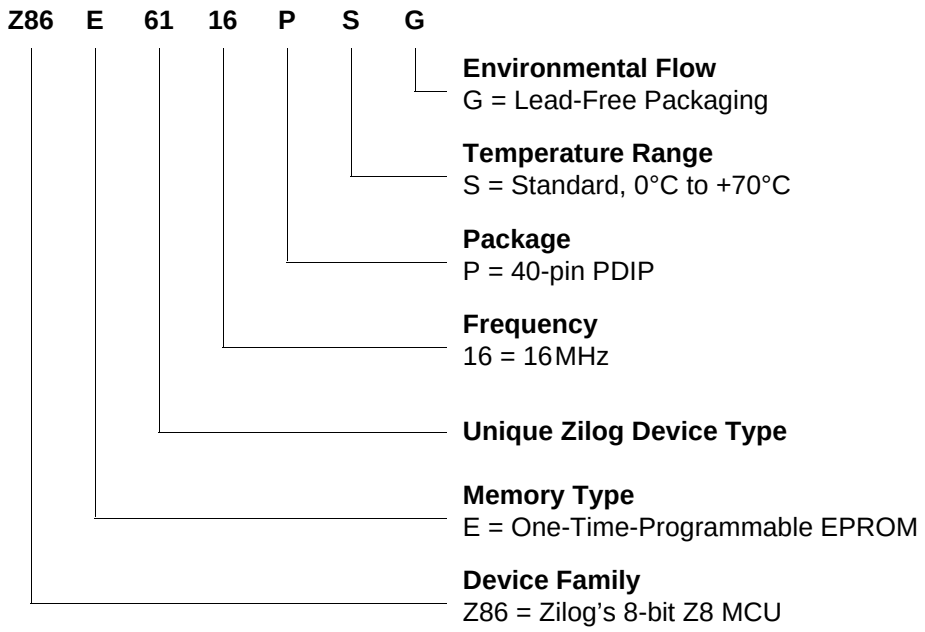
Temperature Range
S = 0ºC to +70ºC

Package
P = 40-pin Plastic DIP (PDIP)
V = 44-pin Plastic Chip Carrier (PLCC)
A = 44-pin Low-Profile Quad Flat Package (LQFP)

Frequency
16 = 16MHz
20 = 20MHz

Memory Type
E = One-Time-Programmable EPROM

Example. Part number Z86E6116PSC is an 8-bit Z8-powered MCU operating at a 16MHz frequency in a 40-pin PDIP package, operating within a 0ºC to +70ºC temperature range and built using lead-free solder.



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