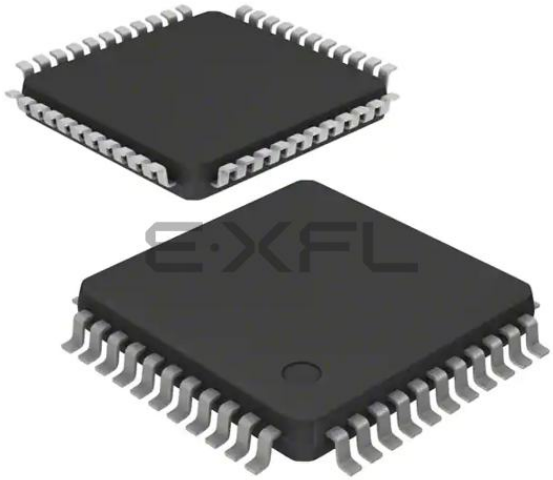

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e6116fsc

Revision History

Each instance in the following revision history table reflects a change to this document from its previous version. For more details, refer to the corresponding pages or appropriate links provided in the table.

Date	Revision Level	Description	Page
Feb 2012	04	Globally updated for style and content.	All
Oct 2008	03	Updated pin descriptions.	11
May 2008	02	Added LQFP pin diagram (Standard and Programming modes); replaced 44-pin QFP with 44-pin LQFP for CR #10886.	7, 8
Nov 2001	01	Original issue.	All

Table of Contents

Figure 3 shows the pin-outs for the 40-pin PDIP EPROM Programming Mode package; Table 26 describes each pin.

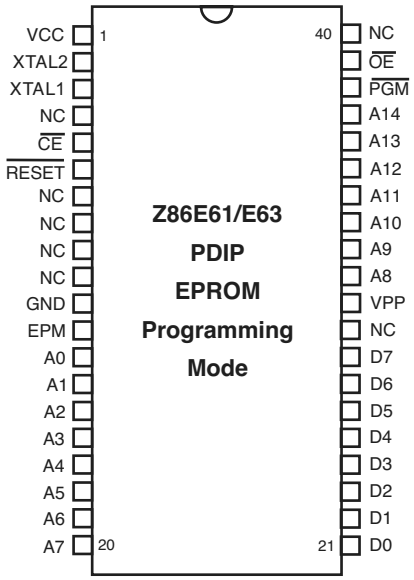


Figure 3. Z86E61/Z86E63 PDIP Pin Diagram, EPROM Programming Mode

Table 26. Z86E61/Z86E63 PDIP Pin Description, EPROM Programming Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{CE}$	Chip Enable	Input
$\overline{RESET}$	Reset	Input
EPM	EPROM Programming Mode	Input
A0–A14	15-bit Address Bus	Input
D7–D0	8-bit Data Bus	Input/Output
V_{PP}	Programming Voltage	Input
$\overline{PGM}$	Programming Mode	Input
$\overline{OE}$	Output Enable	Input
NC	Not Connected	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Pin Descriptions

This section describes the major Z86E61/Z86E63 MCU pin signals and ports.

ROMless (Input, Active Low)

Connecting this pin to GND disables the internal ROM and forces the device to function as a Z86C91 ROMless Z8 (see the Z86C91 product specification for more information). When pulled High to V_{CC}, the device functions as a normal Z86E61/Z86E63 EPROM version. This pin is only available on the 44-pin versions of the Z86E61/Z86E63 MCU.

DS (Output, Active Low)

Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of DS. For WRITE operations, the falling edge of DS indicates that output data is valid.

AS (Output, Active Low)

Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of AS. Under program control, AS can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL2, XTAL1

Crystal 2, Crystal 1 (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R/W (Output, Write Low)

The Read/Write signal is Low when the MCU is writing to the external program or data memory.

RESET (Input, Active Low)

To avoid asynchronous and noisy reset problems, the Z86E61/Z86E63 MCU is equipped with a reset filter of four external clocks (4TpC). If the external RESET signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external RESET, whichever is longer. During the reset cycle, DS is held active Low while AS cycles at a rate of TpC/2. When RESET is deactivated, program execution begins at location `000Ch`. Power-up reset time must be held low for 50 ms, or until V_{CC} is stable, whichever is longer.

Port 0 (P07–P00)

Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07–P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 can provide address bits A11–A8 (lower nibble) or A15–A8 (lower and upper nibbles) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode Register.

In ROMless Mode, after a hardware reset, the Port 0 lines are defined as address lines A15–A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode; see Figure 8.

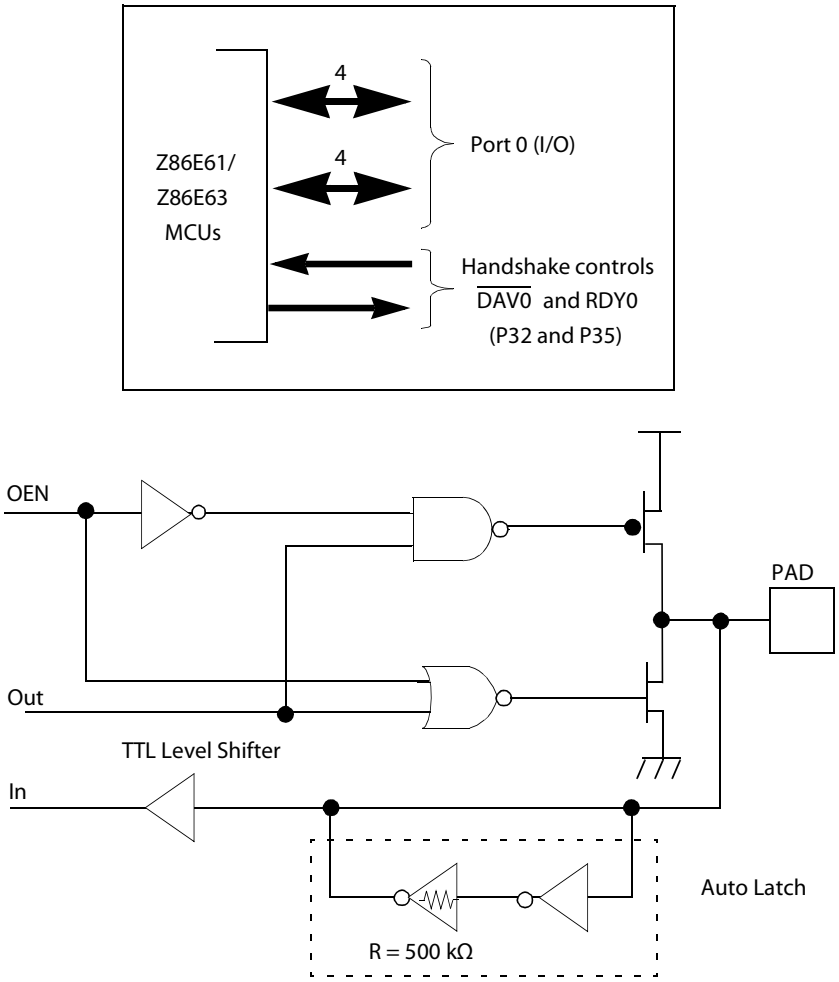


Figure 8. Port 0 Configuration

Port 1 (P17–P10)

Port 1 is an 8-bit, byte programmable, bidirectional, TTL compatible port. It has multiplexed Address (A7–A0) and Data (D7–D0) ports. For the Z86E61/Z86E63 MCU, these eight I/O lines can be programmed as input or output lines or are configured under software control as an address/data port for interfacing external memory. When used as an I/O port, Port 1 can be placed under handshake control. In this configuration, Port 3 lines, P33 and P34, are used as the handshake controls RDY1 and DAV1.

Memory locations greater than 16384 (Z86E61) or 32768 (Z86E63) are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multi-

Port 3 (P37–P30)

Port 3 is an 8-bit, CMOS compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33–P30) input and four-fixed (P37–P34) output ports. Port 3, when used as serial I/O, is programmed as serial in and serial out, respectively; see Figure 11.

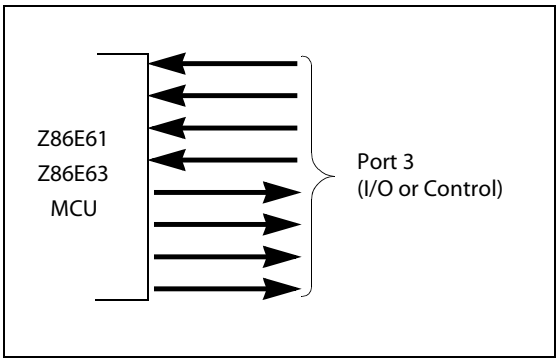


Figure 11. Port 3 Configuration

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (DAV and RDY); four external interrupt request signals (IRQ3–IRQ0); timer input and output signals (T_{IN} and T_{OUT}) Data Memory Select ($\overline{DM}$) and EPROM control signals (P30 = $\overline{CE}$, P31 = $\overline{OE}$, P32 = EPM and P33 = V_{PP}).

Table 31 lists the pin assignments for Port 3.

Table 31. Port 3 Pin Assignments*

Pin	I/O	CTCI	Interrupt	P0 HS	P1 HS	P2 HS	UART	Ext	EPROM
P30	In	T_{IN}	IRQ3				Serial In		$\overline{CE}$
P31	In	T_{IN}	IRQ2			D/R			$\overline{OE}$
P32	In	T_{IN}	IRQ0	D/R					EPM
P33	In	T_{IN}	IRQ1		D/R				V_{PP}
P34	Out	T_{OUT}			R/D			$\overline{DM}$	
P35	Out	T_{OUT}		R/D					
P36	Out	T_{OUT}				R/D			
P37	Out	T_{OUT}					Serial Out		
T0			IRQ4						
T1			IRQ5						

Note: *HS = Handshake Signals; D = Data Available; R = Ready.

Address Space

This section describes the memory and addressing functions of the Z86E61/Z86E63 MCU.

Program Memory

The Z86E61/Z86E63 MCU can address 48KB (Z86E61) or 32KB (Z86E63) of external program memory; see Figure 13. The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM Mode, byte 13 to byte 16383 (Z86E61) or 32767 (Z86E63) consists of on-chip EPROM. At addresses 16384 (Z86E61) or 32768 (Z86E63) and above, the Z86E61/Z86E63 MCU executes external program memory fetches. In ROMless Mode, the Z86E61/Z86E63 MCU can address up to 64KB of program memory. Program execution begins at external location 000C (HEX) after a reset.

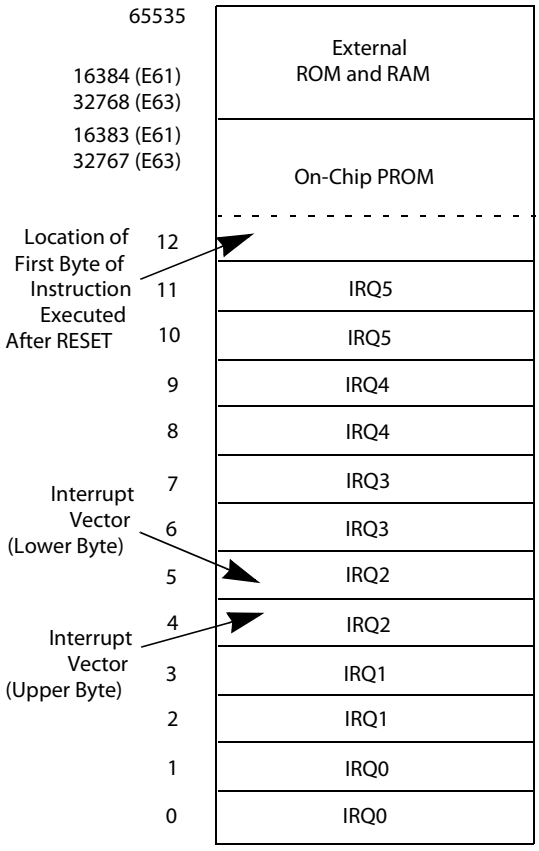


Figure 13. Program Memory Configuration

Register File

The register file consists of four I/0 port registers, 236 general-purpose registers, and 16 control and status registers, as shown in Figure 15. The instructions can access registers directly or indirectly through an 8-bit address field. The Z86E61/Z86E63 MCU also allows short 4-bit register addressing using the Register Pointer, which is shown in Figure 16. In 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

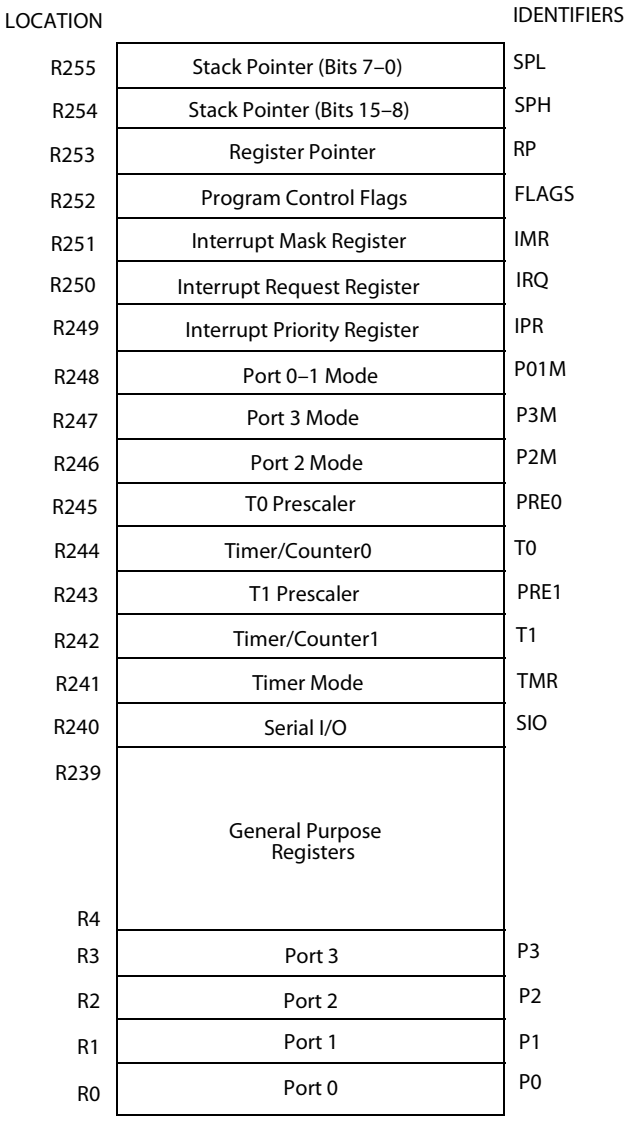


Figure 15. Register File

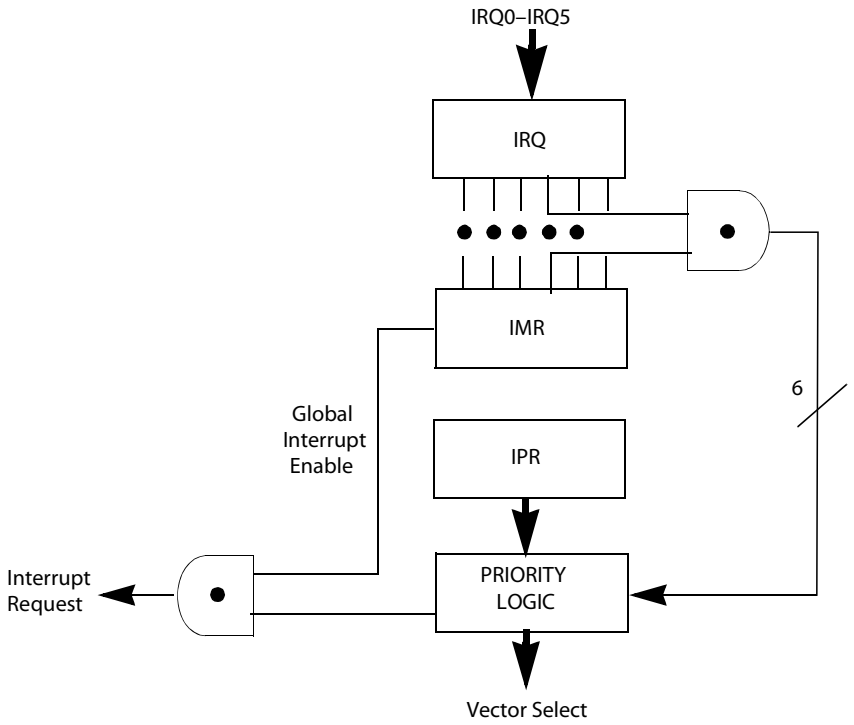


Figure 18. Interrupt Block Diagram

For the ROMless Mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the Flag Register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

Clock

The Z86E61/Z86E63 MCU's on-chip oscillator features a high gain, parallel resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 20 MHz max; series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF < CL < 100 pF) from each pin to ground; see Figure 19.

Table 33. Timing of Programming Waveforms (Continued)

Parameters	Name	Min	Max	Unit
7	Data Hold Time	2		µs
8	$\overline{OE}$ Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	$\overline{PGM}$ Setup Time	2		µs
14	Address to $\overline{OE}$ Setup Time	2		µs
15	Option Program Pulse Width	78		ms

User MODE 1: EPROM Read

The Z86E61/Z86E63 EPROM read cycle is provided so that the user may read the Z86E61/Z86E63 MCU as a standard 27128 (Z86E61) or 27256 (Z86E63) EPROM. This is accomplished by driving the EPM pin (P32) to V_H and activating CE and OE. PGM remains inactive. This mode is not valid after execution of an EPROM protect cycle.

Timing for the EPROM read cycle is shown in Figure 20.

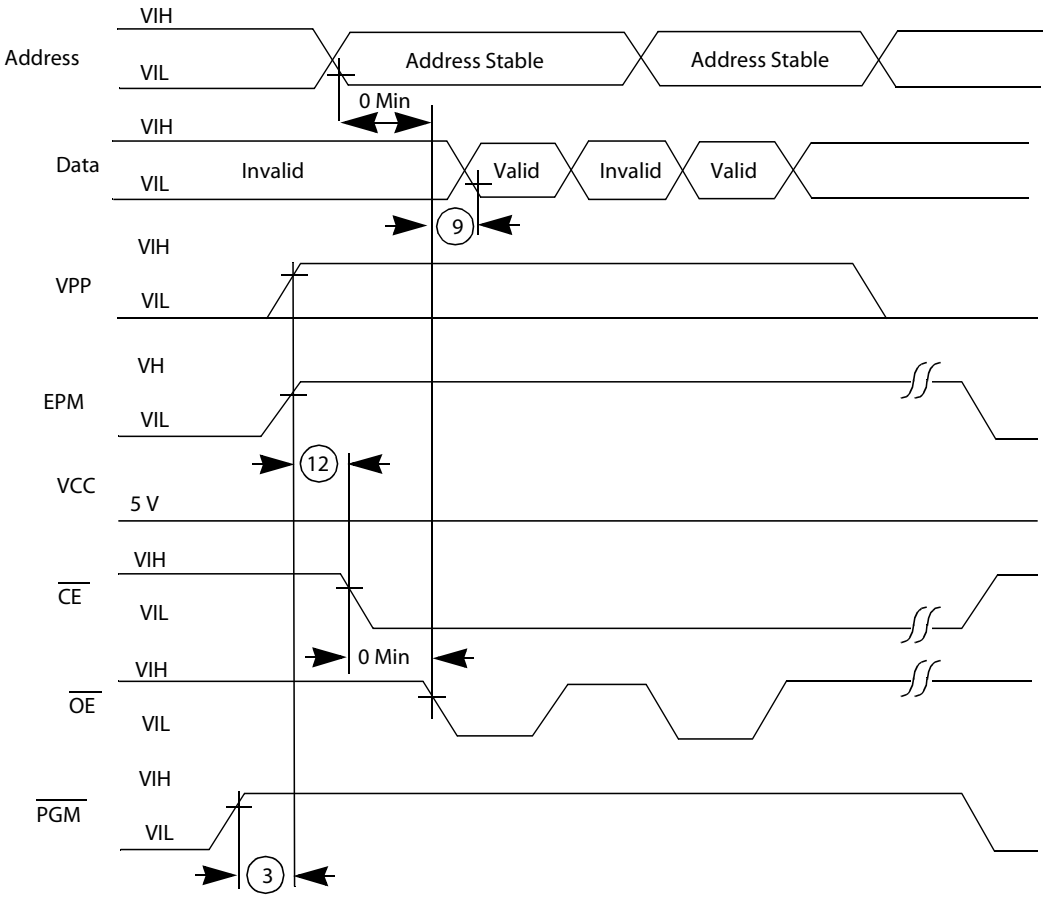


Figure 20. EPROM Read Timing

User MODE 2: EPROM Program

The Z86E61/Z86E63 MCU's Program function conforms to the Intelligent programming algorithm. The device is programmed with V_{CC}, at 6.0V and V_{PP} = 12.5V. Programming pulses are applied in 1 ms increments to a maximum of 25 pulses before proper verification. After verification, a programming pulse of three times the duration of the cycles necessary to program the device is issued to ensure proper programming. After all addresses are programmed, a final data comparison is executed and the programming cycle is complete. Timing for the Z86E61/Z86E63 MCU programming cycle is shown in Figure 21.

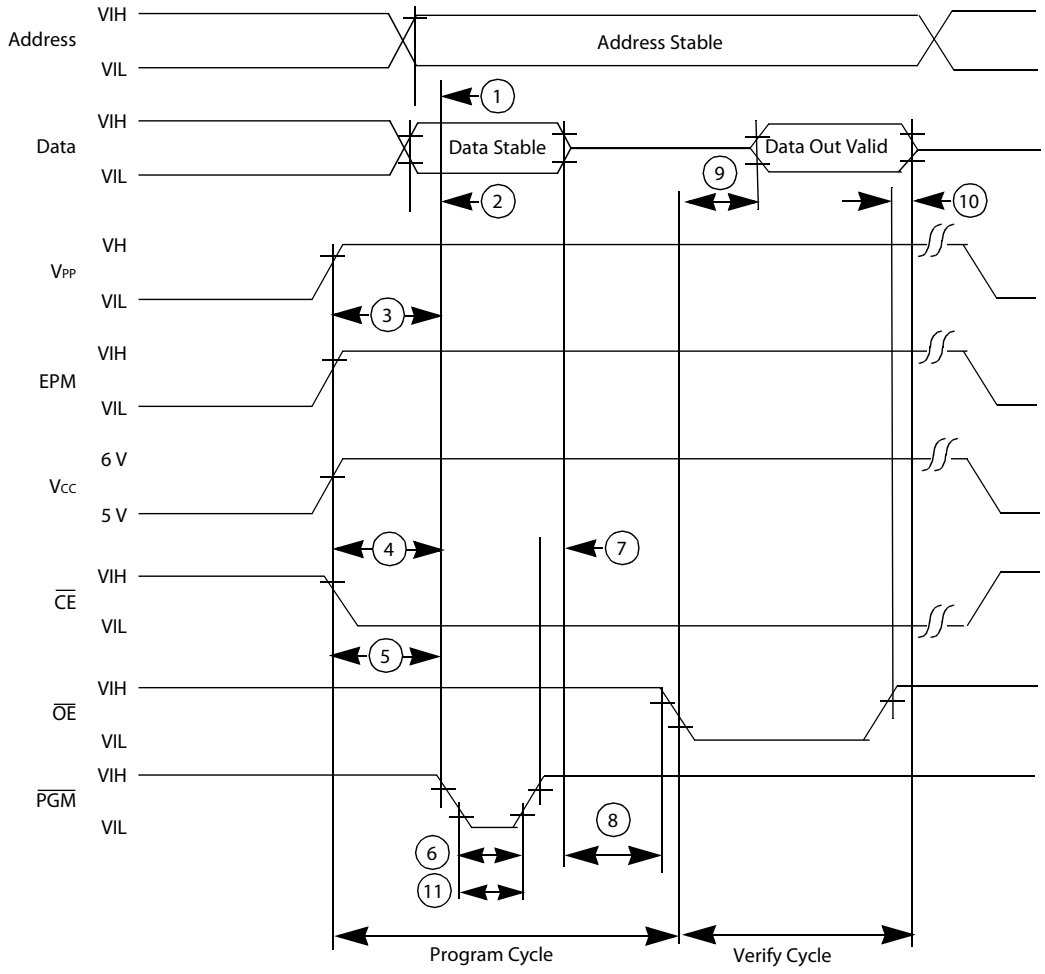


Figure 21. EPROM Program and Verify Timing

User Mode 3: PROM Verify

The Program Verify cycle is used as part of the intelligent programming algorithm to insure data integrity under worst-case conditions. It differs from the EPROM Read cycle in that V_{PP} is active and V_{CC} must be driven to 6.0V. Timing is shown in Figure 21.

User Modes 4 and 5: EPROM and RAM Protect

To extend program security, EPROM and RAM protect cycles are provided for the Z86E61/Z86E63 MCU. Execution of the EPROM protect cycle prohibits proper execution of the EPROM Read, EPROM Verify, and EPROM programming cycles. Execution of the RAM protect cycle disables accesses to the upper 128 bytes of register memory (excluding

Standby Current

Figure 26 shows the typical standby current values (in milliamps), for the Z86E61/ Z86E63 MCU as a function of frequency (in megahertz).

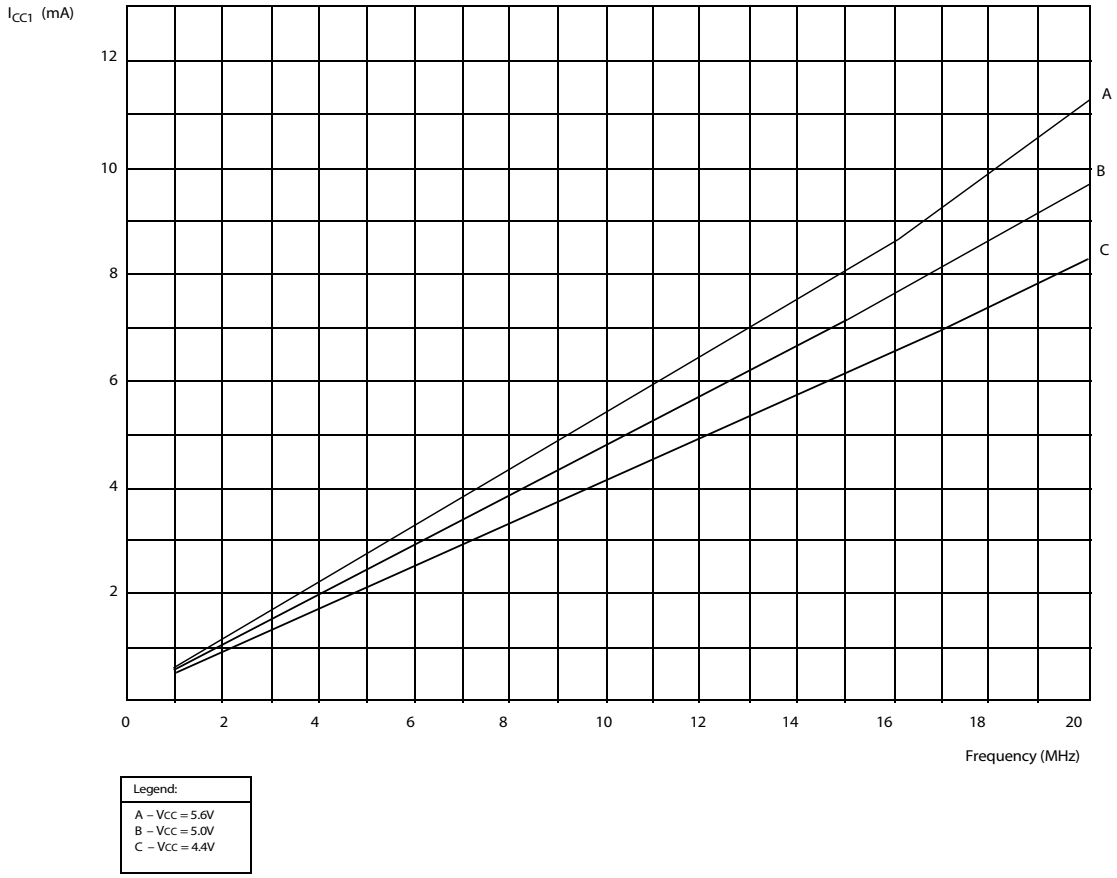


Figure 26. Typical I_{CC1} vs. Frequency

Additional timing characteristics are shown in Figure 30 and described in Table 39.

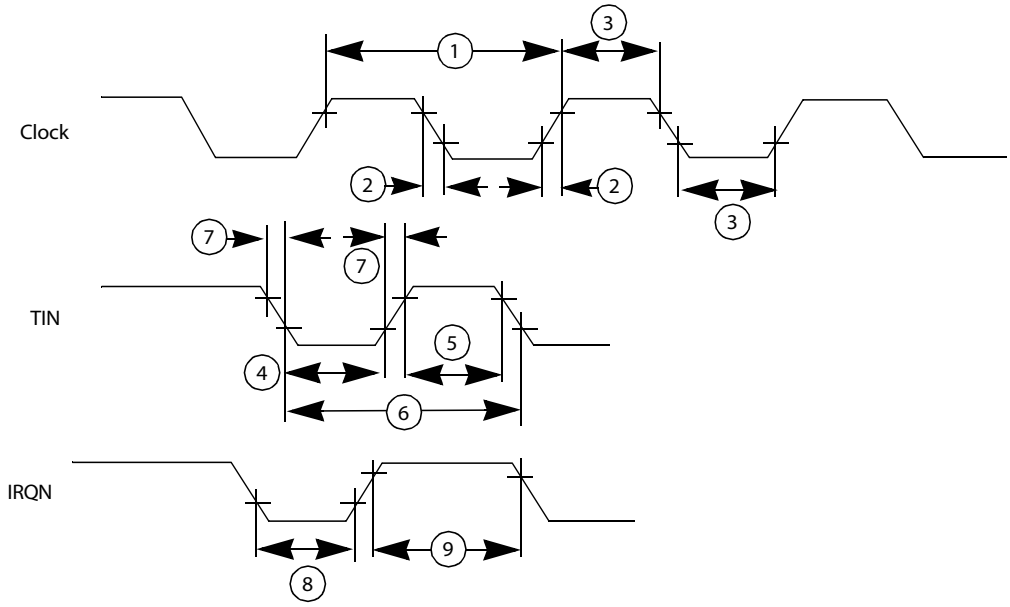


Figure 30. Additional Timing

Table 39. Additional Timing

			TA = 0°C to +70°C					
			16MHz[1]		20MHz			
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	62.5	1000	50	1000	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times		10		15	ns	1
3	TwC	Input Clock Width	21		37		ns	1
4	$TwT_{IN}L$	Timer Input Low Width	50		75		ns	2
5	$TwT_{IN}H$	Timer Input High Width	5TpC		5TpC			2
6	TpT_{IN}	Timer Input Period	8TpC		8TpC			2
7	TrT_{IN},TfT_{IN}	Timer Input Rise & Fall times	100		100		ns	2

Notes:
1. Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
3. Interrupt request through Port 3 (P33–P31).
4. Interrupt request through Port 30.
5. Interrupt references request through Port 3.

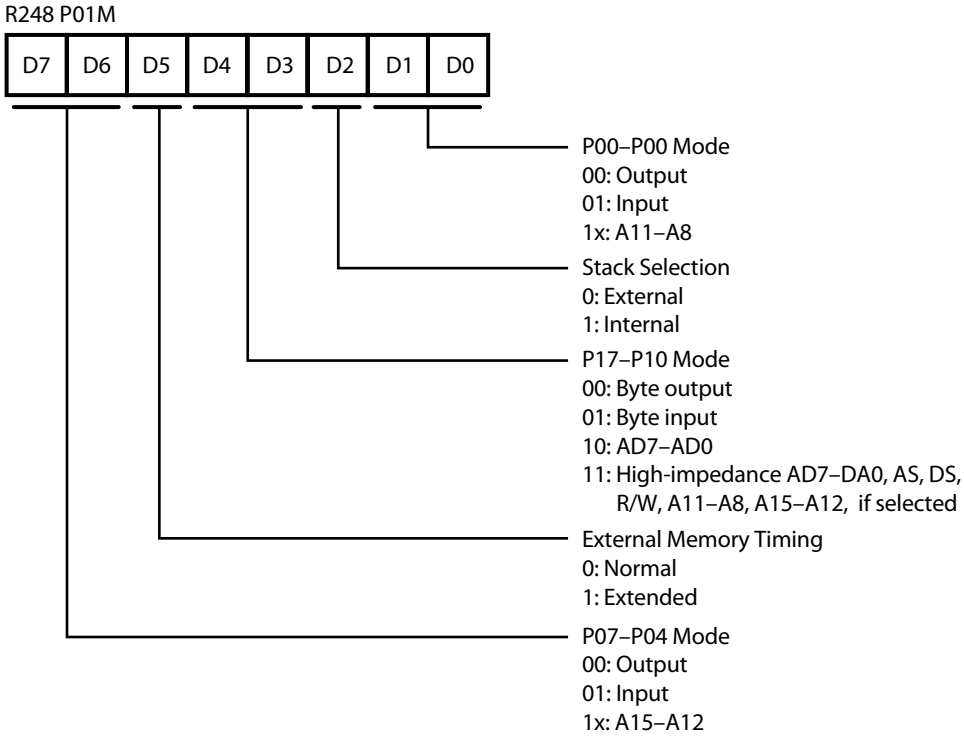


Figure 39. Port 0 and 1 Mode Register (F8H: Write Only)

Instruction Formats

Figure 47 shows the one-, two- and three-byte formats used in the Z8 instruction set.

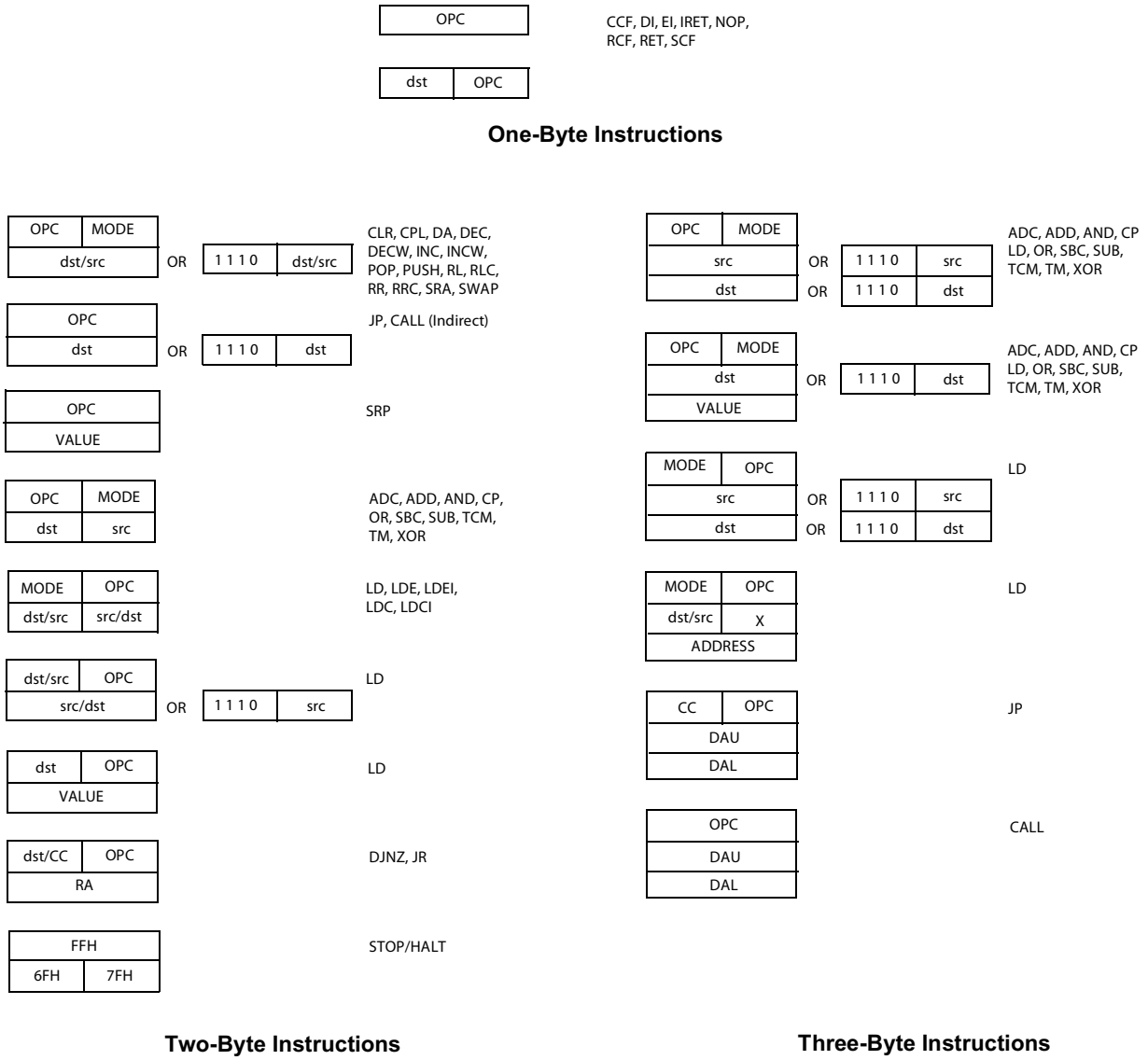


Figure 47. Instruction Formats

Table 45. Instruction Summary (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Op Code Byte (Hex)	Flags Affected C	Z	S	V	D	H
DJNZ r, dst r ← r – 1 if r ≠ 0 PC ← PC + dst Range: +127, –128	RA		rA r = 0 – F	–	–	–	–	–	–
EI IRM(7) ← 1			BF	*	*	*	*	*	*
HALT			7F	–	–	–	–	–	–
INC dst dst ← dst + 1	r R IR		rE r = 0 – F 20 21	–	*	*	*	–	–
INCW dst dst ← dst + 1	RR IR		A0 A1	–	*	*	*	–	–
IRET FLAGS ← @SP; SP ← SP + 1 PC ← @SP; SP ← SP + 2; IMR(7) ← 1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC ← dst	DA IRR		cD c = 0 – F 30	–	–	–	–	–	–
JR cc, dst if cc is true, PC ← PC + dst Range: +127, –128	RA		cB c = 0 – F	–	–	–	–	–	–

Note: These instructions have an identical set of addressing modes, which are encoded for brevity. The first Op Code nibble is found in this instruction set table. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found on the left of the applicable addressing mode pair in the Op Code Map in Figure 48.

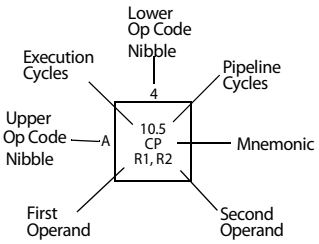
For example, the op code of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Op Code Map

Figure 48 shows a map of the Z86E61/Z86E63 MCU's operational codes.

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.6 DEC R1	6.5 DEC IR1	6.5 ADD r1, r2	8.5 ADD r1, Ir2	10.5 ADD R2,R1	10.5 ADD IR2, R1	10.5 ADD R1, 1M	10.5 ADD R1, 1M	6.5 LD r1, R2	6.5 LD r2, R1	12/10.5 DJNZ r1, RA	12/0.0 JA cc, RA	6.5 LD r1, 1M	12/10.0 JP cc, DA	6.5 INC r1	
1	6.5 RLC R1	6.5 RLC IR1	6.5 ADC r1, r2	6.5 ADC r1, Ir2	10.5 ADC R2, R1	10.5 ADC IR2, R1	10.5 ADC R1, 1M	10.5 ADC R1, 1M								
2	6.5 INC R1	6.6 WC IR1	6.5 SUB r1, r2	0.5 SUB r1, Ir2	10.5 SUB R2, R1	10.5 SUB IR2, R1	10.5 SUB R2, 1M	10.5 BUB IR1, 1M								
3	6.5 JP IRR1	6.1 SRP 1M	6.5 SBC r1, r2	6.5 OR r1, Ir2	10.5 SBC R2, R1	10.5 SBC IR2, R1	10.5 SBC R1, 1M	10.5 SBC IR1, 1M								
4	8.5 DA R1	8.5 DA IR1	6.5 OR r1, r2	6.5 OR r1, Ir2	10.5 OR R2, R1	10.5 OR IR2, R1	10.5 OR R1, 1M									
5	10.5 POP R1	10.5 POP IR1	6.5 AND r1, r2	6.5 AND r1, Ir2	10.5 AND R2, R1	10.5 AND IR2, R1	10.5 AND R1, 1M	10.5 TCM IR1, 1M								
6	6.5 COM R1	6.5 COM IR1	6.5 TCM r1, r2	6.5 TCM r1, Ir2	10.5 TCM R2, R1	10.5 TCM IR2, R1	10.5 TCM R1, 1M	10.5 TCM IR1, 1M								6.0 STOP
7	10/12.1 PUSH R2	10/12.1 PUSH IR2	6.5 TM r1, r2	6.5 TM r1, Ir2	10.5 TM R2, R1	10.5 TM IR2, R1	10.5 TM R1, 1M	10.5 TM IR1, 1M								7.0 HALT
8	10.5 DECW RR1	10.5 DECW IR1	12.0 LDE r1, Irr2	18.0 LDEI r1, Irr2												6.1 DI
9	6.5 RL R1	6.5 RL IR1	12.0 LDE r1, Irr2	18.0 LDEI r1, Irr2												6.1 EI
A	10.5 INCW RR1	10.5 INCW IR1	6.5 CP r1, r2	6.5 CP r1, Ir2	10.5 CP R2, R1	10.5 CP IR2, R1	10.5 CP R1, 1M	10.5 CP IR1, 1M								14.0 RET
B	6.5 CLR R1	6.5 CLR IR1	6.5 XOR r1, r2	6.5 XOR r1, Ir2	10.5 XOR R2, R1	10.5 XOR R2, R1	10.5 XOR R1, 1M	10.5 XOR IR1, 1M								16.0 IRET
C	6.5 RRC R1	6.5 RRC IR1	12.0 LDC r1, Irr2	18.0 LDC Ir1, Irr2				10.5 LD r1, x, R2								6.5 RCF
D	6.5 SRA R1	6.5 SRA IR1	12.0 LDC r1, Irr2	18.0 LDCI Ir1, Irr2	20.0 CALL* IRR1		20.0 CALL DA	10.5 LD 42, x, R1								6.5 SCF
E	6.5 RR R1	6.5 RR IR1		6.5 LD r1, IR2	10.5 LD R2, R1	10.5 LD IR2, R1	10.5 LD R1, 1M	10.5 LD IR1, 1M								6.5 CCF
F	8.5 SWAP R1	8.5 SWAP IR1		6.5 LD Ir1, r2		10.5 LD R2, IR1										6.0 NOP
Bytes per instruction	2				3				2					3	1	



Legend:
R = 8-bit address
r = 4-bit address
R1 or r1 = dst address
R2 or r2 = src address

Sequence:
Op code, first operand, second operand

Note: *The 2-byte instruction appears as a 3-byte instruction; blank areas are not defined.

Figure 48. Op Code Map