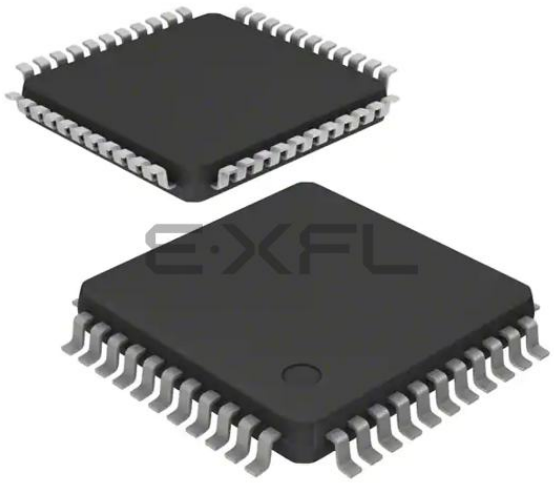

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e6116fsc00tr

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Figure 5 shows the pin-outs for the 44-pin LQFP EPROM Programming Mode package; Table 28 describes each pin.

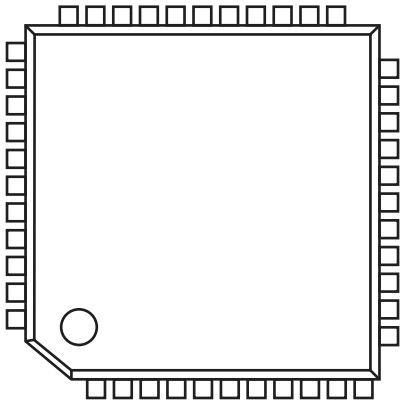

Figure 5. Z86E61/Z86E63 LQFP Pin Diagram, EPROM Programming Mode

Table 28. Z86E61/Z86E63 LQFP Pin Description, EPROM Programming Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{CE}$	Chip Enable	Input
$\overline{RESET}$	Reset	Input
EPM	EPROM Programming Mode	Input
A0–A14	15-bit Address Bus	Input
D7–D0	8-bit Data Bus	Input/Output
V_{PP}	Programming Voltage	Input
$\overline{PGM}$	Programming Mode	Input
$\overline{OE}$	Output Enable	Input
NC	Not Connected	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

plexed Address/ Data Mode. If more than 256 external locations are required, Port 0 must output the additional address lines.

Port 1 can be placed in high-impedance state along with Port 0, AS, DS, and R/W, allowing the MCU to share common resources in multiprocessor and DMA applications. Data transfers are controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus Request output; see Figure 9.

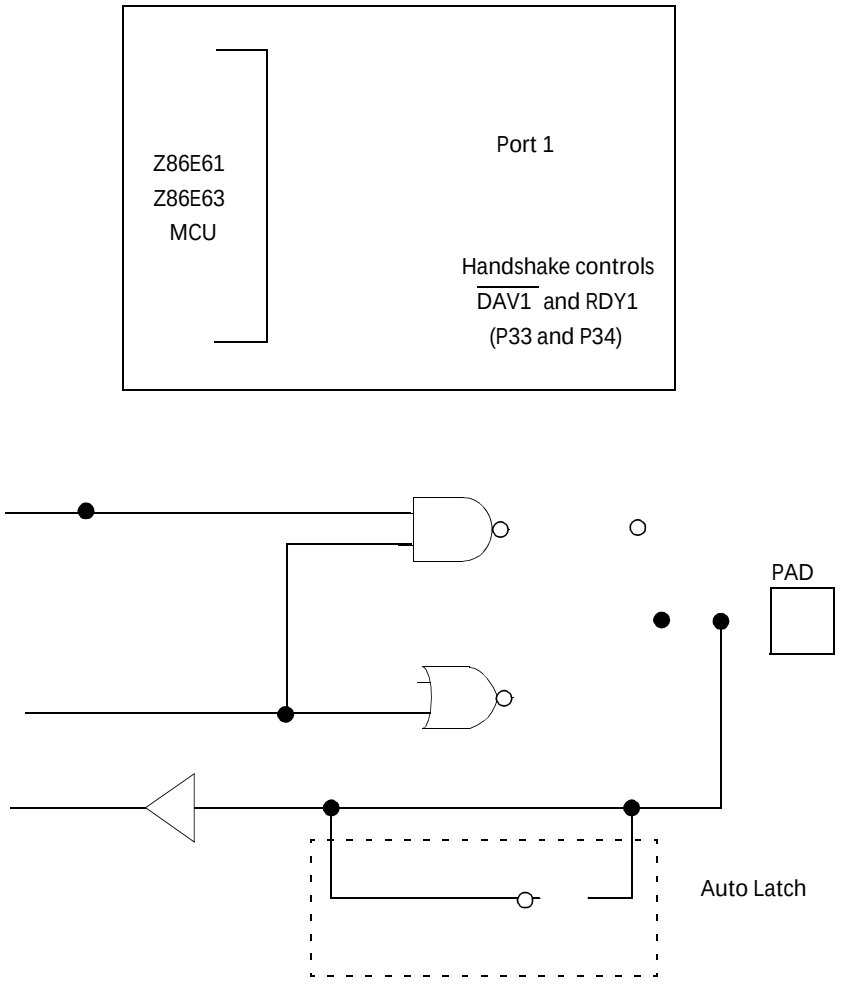

Figure 9. Port 1 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bit programmable, bi-directional, CM0S compatible port. Each of these eight I/0 lines can be independently programmed as an input or output, or globally as an

Port 3 (P37–P30)

Port 3 is an 8-bit, CMOS compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33 P30) input and four-fixed (P37 P34) output ports. Port 3, when used as serial I/O, is programmed as serial in and serial out, respectively; see Figure 11.

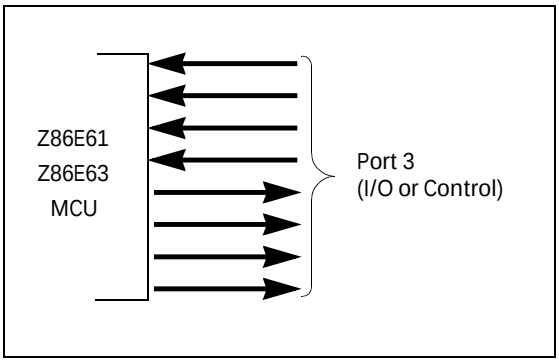

Figure 11. Port 3 Configuration

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (DAV and RDY); four external interrupt request signals (IRQ3 IRQ0); timer input and output signals (T_{IN} and T_{OUT}) Data Memory Select ($\overline{DM}$) and EPROM control signals (P30 = $\overline{CE}$, P31 = $\overline{OE}$, P32 = EPM and P33 = V_{PP}).

Table 31 lists the pin assignments for Port 3.

Table 31. Port 3 Pin Assignments*

Pin	I/O	CTCI	Interrupt	P0 HS	P1 HS	P2 HS	UART	Ext	EPROM
P30	In	T_{IN}	IRQ3				Serial In		$\overline{CE}$
P31	In	T_{IN}	IRQ2			D/R			$\overline{OE}$
P32	In	T_{IN}	IRQ0	D/R					EPM
P33	In	T_{IN}	IRQ1		D/R				V_{PP}
P34	Out	T_{OUT}			R/D			$\overline{DM}$	
P35	Out	T_{OUT}		R/D					
P36	Out	T_{OUT}				R/D			
P37	Out	T_{OUT}					Serial Out		
T0			IRQ4						
T1			IRQ5						

Note: *HS = Handshake Signals; D = Data Available; R = Ready.

UART Operation. Port 3 lines, P37 and P30, are programmed as serial I/0 lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/ Timer0.

The Z86E61/Z86E63 MCU automatically adds a start bit and two stop bits to transmitted data; see Figure 12. Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits, and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

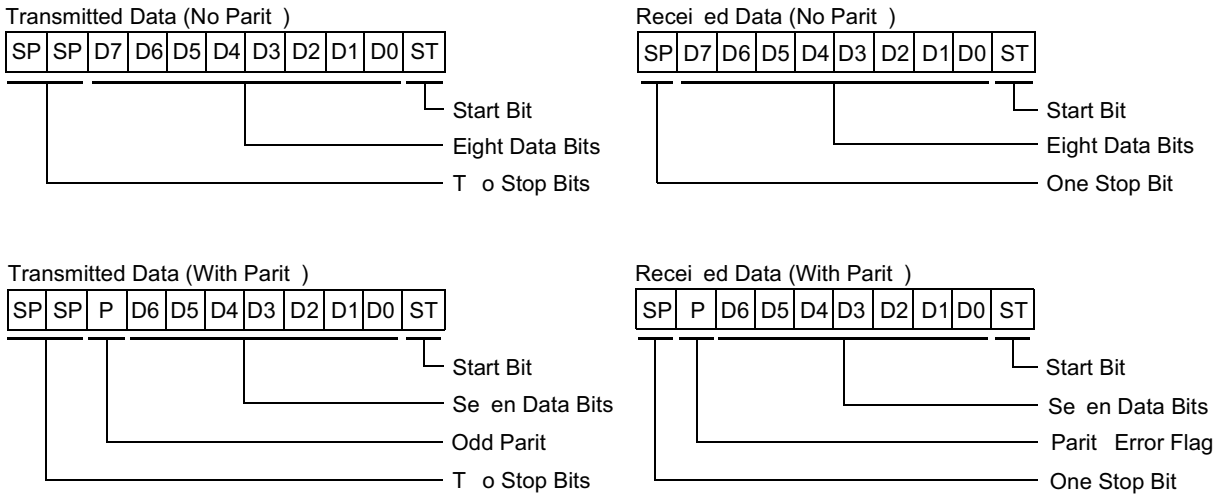

Figure 12. Serial Data Formats

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not driven by any source.

Note: P33 P30 inputs differ from the Z86C61/C63 in that there is no clamping diode to V_{CC} because of the EPROM high voltage detection circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM Mode.

Table 33. Timing of Programming Waveforms (Continued)

Parameters	Name	Min	Max	Unit
7	Data Hold Time	2		µs
8	$\overline{OE}$ Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	$\overline{PGM}$ Setup Time	2		µs
14	Address to $\overline{OE}$ Setup Time	2		µs
15	Option Program Pulse Width	78		ms

User MODE 1: EPROM Read

The Z86E61/Z86E63 EPROM read cycle is provided so that the user may read the Z86E61/Z86E63 MCU as a standard 27128 (Z86E61) or 27256 (Z86E63) EPROM. This is accomplished by driving the EPM pin (P32) to V_H and activating CE and OE. PGM remains inactive. This mode is not valid after execution of an EPROM protect cycle.

Timing for the EPROM read cycle is shown in Figure 20.

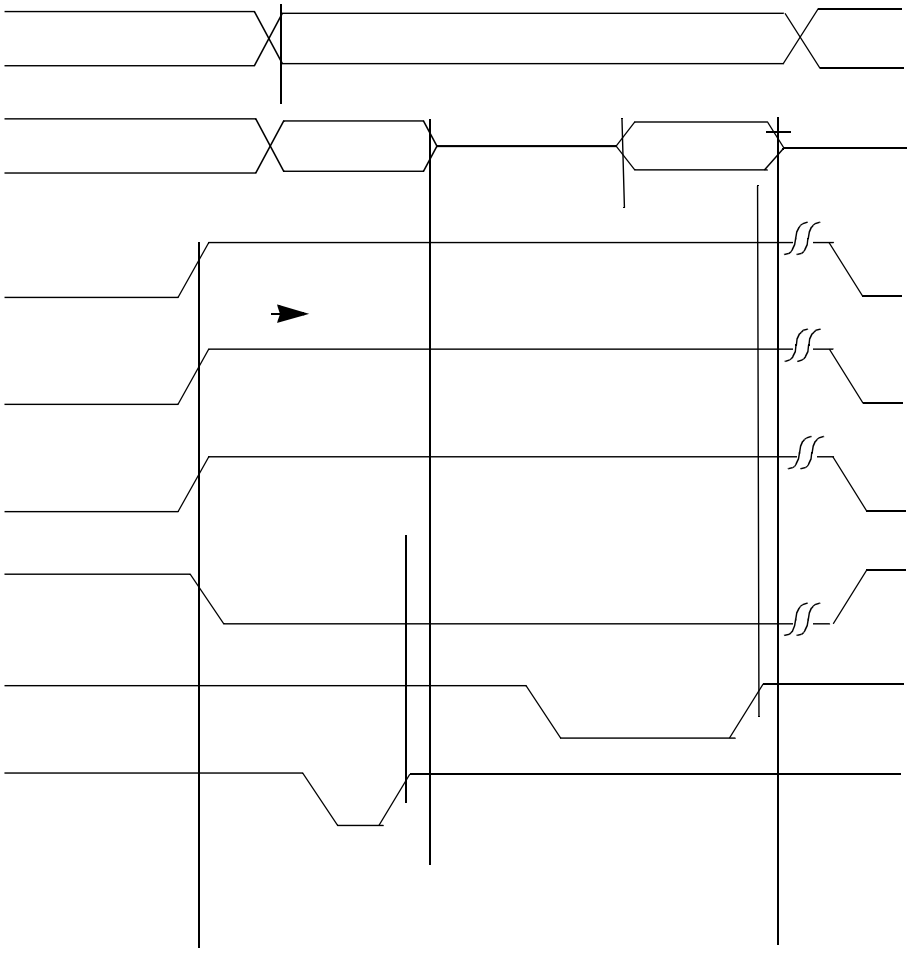

Figure 21. EPROM Program and Verify Timing

User Mode 3: PROM Verify

The Program Verify cycle is used as part of the intelligent programming algorithm to insure data integrity under worst-case conditions. It differs from the EPROM Read cycle in that V_{PP} is active and V_{CC} must be driven to 6.0V. Timing is shown in Figure 21.

User Modes 4 and 5: EPROM and RAM Protect

To extend program security, EPROM and RAM protect cycles are provided for the Z86E61/Z86E63 MCU. Execution of the EPROM protect cycle prohibits proper execution of the EPROM Read, EPROM Verify, and EPROM programming cycles. Execution of the RAM protect cycle disables accesses to the upper 128 bytes of register memory (excluding

mode and configuration registers), but first the user s program must set bit 6 of the IMR (R251). Timing is shown in Figure 22.

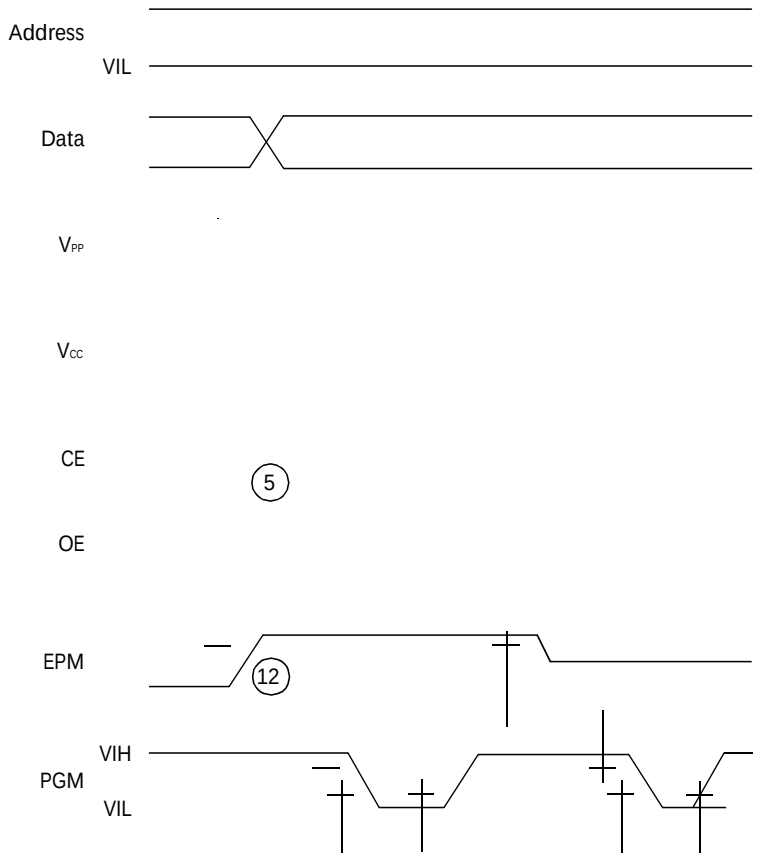

Figure 22. Programming EPROM and RAM Protect

Z86E63 Signal Description for EPROM Program/Read

The following signals are required to correctly program or read the Z86E63 device.

ADDR

The address must remain stable throughout the program read cycle. On both the Z86E61 and Z86E63 MCUs, all A0 A14 address lines must be driven at all times.

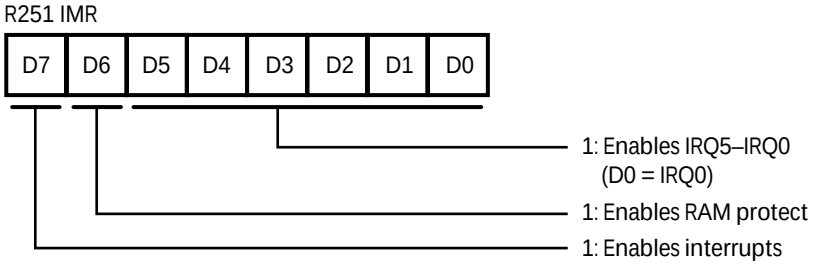

Figure 42. Interrupt Mask Register (FBH: Read/Write)

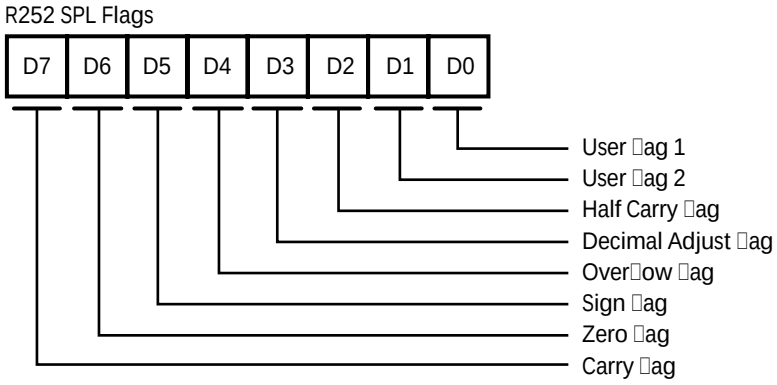

Figure 43. Flag Register (FCH: Read/Write)

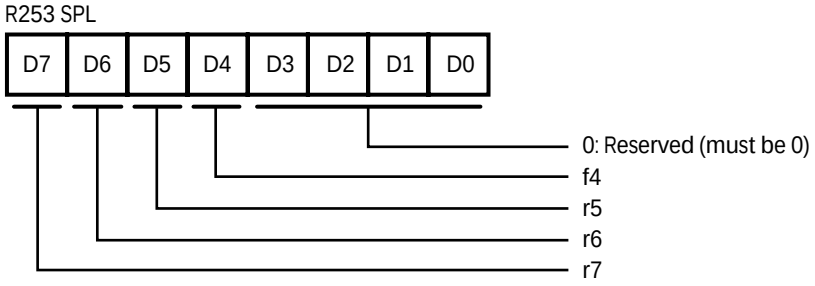

Figure 44. Register Pointer Register (FDH: Read/Write)

Z8 Instruction Set

This section discusses the addressing modes, symbols, flags, condition codes and instruction formats that apply to the Z8 instruction set. A summary of the Z8 instruction set follows on page 55.

The notations listed in Table 40 are used to describe addressing modes and instruction operations.

Table 40. Instruction Set Notation

Notation	Definition
IRR	Indirect register pair or indirect working register pair address.
Irr	Indirect working register pair only.
X	Indexed address.
DA	Direct address.
RA	Relative address.
IM	Immediate.
R	Register or working register address.
r	Working register address only.
IR	Indirect register or indirect working register address.
Ir	Indirect working register address only.
RR	Register pair or working register pair address.

The symbols listed in Table 41are used to describe the Z8 instruction set.

Table 41. Instruction Set Symbols

Symbol	Definition
dst	Destination location or contents.
src	Source location or contents.
cc	Condition code.
@	Indirect address prefix.
SP	Stack Pointer.
PC	Program Counter.
FLAGS	Flag Register (Control Register 252).
RP	Register Pointer (R253).
IMR	Interrupt Mask Register (R251).

Instruction Formats

Figure 47 shows the one-, two- and three-byte formats used in the Z8 instruction set.

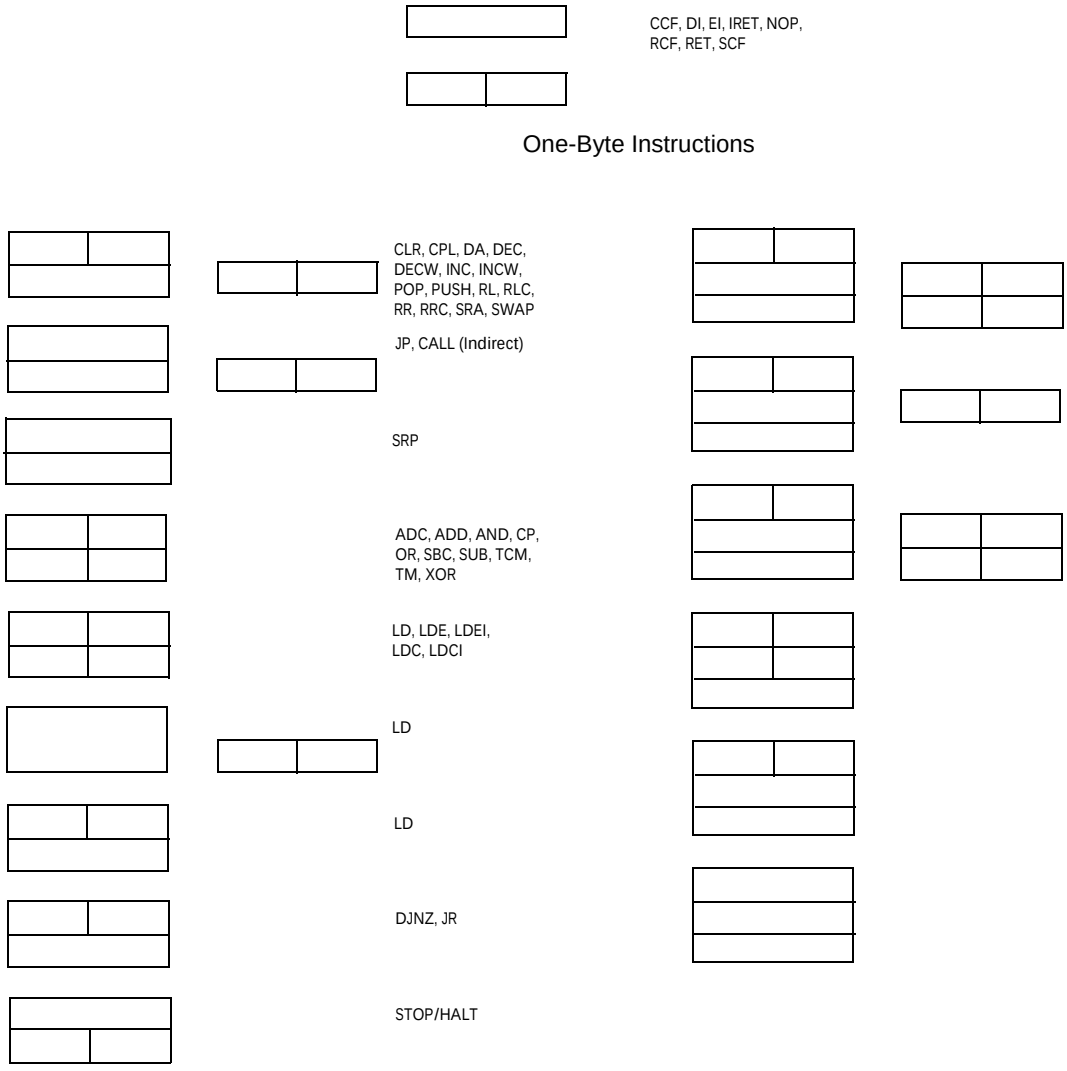

Figure 47. Instruction Formats

Instruction Summary

Table 45 summarizes each Z8 instruction by its operation, addressing mode, operation code, and the flag(s) each instruction affects.

Table 45. Instruction Summary

Instruction and Operation	Address Mode dst	Address Mode src	Op Code Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src♯ dst ← dst + src + C	See Note 1		1[]	*	*	*	*	0	*
ADD dst, src♯ dst ← dst + src	See Note 1		0[]	*	*	*	*	0	*
AND dst, src♯ dst ← dst AND src	See Note 1		5[]	–	*	*	0	–	—
CALL dst♯ SP ← SP – 2 @ SP ← PC, PC ← dst	DA IRR		06 D4	–	–	–	–	–	–
CCF♯ C ← NOT C			EF	*	–	–	–	–	–
CLR dst♯ dst ← 0	R IR		B0 B11	–	–	–	–	–	–
COM dst♯ dst ← NOT dst	R IR		60 61	–	*	*	0	–	–
CP dst, src♯ dst – src	See Note 1		A[]	*	*	*	*	–	–
DA dst♯ dst ← DA dst	R IR		40 41	*	*	*	X	–	–
DEC dst♯ dst ← dst – 1	R IR		00 01	–	*	*	*	–	–
DECW dst♯ dst ← dst – 1	R IR		80 81	–	*	*	*	–	–
DI♯ IMR(7) ← 0			8F	–	–	–	–	–	–

Note: These instructions have an identical set of addressing modes, which are encoded for brevity. The first Op Code nibble is found in this instruction set table. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found on the left of the applicable addressing mode pair in the Op Code Map in Figure 48.♯
♯
For example, the op code of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Packaging

Zilog s Z86E61 and Z86E63 MCUs are available in the following packages:

- 40-pin Plastic Dual Inline Package (PDIP)
- 44-pin Low-Profile Quad Flat Package (LQFP)
- 44-pin Plastic Chip Carrier (PLCC)#

Current diagrams for each of these packages are published in Zilog s Packaging Product Specification (PS0072), which is available free for download from the Zilog website.

Ordering Information

Order your Z86E61/Z86E63 MCU products from Zilog using the part numbers shown in Table 46. For more information about ordering, please consult your local Zilog sales office. The Sales Location page on the Zilog website lists all regional offices.

Table 46. Z86E61/Z86E63 MCU Ordering Matrix

Part Number	Frequency	Package	Temperature Range
Z86E61 MCU			
Z86E6116PSG	16MHz	40-pin PDIP	0°C to +70°C
Z86E6116VSG	16MHz	44-pin PLCC	0°C to +70°C
Z86E6116ASG	16MHz	44-pin LQFP	0°C to +70°C
Z86E6120PSG	20MHz	40-pin PDIP	0°C to +70°C
Z86E6120VSG	20MHz	44-pin PLCC	0°C to +70°C
Z86E6120ASG	20MHz	44-pin LQFP	0°C to +70°C
Z86E63 MCU			
Z86E6316PSG	16MHz	40-pin PDIP	0°C to +70°C
Z86E6316VSG	16MHz	44-pin PLCC	0°C to +70°C
Z86E6316ASG	16MHz	44-pin LQFP	0°C to +70°C
Z86E6320PSG	20MHz	40-pin PDIP	0°C to +70°C
Z86E6320VSG	20MHz	44-pin PLCC	0°C to +70°C
Z86E6320ASG	20MHz	44-pin LQFP	0°C to +70°C