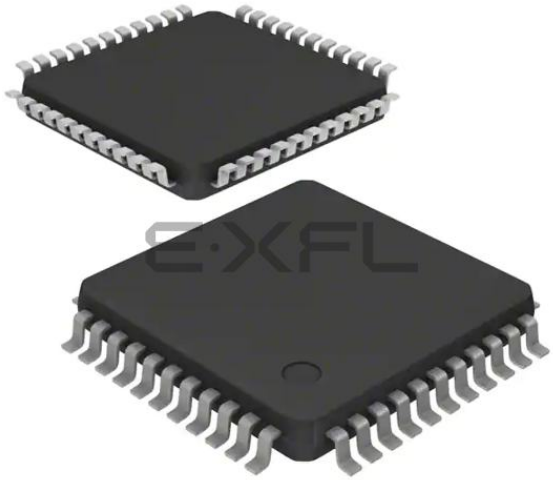

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e6116fsg

Overview

The Z86E61/Z86E63 microcontrollers are members of the Z8® single-chip microcontroller family with 16K/32KB of EPROM and 236 bytes of general-purpose RAM. Offered in 40-pin DIP, 44-pin PLCC or 44-pin LQFP package styles, these devices are pin-compatible EPROM versions of the Z86C61/ 63. The ROMless pin option is available on the 44-pin versions only.

With 16KB/32KB of ROM and 236 bytes of general-purpose RAM, the Z86E61/Z86E63 MCU offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

For applications demanding powerful I/O capabilities, the Z86E61/Z86E63 MCU offers 32 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

The Z86E61/Z86E63 MCU can address both external memory and preprogrammed ROM, making it well suited for high-volume applications or where code flexibility is required. There are three basic address spaces available to support this configuration:

- Program memory
- Data memory
- 236 General-purpose registers

Features

The Z86E61 and Z86E63 MCUs offer the following features:

- 8-Bit CMOS microcontroller
- 40-pin DIP, 44-pin PLCC and 44-pin LQFP packages
- 4.5V to 5.5V operating range
- Clock speeds: 16MHz and 20MHz
- Low power consumption: 275 mW (max)
- Two Standby modes: STOP and HALT
- 32 Input/Output lines
- Full-duplex UART
- All digital inputs are TTL levels

Figure 3 shows the pin-outs for the 40-pin PDIP EPROM Programming Mode package; Table 26 describes each pin.

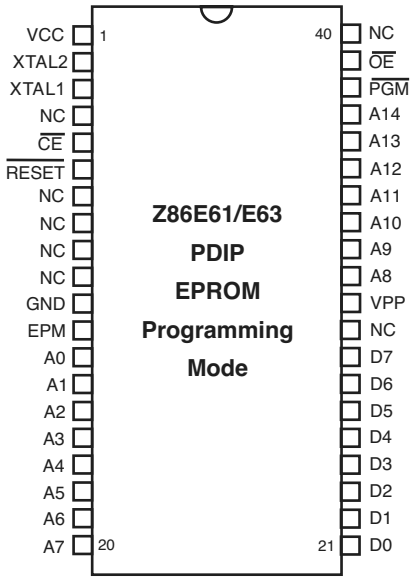

Figure 3. Z86E61/Z86E63 PDIP Pin Diagram, EPROM Programming Mode

Table 26. Z86E61/Z86E63 PDIP Pin Description, EPROM Programming Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{CE}$	Chip Enable	Input
$\overline{RESET}$	Reset	Input
EPM	EPROM Programming Mode	Input
A0–A14	15-bit Address Bus	Input
D7–D0	8-bit Data Bus	Input/Output
V_{PP}	Programming Voltage	Input
$\overline{PGM}$	Programming Mode	Input
$\overline{OE}$	Output Enable	Input
NC	Not Connected	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Figure 5 shows the pin-outs for the 44-pin LQFP EPROM Programming Mode package; Table 28 describes each pin.

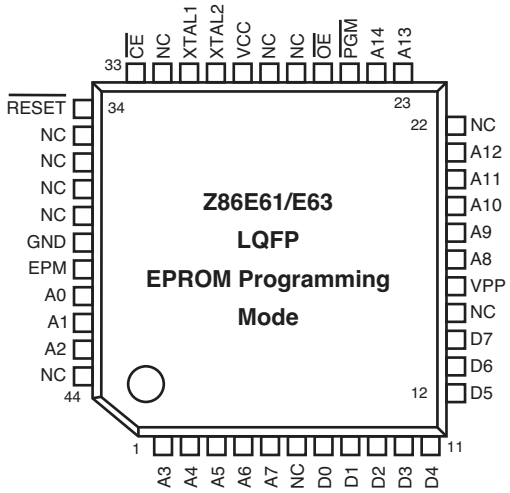

Figure 5. Z86E61/Z86E63 LQFP Pin Diagram, EPROM Programming Mode

Table 28. Z86E61/Z86E63 LQFP Pin Description, EPROM Programming Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{CE}$	Chip Enable	Input
$\overline{RESET}$	Reset	Input
EPM	EPROM Programming Mode	Input
A0–A14	15-bit Address Bus	Input
D7–D0	8-bit Data Bus	Input/Output
V_{PP}	Programming Voltage	Input
$\overline{PGM}$	Programming Mode	Input
$\overline{OE}$	Output Enable	Input
NC	Not Connected	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Figure 7 shows the pin-outs for the 44-pin PLCC EPROM Programming Mode package; Table 30 describes each pin.

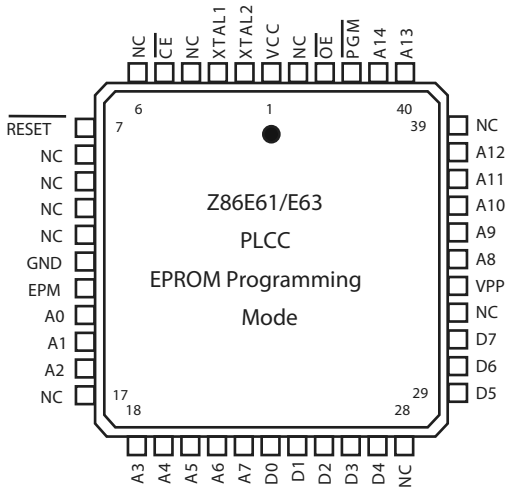

Figure 7. Z86E61/Z86E63 PLCC Pin Diagram, EPROM Programming Mode

Table 30. Z86E61/Z86E63 PLCC Pin Description, EPROM Programming Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{CE}$	Chip Enable	Input
$\overline{RESET}$	Reset	Input
EPM	EPROM Programming Mode	Input
A0–A14	15-bit Address Bus	Input
D7–D0	8-bit Data Bus	Input/Output
V_{PP}	Programming Voltage	Input
$\overline{PGM}$	Programming Mode	Input
$\overline{OE}$	Output Enable	Input
NC	Not Connected	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Port 0 (P07–P00)

Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07–P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 can provide address bits A11–A8 (lower nibble) or A15–A8 (lower and upper nibbles) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode Register.

In ROMless Mode, after a hardware reset, the Port 0 lines are defined as address lines A15–A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode; see Figure 8.

open-drain output. Port 2 is always available for I/ 0 operation. When used as an I/0 port, Port 2 can be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines DAV2 and RDY2. The handshake signal assignment for Port 3 lines, P31 and P36, is dictated by the direction (input or output) assigned to P27; see Figure 10 and Table 31 on page 16).

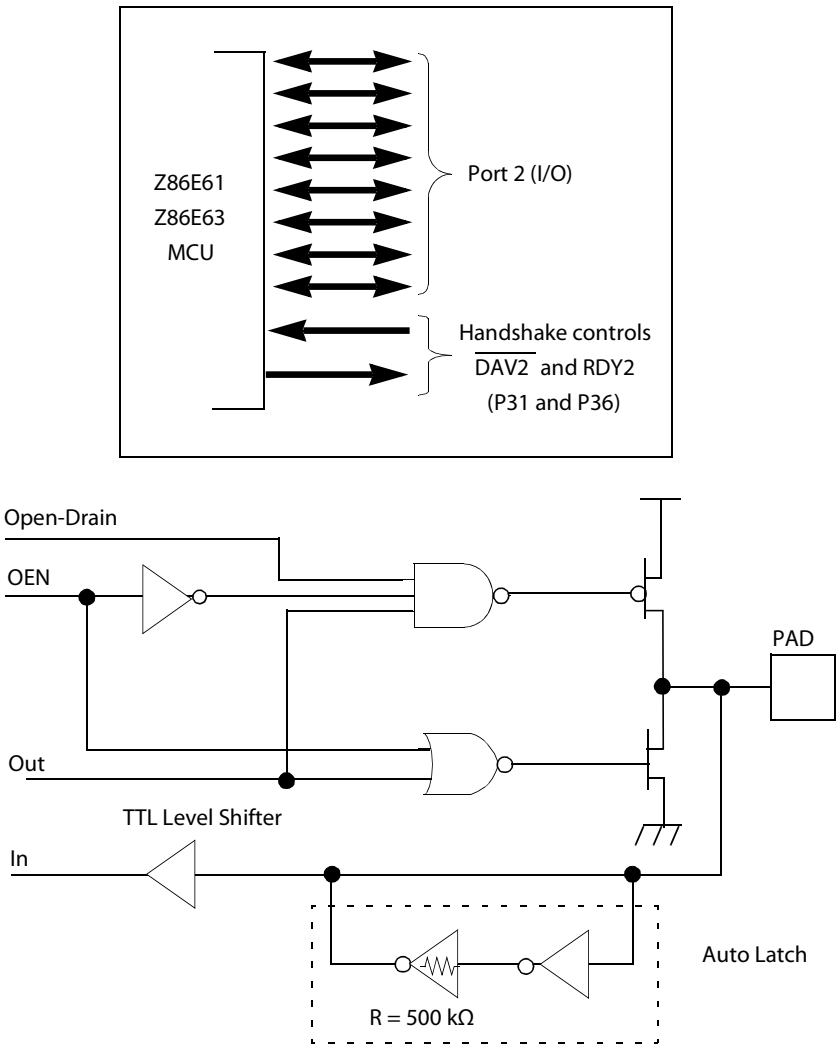

Figure 10. Port 2 Configuration

Address Space

This section describes the memory and addressing functions of the Z86E61/Z86E63 MCU.

Program Memory

The Z86E61/Z86E63 MCU can address 48KB (Z86E61) or 32KB (Z86E63) of external program memory; see Figure 13. The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM Mode, byte 13 to byte 16383 (Z86E61) or 32767 (Z86E63) consists of on-chip EPROM. At addresses 16384 (Z86E61) or 32768 (Z86E63) and above, the Z86E61/Z86E63 MCU executes external program memory fetches. In ROMless Mode, the Z86E61/Z86E63 MCU can address up to 64KB of program memory. Program execution begins at external location 000C (HEX) after a reset.

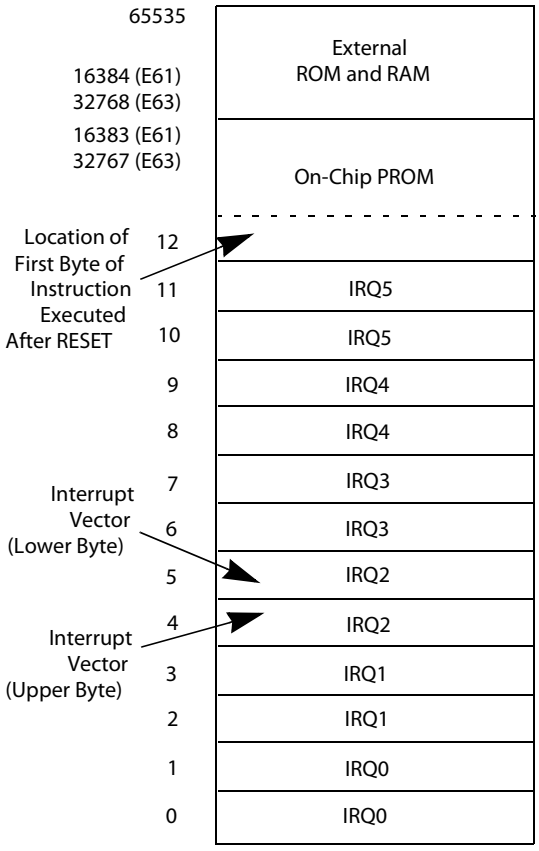

Figure 13. Program Memory Configuration

Data Memory

The EPROM version can address up to 48KB (Z86E61) or 32KB (Z86E63) of external data memory (DM) space beginning at location 16384 (Z86E61) or 32768 (Z86E63). The ROMless version can address up to 64KB of external data memory. External data memory may be included with, or separated from, the external program memory space. DM, an optional I/0 function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space; see Figure 14. The state of the DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (DM inactive) memory, and an LDE instruction references DATA (DM active Low) memory.

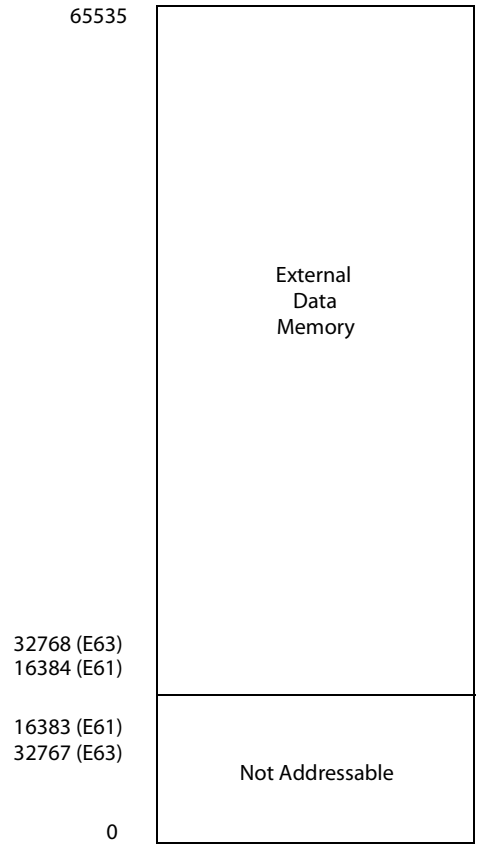

Figure 14. Data Memory Configuration

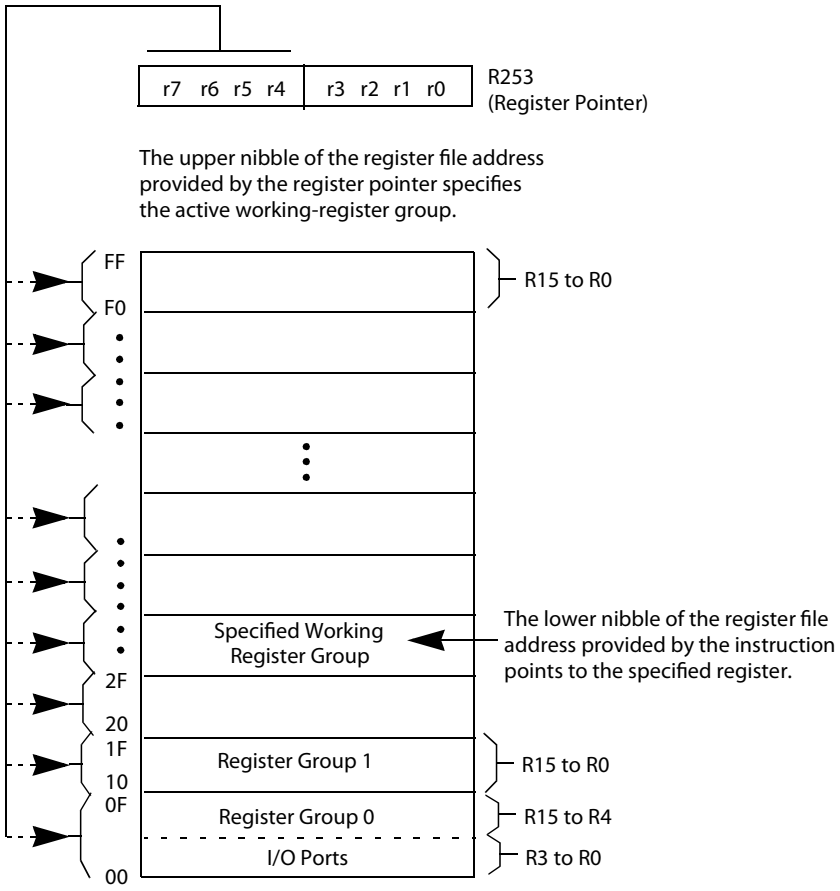

Figure 16. Register Pointer

Stack

The Z86E61/Z86E63 MCU has a 16-bit Stack Pointer (R255–R254) used for external stacks that reside anywhere in the data memory for the ROMless Mode, but only from 16384 (Z86E61) or 32768 (Z86E63) to 65535 in the EPROM Mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R239–R4). The high byte of the Stack Pointer (SPH Bits 15–8) can be use as a general-purpose register when using internal stack only.

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counters and prescalers reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter is programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (Single Pass Mode) or to automatically reload the initial value and continue counting (Modulo-n Continuous Mode).

The counter, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode Register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 also serves as a timer output (T_{OUT}) through which T0, T1, or the internal clock can be output. The counter/timers are cascaded by connecting the T0 output to the input of T1.

Interrupts

The Z86E61/Z86E63 MCU has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follows: four sources are claimed by Port 3 lines P33–P30, one in Serial Out, one in Serial In, and two in the counter/timers; see Figure 18. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register; see Figure 40 on page 48.

All Z86E61/Z86E63 MCU interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request Register is polled to determine which of the interrupt requests need service. Software initialized interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

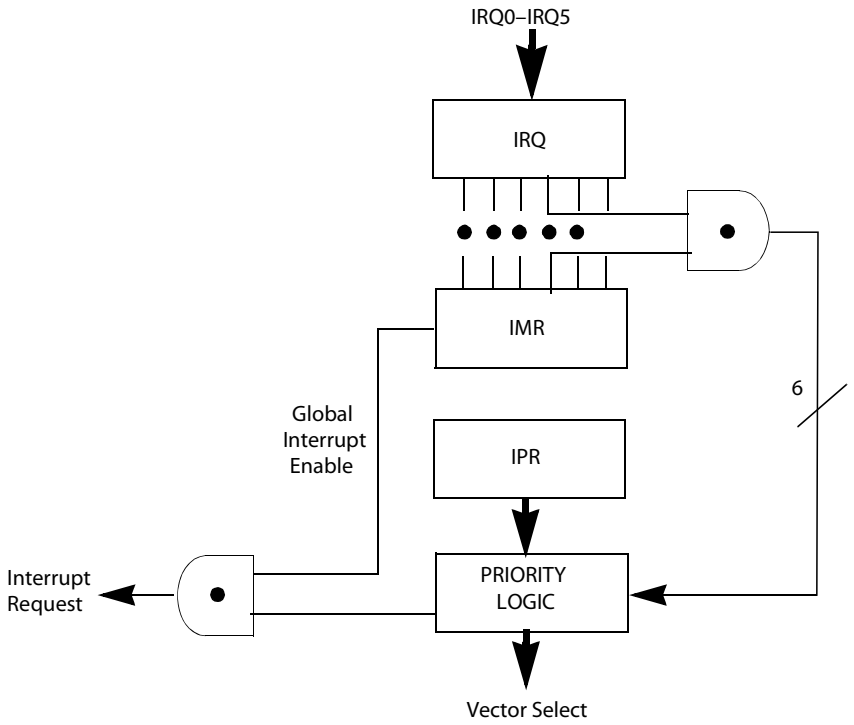

Figure 18. Interrupt Block Diagram

For the ROMless Mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the Flag Register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

Clock

The Z86E61/Z86E63 MCU's on-chip oscillator features a high gain, parallel resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 20 MHz max; series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF < CL < 100 pF) from each pin to ground; see Figure 19.

Programming

This section describes the five user program modes available for programming the Z86E61/Z86E63 MCU, including signal descriptions for programming or reading the Z86E63 device.

Z86E61/Z86E63 User Modes

The Z86E61/Z86E63 MCU uses separate AC timing cycles for the different user modes available. Table 32 shows the Z86E61/Z86E63 MCU's user modes; Table 33 shows the timing of the programming waveforms.

Table 32. OTP Programming[1]

User/Test Mode	Device Pins							
Device Pin No.	P33	P32	P30	P31	P20			Port 1 Config Data
User Modes	V_{PP}	EPM	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	ADDR	V_{CC}	
EPROM Read	Z[2]	V_H[3]	V_{IL}[4]	V_{IL}	V_{IH}	Addr	5.0V	Out
Program	V_{PP}[5]	V_{IH}	V_{IL}	V_{IH}[6]	V_{IL}	Addr	6.0V	In
Program Verify	V_{PP}[5]	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Addr	6.0V	Out
EPROM Protect	V_{PP}[5]	V_H	V_H	V_{IH}	V_{IL}	X[7]	6.0V	X
RAM Protect	V_{PP}	V_{IH}	V_H	V_{IH}	V_{IL}	X	6.0V	X

Notes:
1. I_{PP} during programming = 40 mA maximum; I_{CC} during programming, verify or read = 40 mA maximum.
2. Z = V_{IL} or V_{IH}.
3. V_H = 12.0 ± 0.5V.
4. V_{IL} = 0V.
5. V_{PP} = 12.0 ± 0.5V.
6. V_{IH} = 5V.
7. X = Not used in this mode.

Table 33. Timing of Programming Waveforms

Parameters	Name	Min	Max	Unit
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup Time	2		µs
4	V_{CC} Setup time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		µs

Table 33. Timing of Programming Waveforms (Continued)

Parameters	Name	Min	Max	Unit
7	Data Hold Time	2		µs
8	$\overline{OE}$ Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	$\overline{PGM}$ Setup Time	2		µs
14	Address to $\overline{OE}$ Setup Time	2		µs
15	Option Program Pulse Width	78		ms

User MODE 1: EPROM Read

The Z86E61/Z86E63 EPROM read cycle is provided so that the user may read the Z86E61/Z86E63 MCU as a standard 27128 (Z86E61) or 27256 (Z86E63) EPROM. This is accomplished by driving the EPM pin (P32) to V_H and activating CE and OE. PGM remains inactive. This mode is not valid after execution of an EPROM protect cycle.

Timing for the EPROM read cycle is shown in Figure 20.

DATA

The I/O data bus must be stable during programming (OE High, PGM Low, V_{PP} High). During read the data bus outputs data.

XCLK

A clock is required to clock the RESET signal into the registers before programming. A constant clock can be applied, or the XCLK input can be toggled a minimum of 12 cycles before any programming or verify function begins. The maximum clock frequency to be applied when in the EPROM Mode is 12 MHz.

RESET. The reset input can be held to a constant Low or High value throughout normal programming. It must be held High to program the EPROM protect option bit. Also, any time the RESET input changes state the XCLK must be clocked a minimum of 12 times to clock the RESET through the reset filter.

OE. When the device is placed in EPROM Mode, the OE input also serves as the pre-charge for the sense amp. The precharge signal should be Low for the first half of the stable address and High for the second half. The PRECHG signal is inverted from the OE signal so the OE should be High on the first half and Low on the second half, or stable address. The EPROM output data should be sampled during the second half of stable address.

The access time of the EPROM is defined in later sections. This two part calculation of access time is required because this is a precharged sense amp with a precharge clock.

Programming Flow

Figure 23 shows the steps for programming the Z86E61/Z86E63 MCU.

Absolute Maximum Ratings

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Table 34 lists the absolute maximum ratings of the Z86E61/Z86E63 MCU.

Table 34. Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
V_{CC}	Supply Voltage[1]	–0.3	+7.0	V
T_{STG}	Storage Temperature	–65	+150	°C
T_A	Operating Ambient Temperature		See Note 2	°C

Notes:
1. Voltages on all pins with respect to GND.
2. See Ordering Information on page 60.

Standard Test Conditions

The characteristics described in this document apply to standard test conditions, as noted. All voltages are referenced to GND, and positive current flows into the referenced pin; see Figure 24.

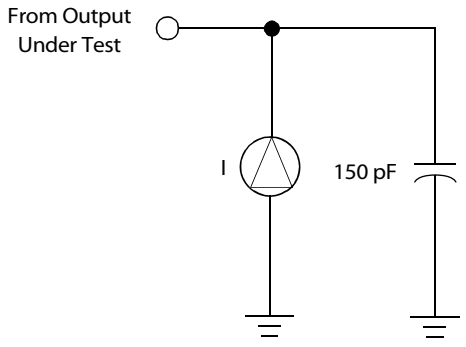

Figure 24. Test Load Diagram

Table 39. Additional Timing (Continued)

			TA = 0°C to +70°C					
			16MHz[1]		20MHz			
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
8A	TwIL	Interrupt Request Input Low Times	70		50		ns	2,3
8B	TwIL	Interrupt Request Input Low Times	5TpC		5TpC			2,4
9	TwIH	Interrupt Request Input High Times	5TpC		5TpC			2,5

Notes:
1. Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
3. Interrupt request through Port 3 (P33–P31).
4. Interrupt request through Port 30.
5. Interrupt references request through Port 3.

Table 44. Condition Codes (Continued)

Value	Mnemonic	Definition	Flags Set
0111	ULT	Unsigned Less Than	C = 1
1000		Always True	
1001	GE	Greater Than Or Equal To	(S XOR V) = 0
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
1100	NOV	No Overflow	V = 0
1101	PL	Plus	S = 0
1110	NE	Not Equal	Z = 0
1110	NZ	Not Zero	Z = 0
1111	NC	No Carry	C = 0
1111	UGE	Unsigned Greater Than Or Equal To	C = 0

Instruction Formats

Figure 47 shows the one-, two- and three-byte formats used in the Z8 instruction set.

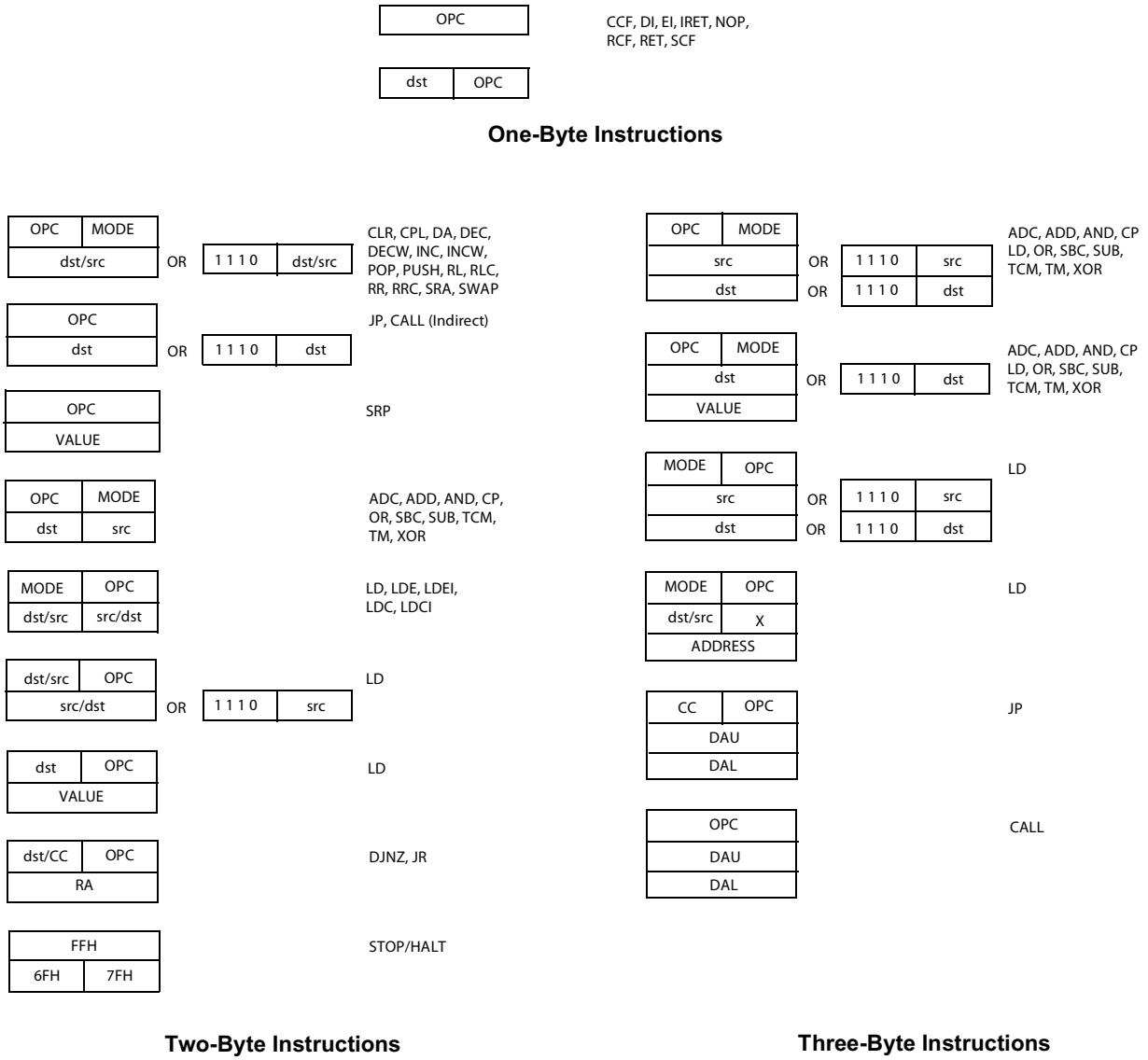

Figure 47. Instruction Formats

Table 45. Instruction Summary (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Op Code Byte (Hex)	Flags Affected C	Z	S	V	D	H
DJNZ r, dst r ← r – 1 if r ≠ 0 PC ← PC + dst Range: +127, –128	RA		rA r = 0 – F	–	–	–	–	–	–
EI IRM(7) ← 1			BF	*	*	*	*	*	*
HALT			7F	–	–	–	–	–	–
INC dst dst ← dst + 1	r R IR		rE r = 0 – F 20 21	–	*	*	*	–	–
INCW dst dst ← dst + 1	RR IR		A0 A1	–	*	*	*	–	–
IRET FLAGS ← @SP; SP ← SP + 1 PC ← @SP; SP ← SP + 2; IMR(7) ← 1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC ← dst	DA IRR		cD c = 0 – F 30	–	–	–	–	–	–
JR cc, dst if cc is true, PC ← PC + dst Range: +127, –128	RA		cB c = 0 – F	–	–	–	–	–	–

Note: These instructions have an identical set of addressing modes, which are encoded for brevity. The first Op Code nibble is found in this instruction set table. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found on the left of the applicable addressing mode pair in the Op Code Map in Figure 48.

For example, the op code of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Packaging

Zilog's Z86E61 and Z86E63 MCUs are available in the following packages:

- 40-pin Plastic Dual Inline Package (PDIP)
- 44-pin Low-Profile Quad Flat Package (LQFP)
- 44-pin Plastic Chip Carrier (PLCC)

Current diagrams for each of these packages are published in Zilog's Packaging Product Specification (PS0072), which is available free for download from the Zilog website.

Ordering Information

Order your Z86E61/Z86E63 MCU products from Zilog using the part numbers shown in Table 46. For more information about ordering, please consult your local Zilog sales office. The Sales Location page on the Zilog website lists all regional offices.

Table 46. Z86E61/Z86E63 MCU Ordering Matrix

Part Number	Frequency	Package	Temperature Range
Z86E61 MCU			
Z86E6116PSG	16MHz	40-pin PDIP	0°C to +70°C
Z86E6116VSG	16MHz	44-pin PLCC	0°C to +70°C
Z86E6116ASG	16MHz	44-pin LQFP	0°C to +70°C
Z86E6120PSG	20MHz	40-pin PDIP	0°C to +70°C
Z86E6120VSG	20MHz	44-pin PLCC	0°C to +70°C
Z86E6120ASG	20MHz	44-pin LQFP	0°C to +70°C
Z86E63 MCU			
Z86E6316PSG	16MHz	40-pin PDIP	0°C to +70°C
Z86E6316VSG	16MHz	44-pin PLCC	0°C to +70°C
Z86E6316ASG	16MHz	44-pin LQFP	0°C to +70°C
Z86E6320PSG	20MHz	40-pin PDIP	0°C to +70°C
Z86E6320VSG	20MHz	44-pin PLCC	0°C to +70°C
Z86E6320ASG	20MHz	44-pin LQFP	0°C to +70°C