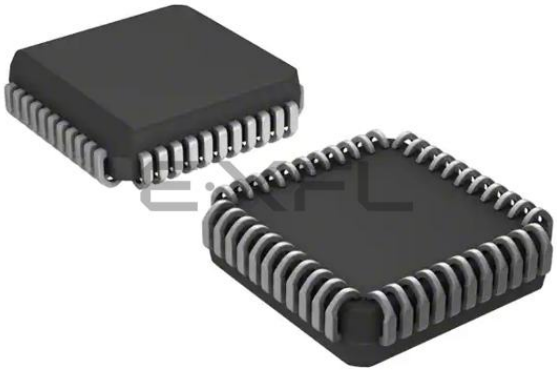

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e6116vsg

Customer Support 62

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Pin Functions

The Z86E61/Z86E63 MCU is available in variety of package styles, programming modes and pin configurations. This section describes the pin signals and configurations for each of the 40-pin PDIP, 44-pin PLCC and 44-pin LQFP packages in both Standard and EPROM Programming modes.

Pin Signals

Figure 2 shows the pin-outs for the 40-pin PDIP Standard Mode package; Table 25 describes each pin.

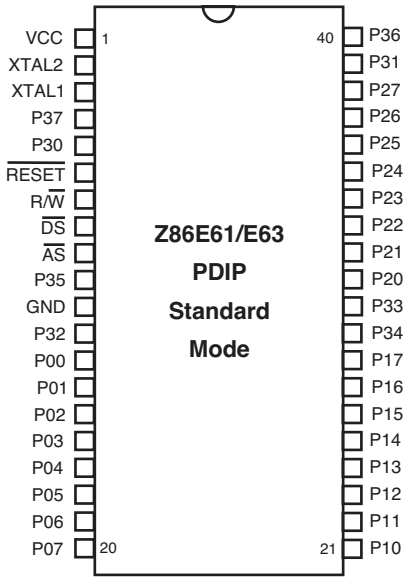

Figure 2. Z86E61/Z86E63 PDIP Pin Diagram, Standard Mode

Table 25. Z86E61/Z86E63 PDIP Pin Description, Standard Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{RESET}}$	Reset	Input
R/$\overline{\text{W}}$	Read/Write	Output

open-drain output. Port 2 is always available for I/ 0 operation. When used as an I/0 port, Port 2 can be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines DAV2 and RDY2. The handshake signal assignment for Port 3 lines, P31 and P36, is dictated by the direction (input or output) assigned to P27; see Figure 10 and Table 31 on page 16).

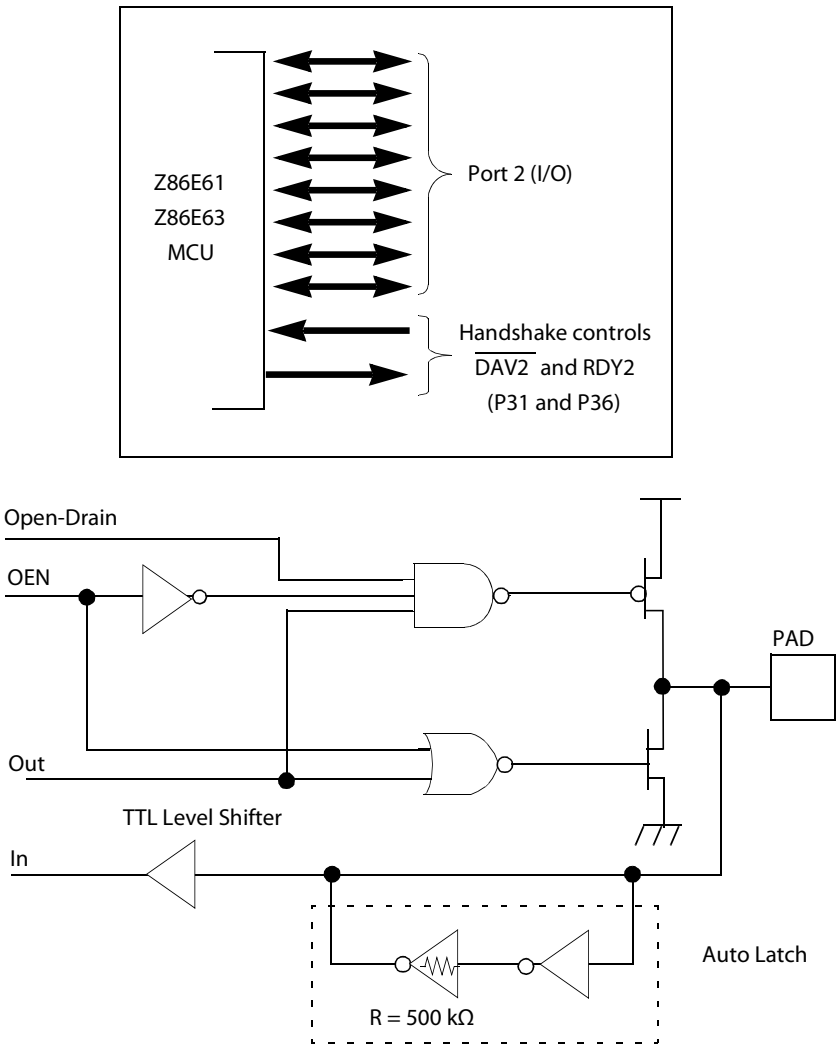

Figure 10. Port 2 Configuration

Address Space

This section describes the memory and addressing functions of the Z86E61/Z86E63 MCU.

Program Memory

The Z86E61/Z86E63 MCU can address 48KB (Z86E61) or 32KB (Z86E63) of external program memory; see Figure 13. The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM Mode, byte 13 to byte 16383 (Z86E61) or 32767 (Z86E63) consists of on-chip EPROM. At addresses 16384 (Z86E61) or 32768 (Z86E63) and above, the Z86E61/Z86E63 MCU executes external program memory fetches. In ROMless Mode, the Z86E61/Z86E63 MCU can address up to 64KB of program memory. Program execution begins at external location 000C (HEX) after a reset.

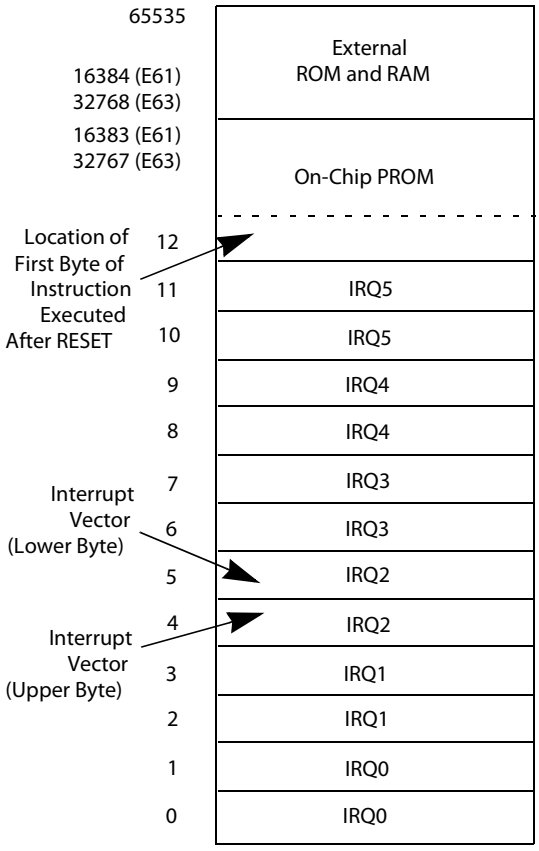

Figure 13. Program Memory Configuration

Register File

The register file consists of four I/0 port registers, 236 general-purpose registers, and 16 control and status registers, as shown in Figure 15. The instructions can access registers directly or indirectly through an 8-bit address field. The Z86E61/Z86E63 MCU also allows short 4-bit register addressing using the Register Pointer, which is shown in Figure 16. In 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

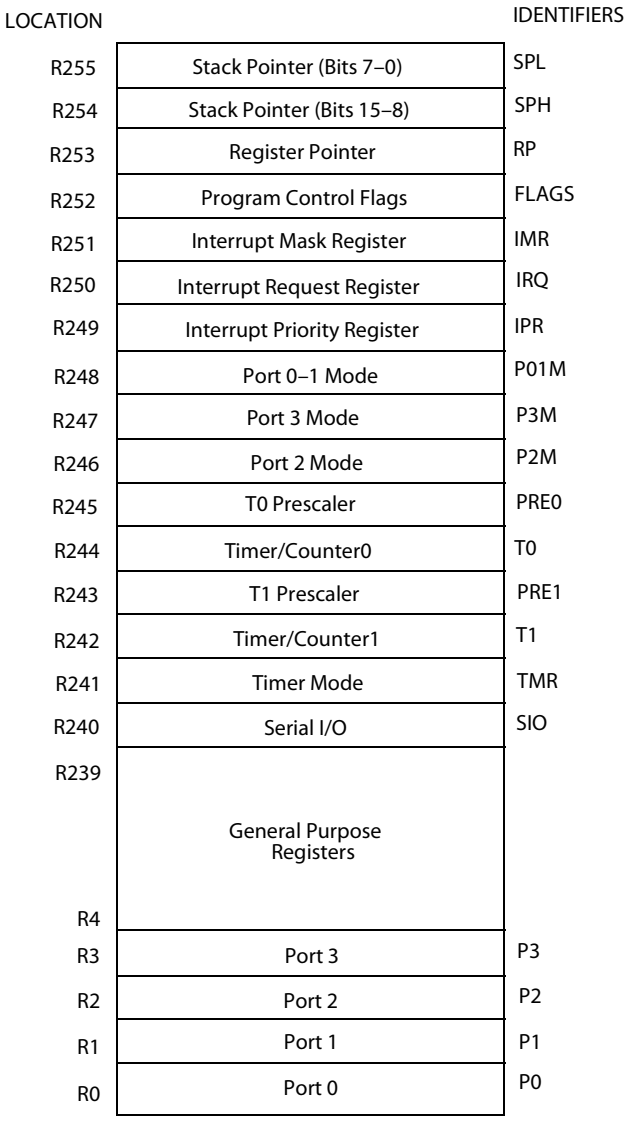

Figure 15. Register File

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counters and prescalers reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter is programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (Single Pass Mode) or to automatically reload the initial value and continue counting (Modulo-n Continuous Mode).

The counter, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode Register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 also serves as a timer output (T_{OUT}) through which T0, T1, or the internal clock can be output. The counter/timers are cascaded by connecting the T0 output to the input of T1.

Interrupts

The Z86E61/Z86E63 MCU has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follows: four sources are claimed by Port 3 lines P33–P30, one in Serial Out, one in Serial In, and two in the counter/timers; see Figure 18. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register; see Figure 40 on page 48.

All Z86E61/Z86E63 MCU interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request Register is polled to determine which of the interrupt requests need service. Software initialized interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

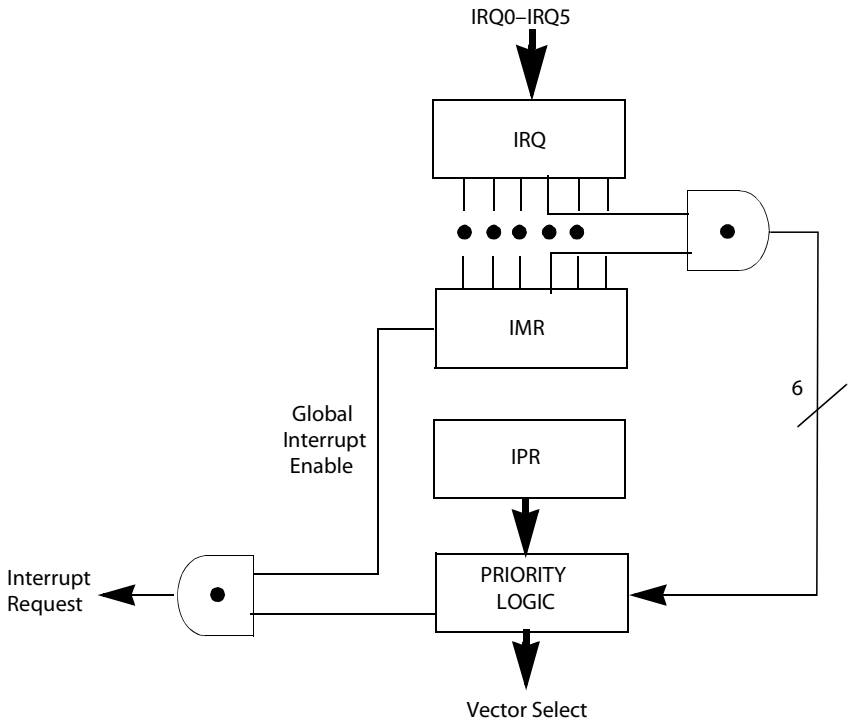

Figure 18. Interrupt Block Diagram

For the ROMless Mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the Flag Register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

Clock

The Z86E61/Z86E63 MCU's on-chip oscillator features a high gain, parallel resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 20 MHz max; series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF < CL < 100 pF) from each pin to ground; see Figure 19.

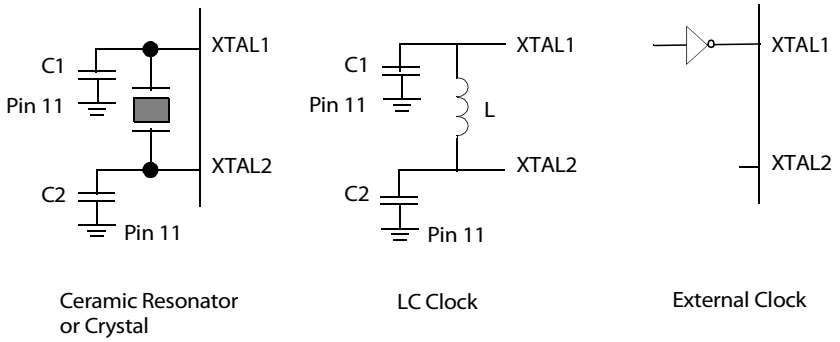

Figure 19. Oscillator Configuration

Note: The actual capacitor value is specified by the crystal manufacturer.

HALT

Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP

This instruction turns off the internal clock and external crystal oscillation, and reduces the standby current to 5µA (typical) or less. The STOP Mode is terminated by a reset, which causes the processor to restart the application program at address 000Ch.

To enter STOP (or HALT) Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = 0FFH) immediately before the appropriate SLEEP instruction, as shown in the following code segment.

```
FF          NOP         ; clear the pipeline
6F          STOP        ; enter STOP Mode
 or
FF          NOP         ; clear the pipeline
7F          HALT        ; enter HALT Mode
```

Programming

This section describes the five user program modes available for programming the Z86E61/Z86E63 MCU, including signal descriptions for programming or reading the Z86E63 device.

Z86E61/Z86E63 User Modes

The Z86E61/Z86E63 MCU uses separate AC timing cycles for the different user modes available. Table 32 shows the Z86E61/Z86E63 MCU's user modes; Table 33 shows the timing of the programming waveforms.

Table 32. OTP Programming[1]

User/Test Mode	Device Pins							
Device Pin No.	P33	P32	P30	P31	P20			Port 1 Config Data
User Modes	V_{PP}	EPM	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	ADDR	V_{CC}	
EPROM Read	Z[2]	V_H[3]	V_{IL}[4]	V_{IL}	V_{IH}	Addr	5.0V	Out
Program	V_{PP}[5]	V_{IH}	V_{IL}	V_{IH}[6]	V_{IL}	Addr	6.0V	In
Program Verify	V_{PP}[5]	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Addr	6.0V	Out
EPROM Protect	V_{PP}[5]	V_H	V_H	V_{IH}	V_{IL}	X[7]	6.0V	X
RAM Protect	V_{PP}	V_{IH}	V_H	V_{IH}	V_{IL}	X	6.0V	X

Notes:
1. I_{PP} during programming = 40 mA maximum; I_{CC} during programming, verify or read = 40 mA maximum.
2. Z = V_{IL} or V_{IH}.
3. V_H = 12.0 ± 0.5V.
4. V_{IL} = 0V.
5. V_{PP} = 12.0 ± 0.5V.
6. V_{IH} = 5V.
7. X = Not used in this mode.

Table 33. Timing of Programming Waveforms

Parameters	Name	Min	Max	Unit
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup Time	2		µs
4	V_{CC} Setup time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		µs

DATA

The I/O data bus must be stable during programming (OE High, PGM Low, V_{PP} High). During read the data bus outputs data.

XCLK

A clock is required to clock the RESET signal into the registers before programming. A constant clock can be applied, or the XCLK input can be toggled a minimum of 12 cycles before any programming or verify function begins. The maximum clock frequency to be applied when in the EPROM Mode is 12 MHz.

RESET. The reset input can be held to a constant Low or High value throughout normal programming. It must be held High to program the EPROM protect option bit. Also, any time the RESET input changes state the XCLK must be clocked a minimum of 12 times to clock the RESET through the reset filter.

OE. When the device is placed in EPROM Mode, the OE input also serves as the pre-charge for the sense amp. The precharge signal should be Low for the first half of the stable address and High for the second half. The PRECHG signal is inverted from the OE signal so the OE should be High on the first half and Low on the second half, or stable address. The EPROM output data should be sampled during the second half of stable address.

The access time of the EPROM is defined in later sections. This two part calculation of access time is required because this is a precharged sense amp with a precharge clock.

Programming Flow

Figure 23 shows the steps for programming the Z86E61/Z86E63 MCU.

AC Characteristics

Figure 27 displays the timing characteristics for the Z86E61/Z86E63 MCU. The circled numbers in this figure reference a description in Table 36 of each symbol, its parameter and its frequency range for these 16MHz and 20MHz parts.

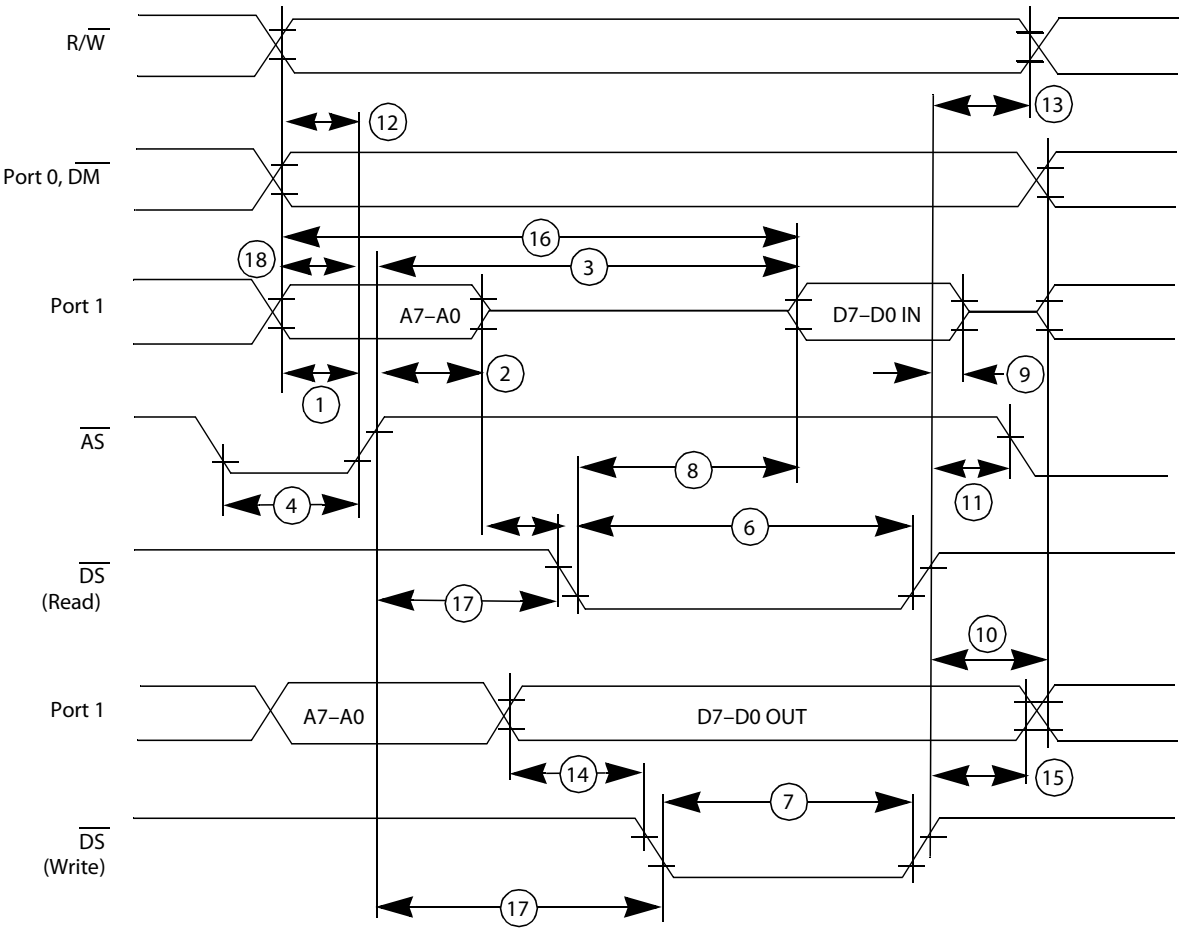

Figure 27. External I/O or Memory Read/Write Timing

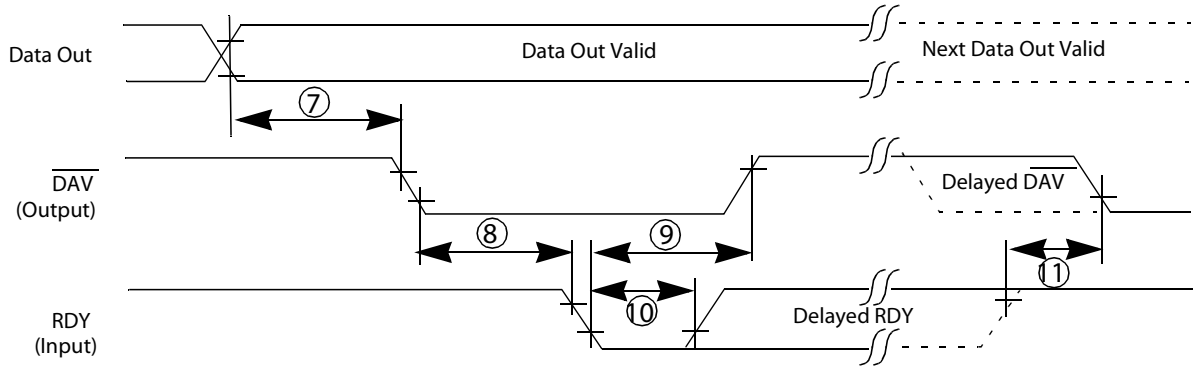

Figure 29. Output Handshake Timing

Table 38. Handshake Timing

			TA = 0°C to +70°				
			16MHz		20MHz		Data
No.	Symbol	Parameter	Min	Max	Min	Max	Direction
1	TsDI(DAV)	Data In Setup Time	0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		IN
3	TwDAV	Data Available Width	110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay		115		115	IN
6	TdRDY0(DAV)	RDY Rise to DAV Fall Delay	0		0		IN
7	TdD0(DAV)	Data Out to DAV Fall Delay		TpC		TpC	OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay		115		115	OUT
10	TwRDY	RDY Width	110		110		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay		115		115	OUT

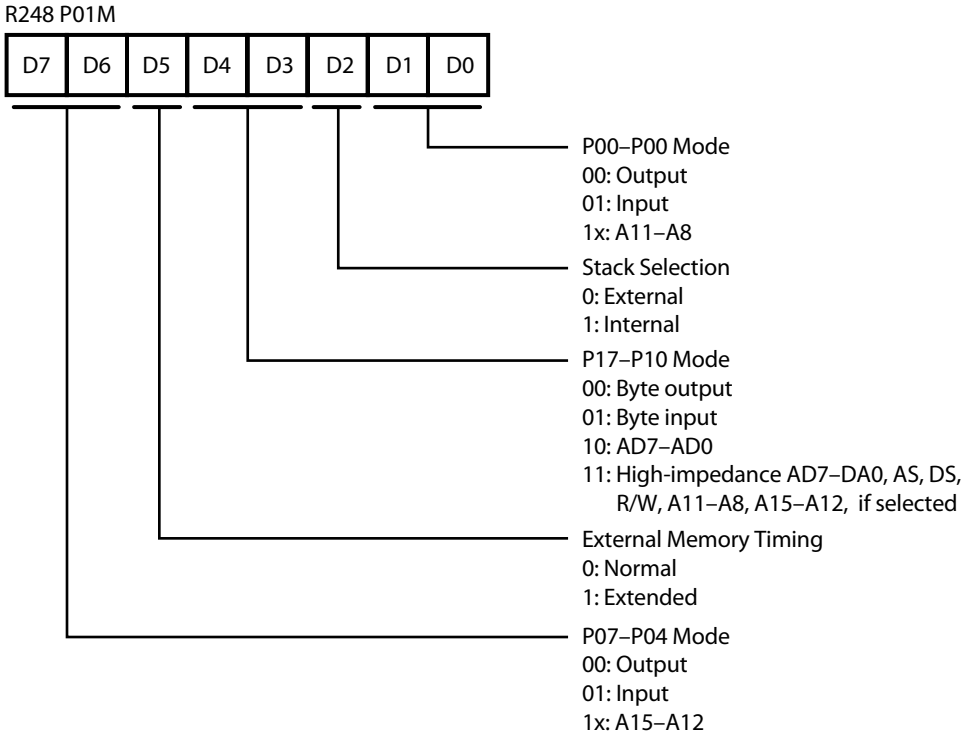

Figure 39. Port 0 and 1 Mode Register (F8H: Write Only)

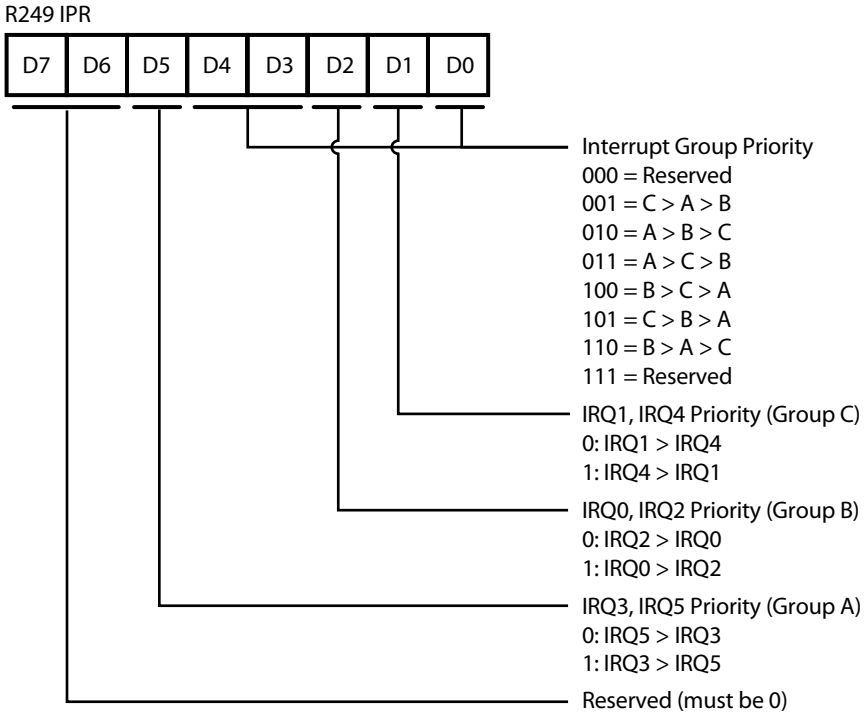

Figure 40. Interrupt Priority Register (F9H: Write Only)

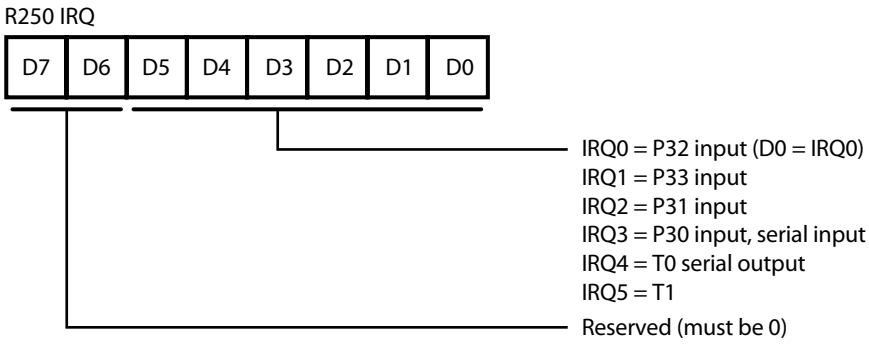

Figure 41. Interrupt Request Register (FAH: Read/Write)

Z8 Instruction Set

This section discusses the addressing modes, symbols, flags, condition codes and instruction formats that apply to the Z8 instruction set. A summary of the Z8 instruction set follows on page 55.

The notations listed in Table 40 are used to describe addressing modes and instruction operations.

Table 40. Instruction Set Notation

Notation	Definition
IRR	Indirect register pair or indirect working register pair address.
Irr	Indirect working register pair only.
X	Indexed address.
DA	Direct address.
RA	Relative address.
IM	Immediate.
R	Register or working register address.
r	Working register address only.
IR	Indirect register or indirect working register address.
Ir	Indirect working register address only.
RR	Register pair or working register pair address.

The symbols listed in Table 41are used to describe the Z8 instruction set.

Table 41. Instruction Set Symbols

Symbol	Definition
dst	Destination location or contents.
src	Source location or contents.
cc	Condition code.
@	Indirect address prefix.
SP	Stack Pointer.
PC	Program Counter.
FLAGS	Flag Register (Control Register 252).
RP	Register Pointer (R253).
IMR	Interrupt Mask Register (R251).

Control Register R252 contains the six flags shown in Table 42.

Table 42. R252 Flags

Symbol	Definition
C	Carry flag.
Z	Zero flag.
S	Sign flag.
V	Overflow flag.
D	Decimal Adjust flag.
H	Half Carry flag.

The flags in Table 42 can be affected by the symbols defined in Table 43.

Table 43. R252 Flags

Symbol	Definition
0	Clear to zero.
1	Set to one.
*	Set to clear according to operation.
–	Unaffected.
x	Undefined.

Table 44 defines the flags that are set for each condition code value.

Table 44. Condition Codes

Value	Mnemonic	Definition	Flags Set
0000	F	Never True (Always False)	
0001	LT	Less Than	(S XOR V) = 1
0010	LE	Less Than Or Equal To	[Z OR (S XOR V)] = 1
0011	ULE	Unsigned Less Than Or Equal	(C OR Z) = 1
0100	OV	Overflow	V = 0
0101	MI	Minus	S = 1
0110	EQ	Equal	Z = 1
0110	Z	Zero	Z = 1
0111	C	Carry	C = 1

Instruction Summary

Table 45 summarizes each Z8 instruction by its operation, addressing mode, operation code, and the flag(s) each instruction affects.

Table 45. Instruction Summary

Instruction and Operation	Address Mode dst	Address Mode src	Op Code Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst ← dst + src + C	See Note 1		1[]	*	*	*	*	0	*
ADD dst, src dst ← dst + src	See Note 1		0[]	*	*	*	*	0	*
AND dst, src dst ← dst AND src	See Note 1		5[]	–	*	*	0	–	–
CALL dst SP ← SP – 2 @ SP ← PC, PC ← dst	DA IRR		06 D4	–	–	–	–	–	–
CCF C ← NOT C			EF	*	–	–	–	–	–
CLR dst dst ← 0	R IR		B0 B11	–	–	–	–	–	–
COM dst dst ← NOT dst	R IR		60 61	–	*	*	0	–	–
CP dst, src dst – src	See Note 1		A[]	*	*	*	*	–	–
DA dst dst ← DA dst	R IR		40 41	*	*	*	X	–	–
DEC dst dst ← dst – 1	R IR		00 01	–	*	*	*	–	–
DECW dst dst ← dst – 1	R IR		80 81	–	*	*	*	–	–
DI IMR(7) ← 0			8F	–	–	–	–	–	–

Note: These instructions have an identical set of addressing modes, which are encoded for brevity. The first Op Code nibble is found in this instruction set table. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found on the left of the applicable addressing mode pair in the Op Code Map in Figure 48.

For example, the op code of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Packaging

Zilog's Z86E61 and Z86E63 MCUs are available in the following packages:

- 40-pin Plastic Dual Inline Package (PDIP)
- 44-pin Low-Profile Quad Flat Package (LQFP)
- 44-pin Plastic Chip Carrier (PLCC)

Current diagrams for each of these packages are published in Zilog's Packaging Product Specification (PS0072), which is available free for download from the Zilog website.

Ordering Information

Order your Z86E61/Z86E63 MCU products from Zilog using the part numbers shown in Table 46. For more information about ordering, please consult your local Zilog sales office. The Sales Location page on the Zilog website lists all regional offices.

Table 46. Z86E61/Z86E63 MCU Ordering Matrix

Part Number	Frequency	Package	Temperature Range
Z86E61 MCU			
Z86E6116PSG	16MHz	40-pin PDIP	0°C to +70°C
Z86E6116VSG	16MHz	44-pin PLCC	0°C to +70°C
Z86E6116ASG	16MHz	44-pin LQFP	0°C to +70°C
Z86E6120PSG	20MHz	40-pin PDIP	0°C to +70°C
Z86E6120VSG	20MHz	44-pin PLCC	0°C to +70°C
Z86E6120ASG	20MHz	44-pin LQFP	0°C to +70°C
Z86E63 MCU			
Z86E6316PSG	16MHz	40-pin PDIP	0°C to +70°C
Z86E6316VSG	16MHz	44-pin PLCC	0°C to +70°C
Z86E6316ASG	16MHz	44-pin LQFP	0°C to +70°C
Z86E6320PSG	20MHz	40-pin PDIP	0°C to +70°C
Z86E6320VSG	20MHz	44-pin PLCC	0°C to +70°C
Z86E6320ASG	20MHz	44-pin LQFP	0°C to +70°C