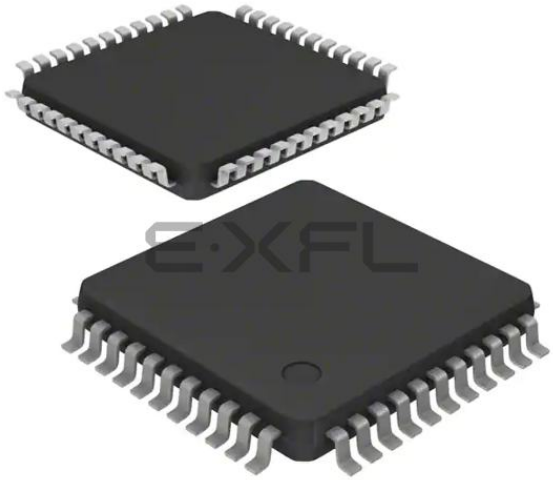

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e6316fsc

- Auto Latches
- High-voltage protection on high-voltage inputs
- RAM and EPROM Protect
- EPROM:
  - 16KB Z86E61
  - 32KB Z86E63

- 256-byte Register File:
  - 236 bytes of General-Purpose RAM
  - 16 bytes of Control and Status registers
  - 4 bytes for ports

- Two programmable 8-bit Counter/Timers, each with 6-bit programmable prescaler
- Six vectored priority interrupts from eight different sources
- On-chip oscillator that accepts a crystal ceramic resonator, LC or external clock drive

To unburden the system from coping with real-time tasks such as counting/timing and serial data communication, the Z86E61/Z86E63 MCU offers two on-chip counter/timers with a large number of user selectable modes. See the block diagram in Figure 1.

Figure 6 shows the pin-outs for the 44-pin PLCC Standard Mode package; Table 29 describes each pin.

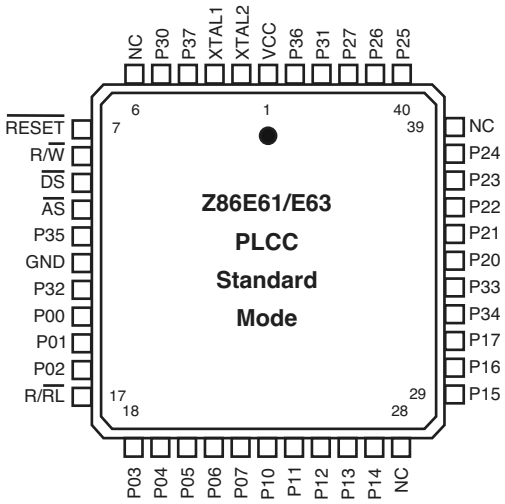

Figure 6. Z86E61/Z86E63 PLCC Pin Diagram, Standard Mode

Table 29. Z86E61/Z86E63 PLCC Pin Description, Standard Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{RESET}}$	Reset	Input
R/$\overline{\text{W}}$	Read/Write	Output
$\overline{\text{DS}}$	Data Strobe	Output
$\overline{\text{AS}}$	Address Strobe	Output
P00–P07 Port 0	8-bit General I/O	Input/Output
P10–P17 Port 1	8-bit General I/O	Input/Output
P20–P27 Port 2	8-bit General I/O	Input/Output
P30–P33 Port 3	4-bit Input	Input
P34–P37 Port 3	4-bit Output	Output
R/$\overline{\text{RL}}$	ROM/ROMless Control	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Figure 7 shows the pin-outs for the 44-pin PLCC EPROM Programming Mode package; Table 30 describes each pin.

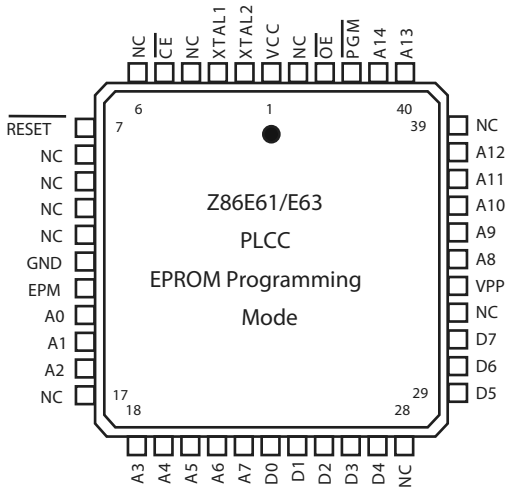

Figure 7. Z86E61/Z86E63 PLCC Pin Diagram, EPROM Programming Mode

Table 30. Z86E61/Z86E63 PLCC Pin Description, EPROM Programming Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{CE}$	Chip Enable	Input
$\overline{RESET}$	Reset	Input
EPM	EPROM Programming Mode	Input
A0–A14	15-bit Address Bus	Input
D7–D0	8-bit Data Bus	Input/Output
V_{PP}	Programming Voltage	Input
$\overline{PGM}$	Programming Mode	Input
$\overline{OE}$	Output Enable	Input
NC	Not Connected	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Port 0 (P07–P00)

Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07–P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 can provide address bits A11–A8 (lower nibble) or A15–A8 (lower and upper nibbles) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode Register.

In ROMless Mode, after a hardware reset, the Port 0 lines are defined as address lines A15–A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode; see Figure 8.

Port 3 (P37–P30)

Port 3 is an 8-bit, CMOS compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33–P30) input and four-fixed (P37–P34) output ports. Port 3, when used as serial I/O, is programmed as serial in and serial out, respectively; see Figure 11.

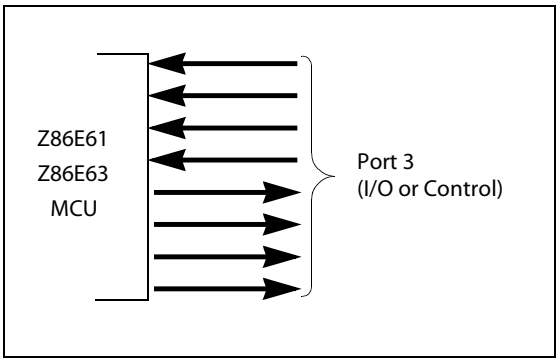

Figure 11. Port 3 Configuration

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (DAV and RDY); four external interrupt request signals (IRQ3–IRQ0); timer input and output signals (T_{IN} and T_{OUT}) Data Memory Select ($\overline{DM}$) and EPROM control signals (P30 = $\overline{CE}$, P31 = $\overline{OE}$, P32 = EPM and P33 = V_{PP}).

Table 31 lists the pin assignments for Port 3.

Table 31. Port 3 Pin Assignments*

Pin	I/O	CTCI	Interrupt	P0 HS	P1 HS	P2 HS	UART	Ext	EPROM
P30	In	T_{IN}	IRQ3				Serial In		$\overline{CE}$
P31	In	T_{IN}	IRQ2			D/R			$\overline{OE}$
P32	In	T_{IN}	IRQ0	D/R					EPM
P33	In	T_{IN}	IRQ1		D/R				V_{PP}
P34	Out	T_{OUT}			R/D			$\overline{DM}$	
P35	Out	T_{OUT}		R/D					
P36	Out	T_{OUT}				R/D			
P37	Out	T_{OUT}					Serial Out		
T0			IRQ4						
T1			IRQ5						

Note: *HS = Handshake Signals; D = Data Available; R = Ready.

Address Space

This section describes the memory and addressing functions of the Z86E61/Z86E63 MCU.

Program Memory

The Z86E61/Z86E63 MCU can address 48KB (Z86E61) or 32KB (Z86E63) of external program memory; see Figure 13. The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM Mode, byte 13 to byte 16383 (Z86E61) or 32767 (Z86E63) consists of on-chip EPROM. At addresses 16384 (Z86E61) or 32768 (Z86E63) and above, the Z86E61/Z86E63 MCU executes external program memory fetches. In ROMless Mode, the Z86E61/Z86E63 MCU can address up to 64KB of program memory. Program execution begins at external location 000C (HEX) after a reset.

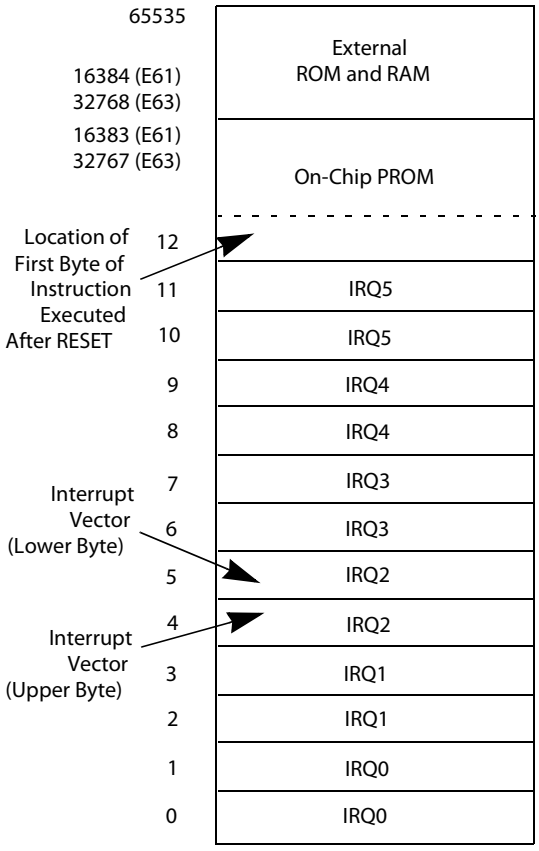

Figure 13. Program Memory Configuration

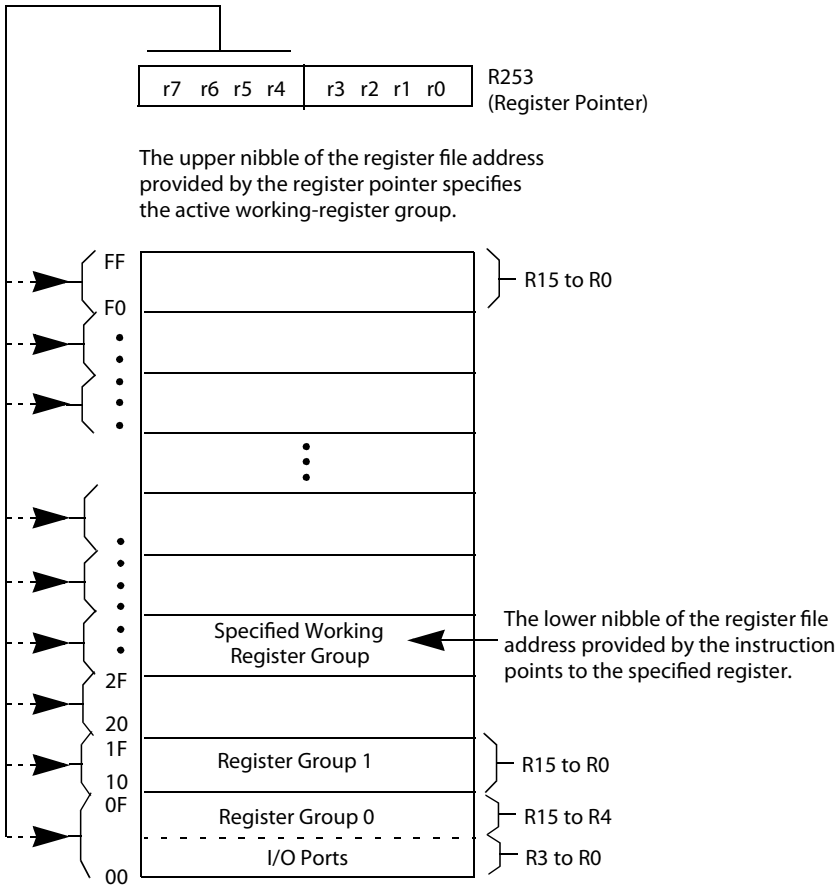

Figure 16. Register Pointer

Stack

The Z86E61/Z86E63 MCU has a 16-bit Stack Pointer (R255–R254) used for external stacks that reside anywhere in the data memory for the ROMless Mode, but only from 16384 (Z86E61) or 32768 (Z86E63) to 65535 in the EPROM Mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R239–R4). The high byte of the Stack Pointer (SPH Bits 15–8) can be use as a general-purpose register when using internal stack only.

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counters and prescalers reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter is programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (Single Pass Mode) or to automatically reload the initial value and continue counting (Modulo-n Continuous Mode).

The counter, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode Register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3 line P36 also serves as a timer output (T_{OUT}) through which T0, T1, or the internal clock can be output. The counter/timers are cascaded by connecting the T0 output to the input of T1.

Interrupts

The Z86E61/Z86E63 MCU has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follows: four sources are claimed by Port 3 lines P33–P30, one in Serial Out, one in Serial In, and two in the counter/timers; see Figure 18. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register; see Figure 40 on page 48.

All Z86E61/Z86E63 MCU interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request Register is polled to determine which of the interrupt requests need service. Software initialized interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

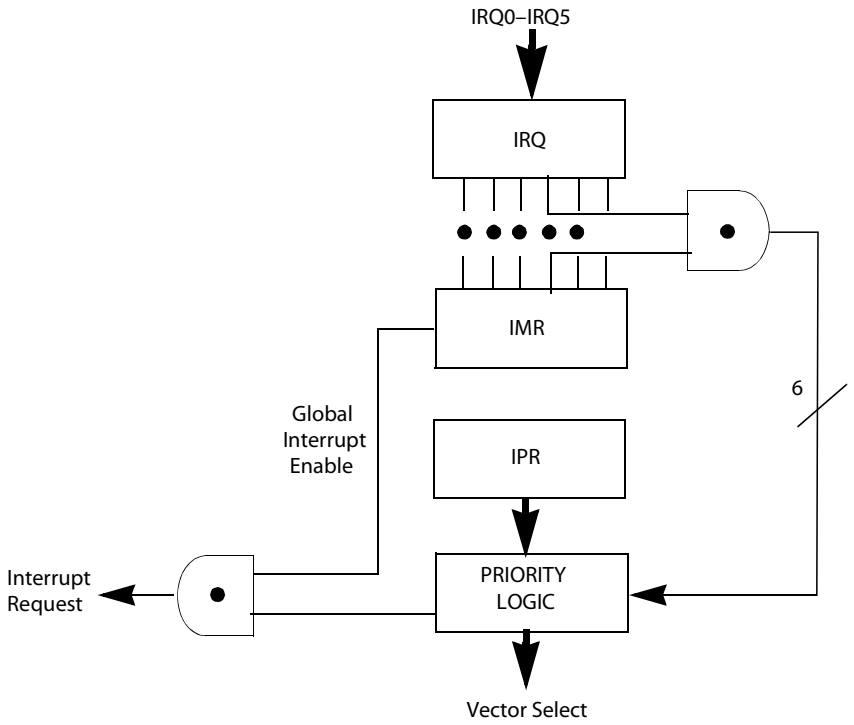

Figure 18. Interrupt Block Diagram

For the ROMless Mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the Flag Register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

Clock

The Z86E61/Z86E63 MCU's on-chip oscillator features a high gain, parallel resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 20 MHz max; series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF < CL < 100 pF) from each pin to ground; see Figure 19.

Absolute Maximum Ratings

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Table 34 lists the absolute maximum ratings of the Z86E61/Z86E63 MCU.

Table 34. Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
V_{CC}	Supply Voltage[1]	–0.3	+7.0	V
T_{STG}	Storage Temperature	–65	+150	°C
T_A	Operating Ambient Temperature		See Note 2	°C

Notes:
1. Voltages on all pins with respect to GND.
2. See Ordering Information on page 60.

Standard Test Conditions

The characteristics described in this document apply to standard test conditions, as noted. All voltages are referenced to GND, and positive current flows into the referenced pin; see Figure 24.

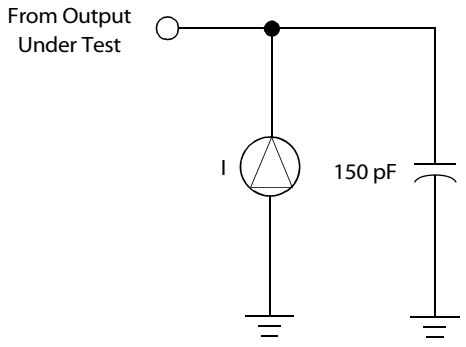

Figure 24. Test Load Diagram

AC Characteristics

Figure 27 displays the timing characteristics for the Z86E61/Z86E63 MCU. The circled numbers in this figure reference a description in Table 36 of each symbol, its parameter and its frequency range for these 16MHz and 20MHz parts.

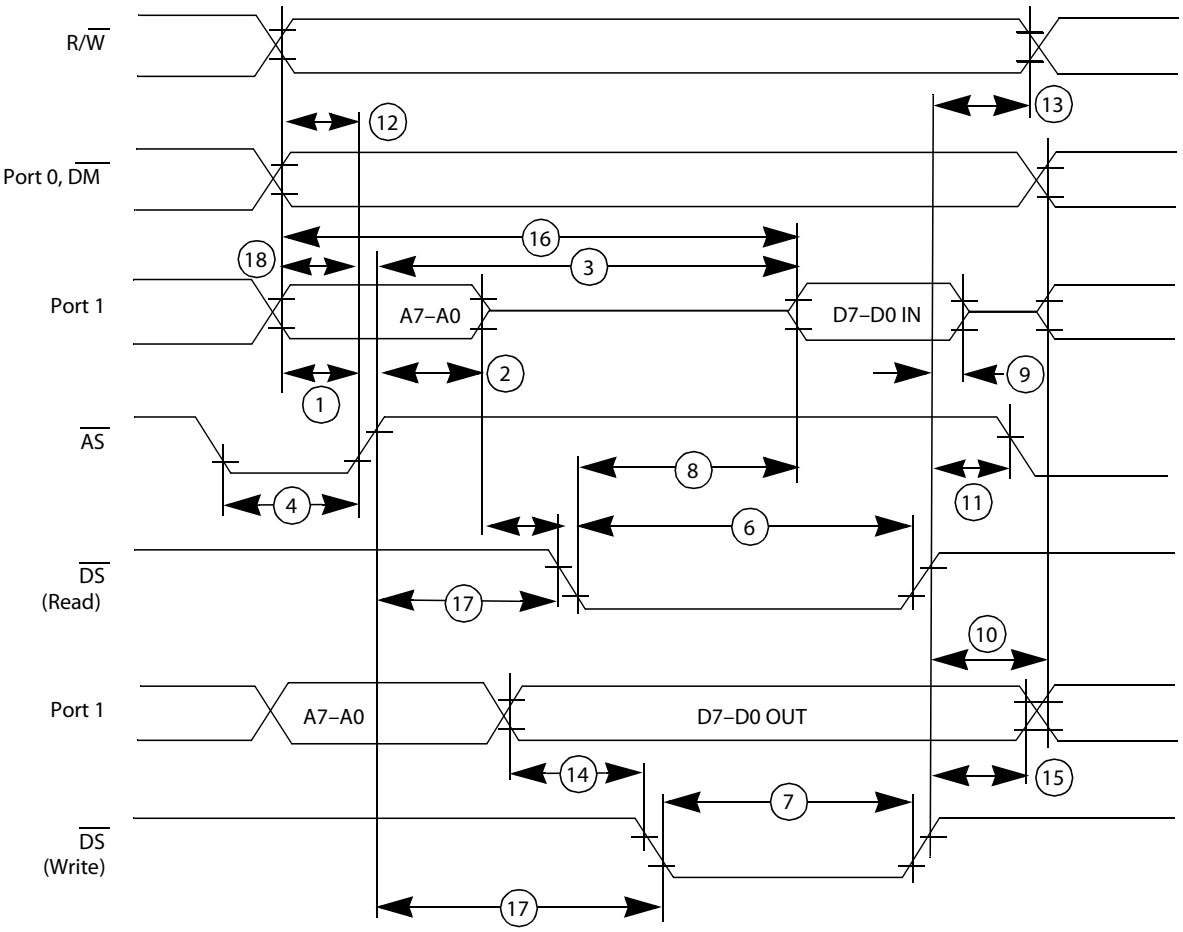

Figure 27. External I/O or Memory Read/Write Timing

Table 37. Clock-Dependent Formulas

Number	Symbol	Formula
1	TdA(AS)	0.40 TpC + 0.32
2	TdAS(A)	0.59 TpC – 3.25
3	TdAS(DR)	2.83 TpC + 6.14
4	TwAS	0.66 TpC – 1.65
6	TwDSR	2.33 TpC – 10.56
7	TwDSW	1.27 TpC + 1.67
8	TdDSR(DR)	1.97 TpC – 42.5
10	TdDS(A)	0.8 TpC
11	TdDS(AS)	0.59 TpC – 3.14
12	TdR/W(AS)	0.4 TpC
13	TdDS(R/$\overline{W}$)	0.8 TpC – 15
14	TdDW(DSW)	0.4 sTpC
15	TdDS(DW)	0.88 TpC – 19
16	TdA(DR)	4 TpC – 20
17	TdAS(DS)	0.91 TpC – 10.7
18	TdDM(AS)	0.9 TpC – 26.3

Input and output handshake timing characteristics are shown in Figures 28 and 29 and described in Table 38.

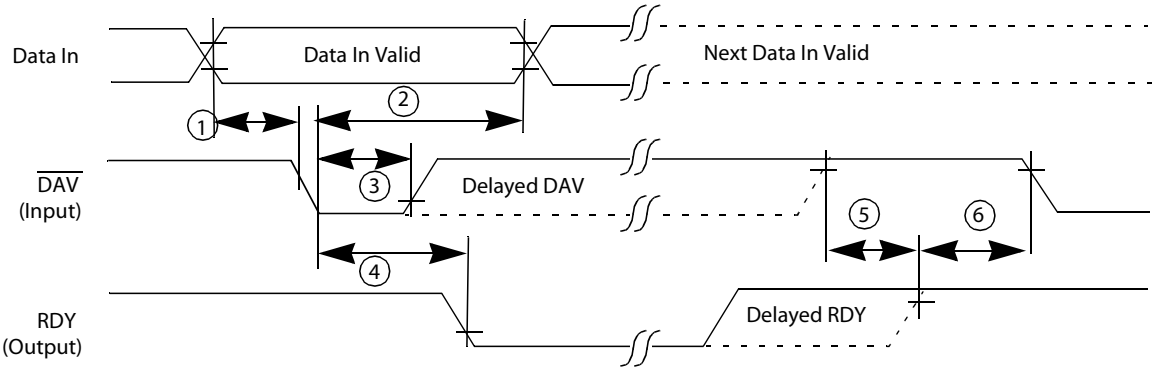

Figure 28. Input Handshake Timing

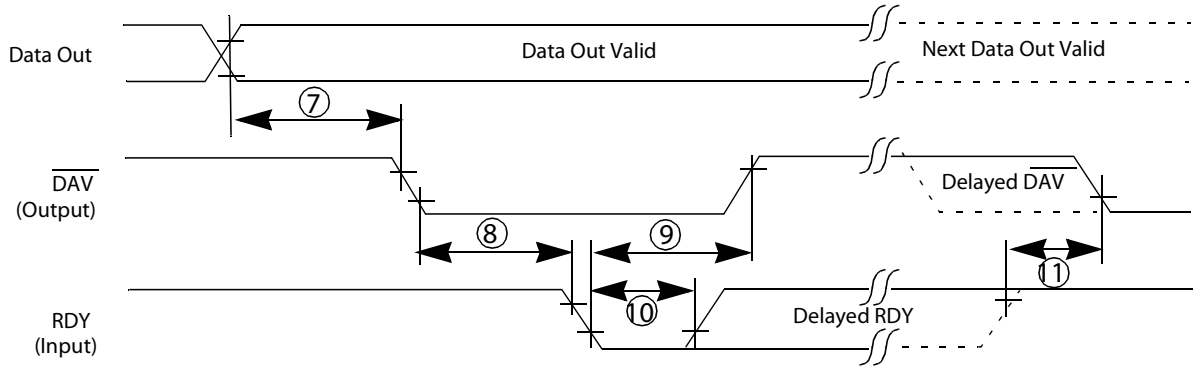

Figure 29. Output Handshake Timing

Table 38. Handshake Timing

			TA = 0°C to +70°				
			16MHz		20MHz		Data
No.	Symbol	Parameter	Min	Max	Min	Max	Direction
1	TsDI(DAV)	Data In Setup Time	0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		IN
3	TwDAV	Data Available Width	110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay		115		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay		115		115	IN
6	TdRDY0(DAV)	RDY Rise to DAV Fall Delay	0		0		IN
7	TdD0(DAV)	Data Out to DAV Fall Delay		TpC		TpC	OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay		115		115	OUT
10	TwRDY	RDY Width	110		110		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay		115		115	OUT

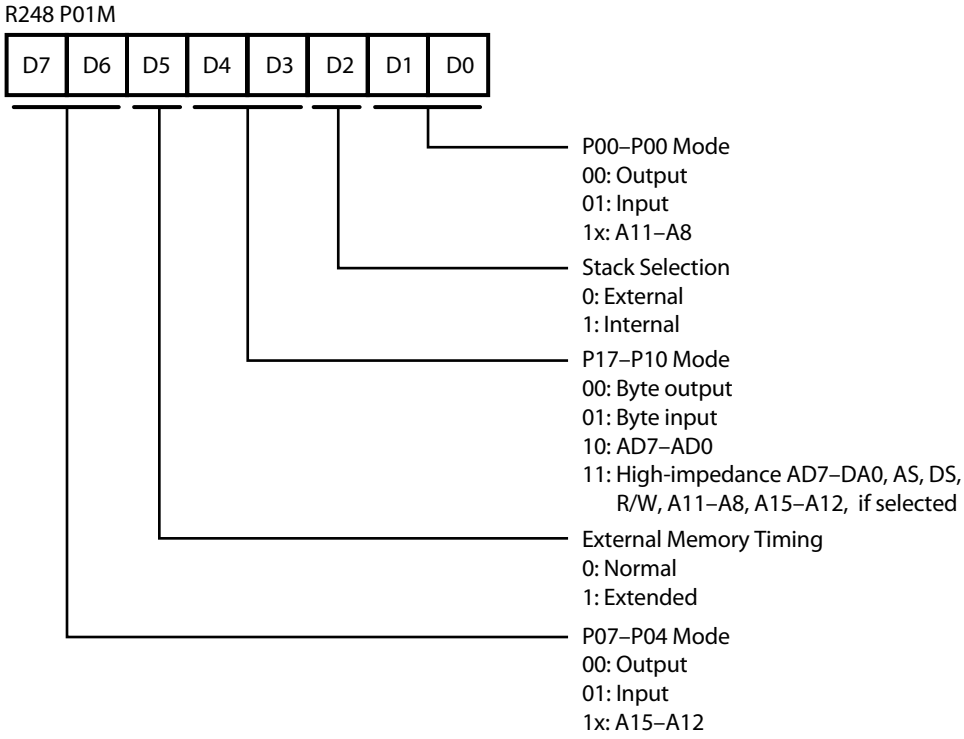

Figure 39. Port 0 and 1 Mode Register (F8H: Write Only)

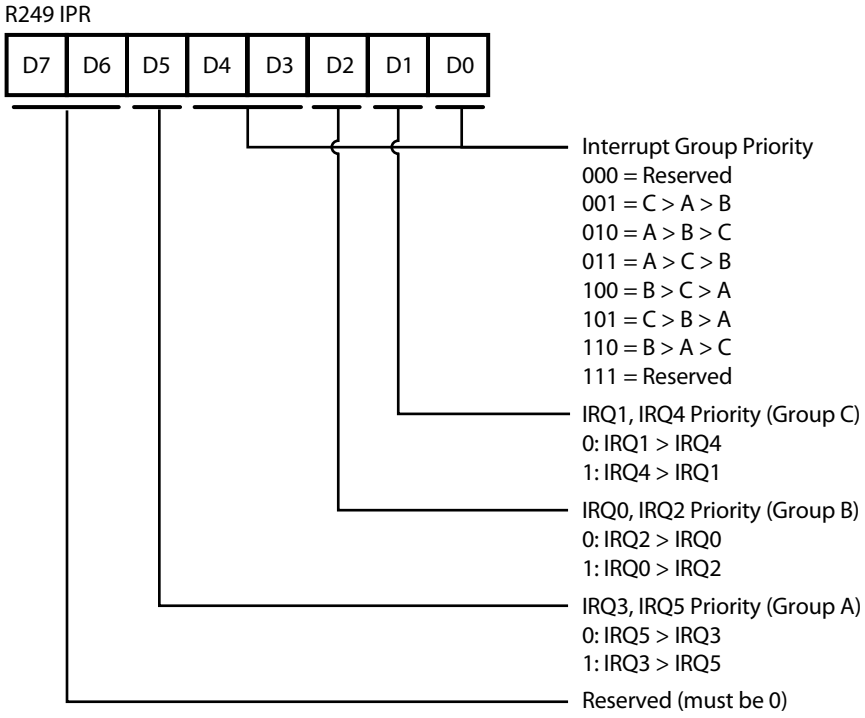

Figure 40. Interrupt Priority Register (F9H: Write Only)

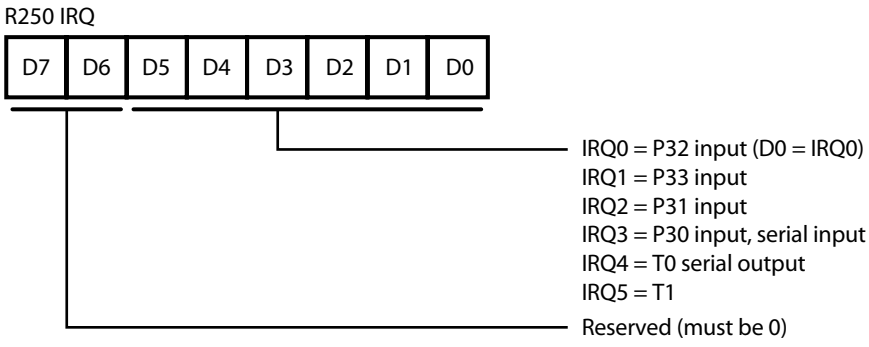

Figure 41. Interrupt Request Register (FAH: Read/Write)

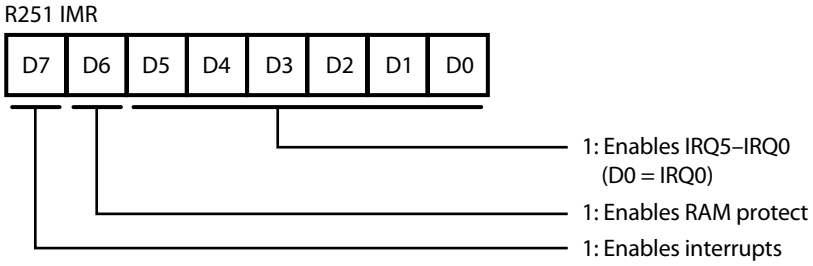

Figure 42. Interrupt Mask Register (FBH: Read/Write)

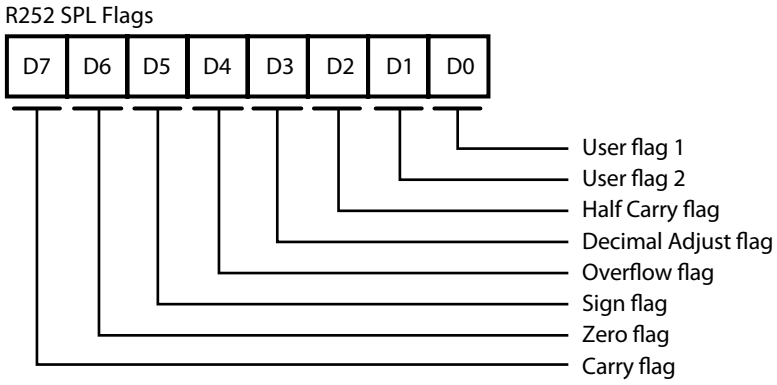

Figure 43. Flag Register (FCH: Read/Write)

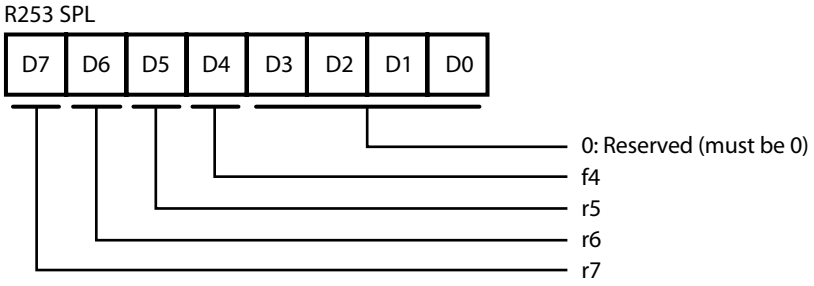

Figure 44. Register Pointer Register (FDH: Read/Write)

Table 44. Condition Codes (Continued)

Value	Mnemonic	Definition	Flags Set
0111	ULT	Unsigned Less Than	C = 1
1000		Always True	
1001	GE	Greater Than Or Equal To	(S XOR V) = 0
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
1100	NOV	No Overflow	V = 0
1101	PL	Plus	S = 0
1110	NE	Not Equal	Z = 0
1110	NZ	Not Zero	Z = 0
1111	NC	No Carry	C = 0
1111	UGE	Unsigned Greater Than Or Equal To	C = 0

Instruction Formats

Figure 47 shows the one-, two- and three-byte formats used in the Z8 instruction set.

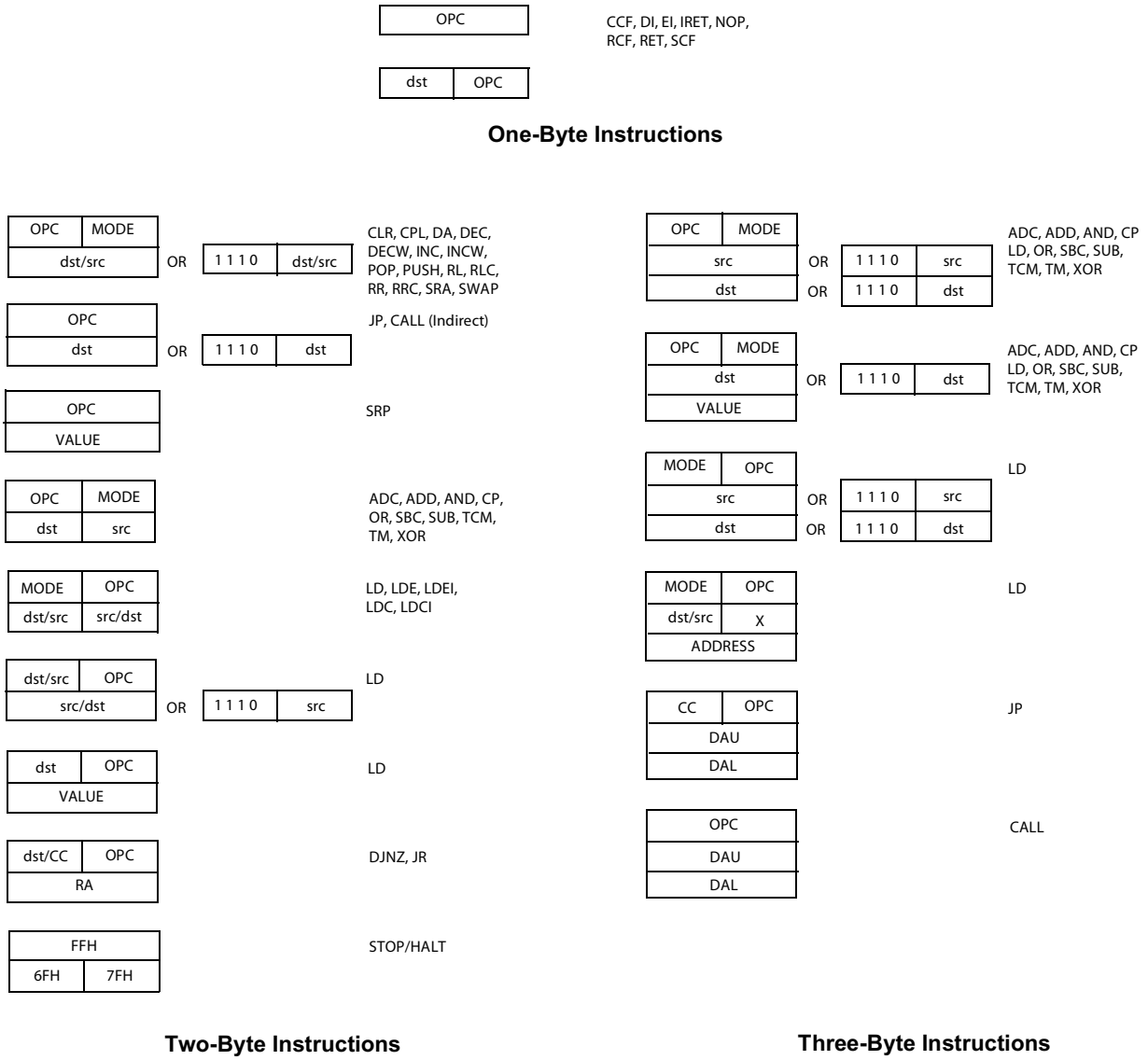

Figure 47. Instruction Formats

Instruction Summary

Table 45 summarizes each Z8 instruction by its operation, addressing mode, operation code, and the flag(s) each instruction affects.

Table 45. Instruction Summary

Instruction and Operation	Address Mode dst	Address Mode src	Op Code Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst ← dst + src + C	See Note 1		1[]	*	*	*	*	0	*
ADD dst, src dst ← dst + src	See Note 1		0[]	*	*	*	*	0	*
AND dst, src dst ← dst AND src	See Note 1		5[]	–	*	*	0	–	–
CALL dst SP ← SP – 2 @ SP ← PC, PC ← dst	DA IRR		06 D4	–	–	–	–	–	–
CCF C ← NOT C			EF	*	–	–	–	–	–
CLR dst dst ← 0	R IR		B0 B11	–	–	–	–	–	–
COM dst dst ← NOT dst	R IR		60 61	–	*	*	0	–	–
CP dst, src dst – src	See Note 1		A[]	*	*	*	*	–	–
DA dst dst ← DA dst	R IR		40 41	*	*	*	X	–	–
DEC dst dst ← dst – 1	R IR		00 01	–	*	*	*	–	–
DECW dst dst ← dst – 1	R IR		80 81	–	*	*	*	–	–
DI IMR(7) ← 0			8F	–	–	–	–	–	–

Note: These instructions have an identical set of addressing modes, which are encoded for brevity. The first Op Code nibble is found in this instruction set table. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found on the left of the applicable addressing mode pair in the Op Code Map in Figure 48.

For example, the op code of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Table 45. Instruction Summary (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Op Code Byte (Hex)	Flags Affected C	Z	S	V	D	H
RLC dst	R IR		10 11	*	*	*	*	–	–
RR dst	R IR		E0 E1	*	*	*	*	–	–
RRC dst	R IR		C0 C1	*	*	*	*	–	–
SBC dst, src dst ← dst ← src ← C	See Note 1		3[]	*	*	*	*	1	*
SCF C ← 1			DF	1	–	–	–	–	–
SRA dst	R IR		D0 D1	*	*	*	0	–	–
SRP dst RP ← src	Im		31	–	–	–	–	–	–
STOP			6F	1	–	–	–	–	–
SUB dst, src dst ← dst ← src	See Note 1		2[ ]	[	[	[	[	1	[
SWAP dst	R IR		F0 F1	X	*	*	X	–	–
TCM dst, src (NOT dst) AND src	See Note 1		6[ ]	–	*	*	0	–	–
TM dst, src dst AND src	See Note 1		7[ ]	–	*	*	0	–	–
XOR dst, src dst ← dst XOR src	See Note 1		B[ ]	–	*	*	0	–	–

Note: These instructions have an identical set of addressing modes, which are encoded for brevity. The first Op Code nibble is found in this instruction set table. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found on the left of the applicable addressing mode pair in the Op Code Map in Figure 48.

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