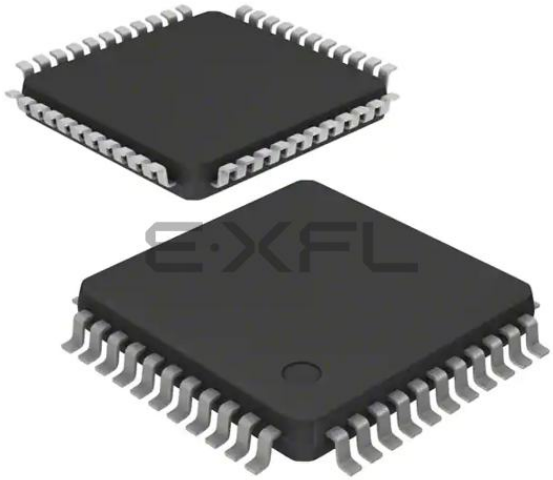

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e6316fsc00tr

Overview

The Z86E61/Z86E63 microcontrollers are members of the Z8® single-chip microcontroller family with 16K/32KB of EPROM and 236 bytes of general-purpose RAM. Offered in 40-pin DIP, 44-pin PLCC or 44-pin LQFP package styles, these devices are pin-compatible EPROM versions of the Z86C61/ 63. The ROMless pin option is available on the 44-pin versions only.

With 16KB/32KB of ROM and 236 bytes of general-purpose RAM, the Z86E61/Z86E63 MCU offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

For applications demanding powerful I/O capabilities, the Z86E61/Z86E63 MCU offers 32 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

The Z86E61/Z86E63 MCU can address both external memory and preprogrammed ROM, making it well suited for high-volume applications or where code flexibility is required. There are three basic address spaces available to support this configuration:

- Program memory
- Data memory
- 236 General-purpose registers

Features

The Z86E61 and Z86E63 MCUs offer the following features:

- 8-Bit CMOS microcontroller
- 40-pin DIP, 44-pin PLCC and 44-pin LQFP packages
- 4.5V to 5.5V operating range
- Clock speeds: 16MHz and 20MHz
- Low power consumption: 275 mW (max)
- Two Standby modes: STOP and HALT
- 32 Input/Output lines
- Full-duplex UART
- All digital inputs are TTL levels

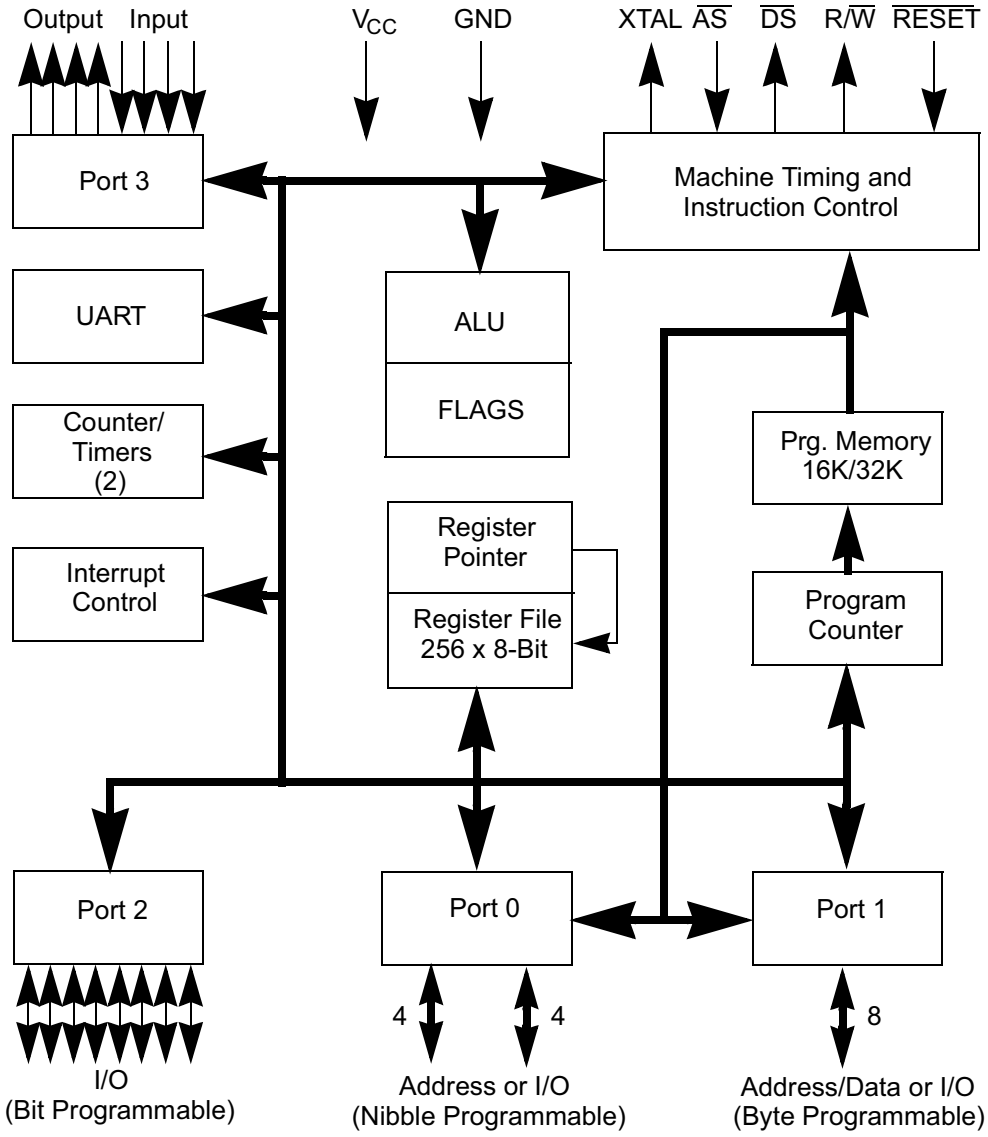

Figure 1. Z86E61/Z86E63 MCU Functional Block Diagram

Power connections follow the conventional descriptions listed in Table 24.

Table 24. Power Connection Conventions

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Pin Functions

The Z86E61/Z86E63 MCU is available in variety of package styles, programming modes and pin configurations. This section describes the pin signals and configurations for each of the 40-pin PDIP, 44-pin PLCC and 44-pin LQFP packages in both Standard and EPROM Programming modes.

Pin Signals

Figure 2 shows the pin-outs for the 40-pin PDIP Standard Mode package; Table 25 describes each pin.

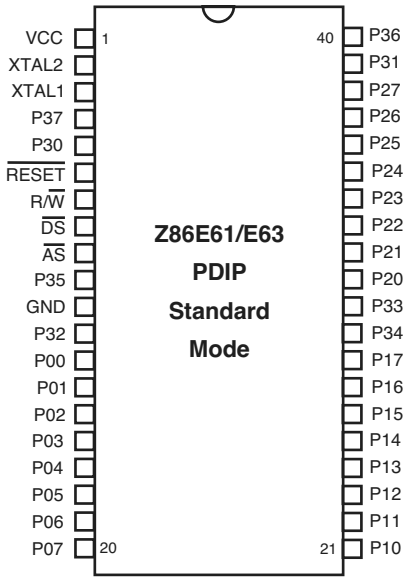

Figure 2. Z86E61/Z86E63 PDIP Pin Diagram, Standard Mode

Table 25. Z86E61/Z86E63 PDIP Pin Description, Standard Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{RESET}}$	Reset	Input
R/$\overline{\text{W}}$	Read/Write	Output

Figure 3 shows the pin-outs for the 40-pin PDIP EPROM Programming Mode package; Table 26 describes each pin.

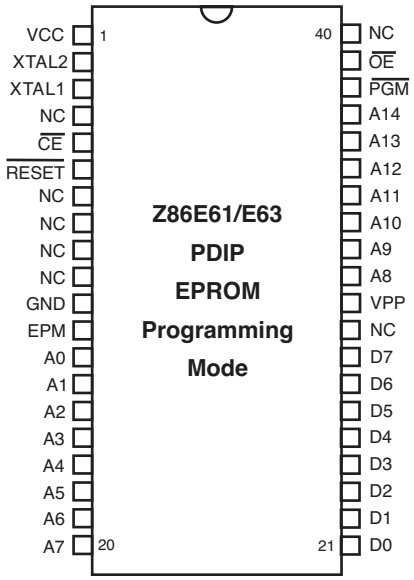

Figure 3. Z86E61/Z86E63 PDIP Pin Diagram, EPROM Programming Mode

Table 26. Z86E61/Z86E63 PDIP Pin Description, EPROM Programming Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{CE}$	Chip Enable	Input
$\overline{RESET}$	Reset	Input
EPM	EPROM Programming Mode	Input
A0–A14	15-bit Address Bus	Input
D7–D0	8-bit Data Bus	Input/Output
V_{PP}	Programming Voltage	Input
$\overline{PGM}$	Programming Mode	Input
$\overline{OE}$	Output Enable	Input
NC	Not Connected	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Figure 5 shows the pin-outs for the 44-pin LQFP EPROM Programming Mode package; Table 28 describes each pin.

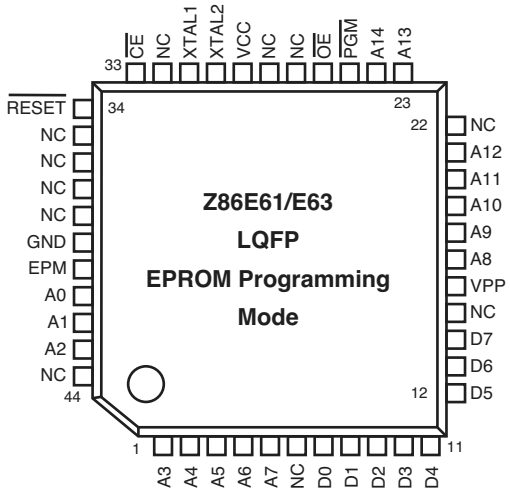

Figure 5. Z86E61/Z86E63 LQFP Pin Diagram, EPROM Programming Mode

Table 28. Z86E61/Z86E63 LQFP Pin Description, EPROM Programming Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{CE}$	Chip Enable	Input
$\overline{RESET}$	Reset	Input
EPM	EPROM Programming Mode	Input
A0–A14	15-bit Address Bus	Input
D7–D0	8-bit Data Bus	Input/Output
V_{PP}	Programming Voltage	Input
$\overline{PGM}$	Programming Mode	Input
$\overline{OE}$	Output Enable	Input
NC	Not Connected	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

Figure 6 shows the pin-outs for the 44-pin PLCC Standard Mode package; Table 29 describes each pin.

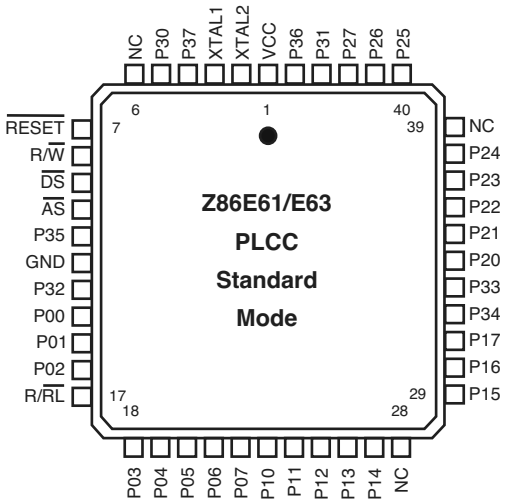

Figure 6. Z86E61/Z86E63 PLCC Pin Diagram, Standard Mode

Table 29. Z86E61/Z86E63 PLCC Pin Description, Standard Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{RESET}}$	Reset	Input
R/$\overline{\text{W}}$	Read/Write	Output
$\overline{\text{DS}}$	Data Strobe	Output
$\overline{\text{AS}}$	Address Strobe	Output
P00–P07 Port 0	8-bit General I/O	Input/Output
P10–P17 Port 1	8-bit General I/O	Input/Output
P20–P27 Port 2	8-bit General I/O	Input/Output
P30–P33 Port 3	4-bit Input	Input
P34–P37 Port 3	4-bit Output	Output
R/$\overline{\text{RL}}$	ROM/ROMless Control	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

open-drain output. Port 2 is always available for I/ 0 operation. When used as an I/0 port, Port 2 can be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines DAV2 and RDY2. The handshake signal assignment for Port 3 lines, P31 and P36, is dictated by the direction (input or output) assigned to P27; see Figure 10 and Table 31 on page 16).

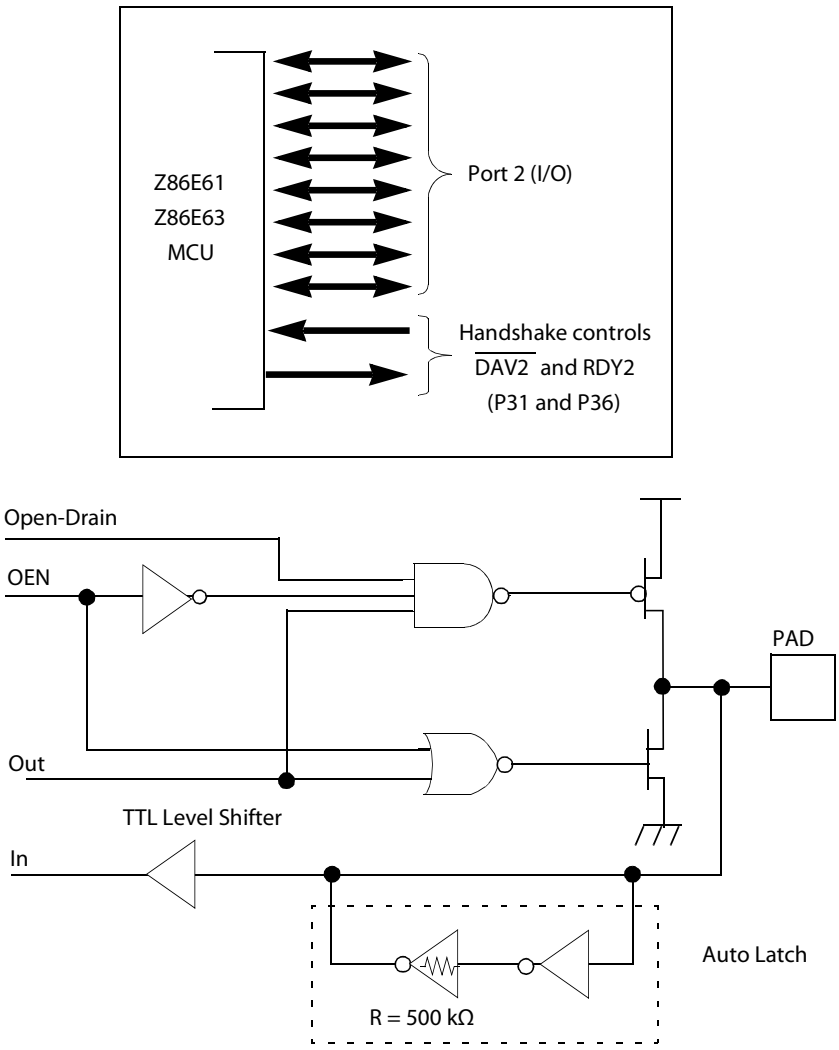

Figure 10. Port 2 Configuration

Port 3 (P37–P30)

Port 3 is an 8-bit, CMOS compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33–P30) input and four-fixed (P37–P34) output ports. Port 3, when used as serial I/O, is programmed as serial in and serial out, respectively; see Figure 11.

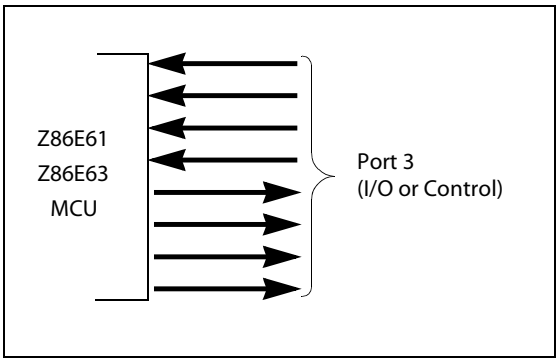

Figure 11. Port 3 Configuration

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (DAV and RDY); four external interrupt request signals (IRQ3–IRQ0); timer input and output signals (T_{IN} and T_{OUT}) Data Memory Select ($\overline{DM}$) and EPROM control signals (P30 = $\overline{CE}$, P31 = $\overline{OE}$, P32 = EPM and P33 = V_{PP}).

Table 31 lists the pin assignments for Port 3.

Table 31. Port 3 Pin Assignments*

Pin	I/O	CTCI	Interrupt	P0 HS	P1 HS	P2 HS	UART	Ext	EPROM
P30	In	T_{IN}	IRQ3				Serial In		$\overline{CE}$
P31	In	T_{IN}	IRQ2			D/R			$\overline{OE}$
P32	In	T_{IN}	IRQ0	D/R					EPM
P33	In	T_{IN}	IRQ1		D/R				V_{PP}
P34	Out	T_{OUT}			R/D			$\overline{DM}$	
P35	Out	T_{OUT}		R/D					
P36	Out	T_{OUT}				R/D			
P37	Out	T_{OUT}					Serial Out		
T0			IRQ4						
T1			IRQ5						

Note: *HS = Handshake Signals; D = Data Available; R = Ready.

Address Space

This section describes the memory and addressing functions of the Z86E61/Z86E63 MCU.

Program Memory

The Z86E61/Z86E63 MCU can address 48KB (Z86E61) or 32KB (Z86E63) of external program memory; see Figure 13. The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For EPROM Mode, byte 13 to byte 16383 (Z86E61) or 32767 (Z86E63) consists of on-chip EPROM. At addresses 16384 (Z86E61) or 32768 (Z86E63) and above, the Z86E61/Z86E63 MCU executes external program memory fetches. In ROMless Mode, the Z86E61/Z86E63 MCU can address up to 64KB of program memory. Program execution begins at external location 000C (HEX) after a reset.

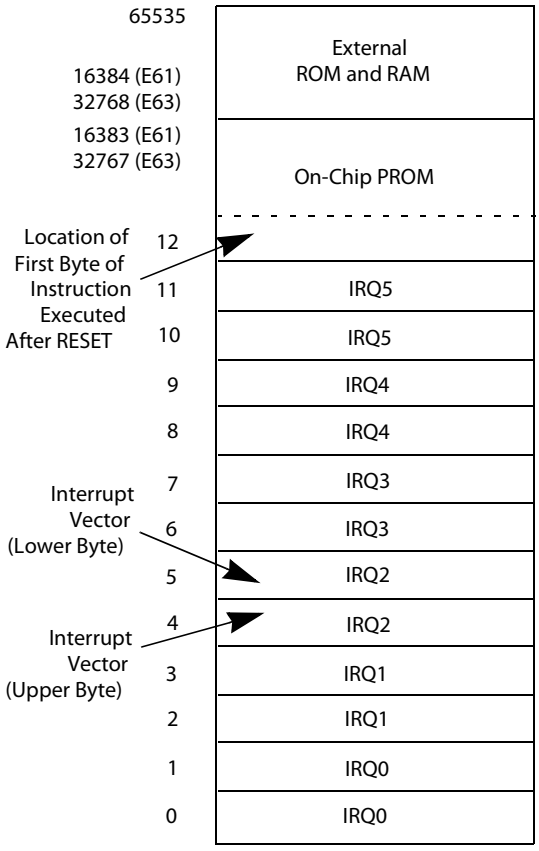

Figure 13. Program Memory Configuration

Functional Description

This section describes the counter/timer, interrupt, clock and timer mode functions of the Z86E61/Z86E63 MCU.

Counter/Timers

There are two 8-bit programmable counter/timers (T0–T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only, as shown in Figure 17.

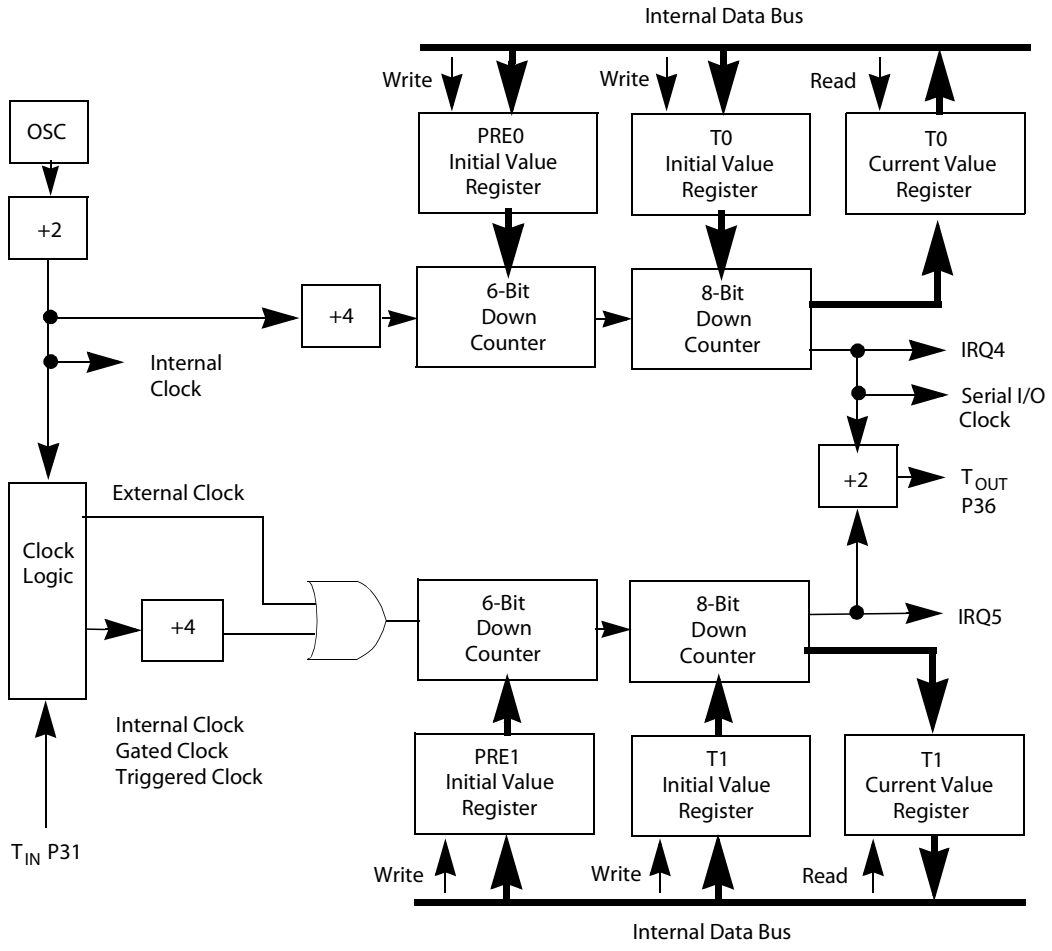

Figure 17. Counter/Timers Block Diagram

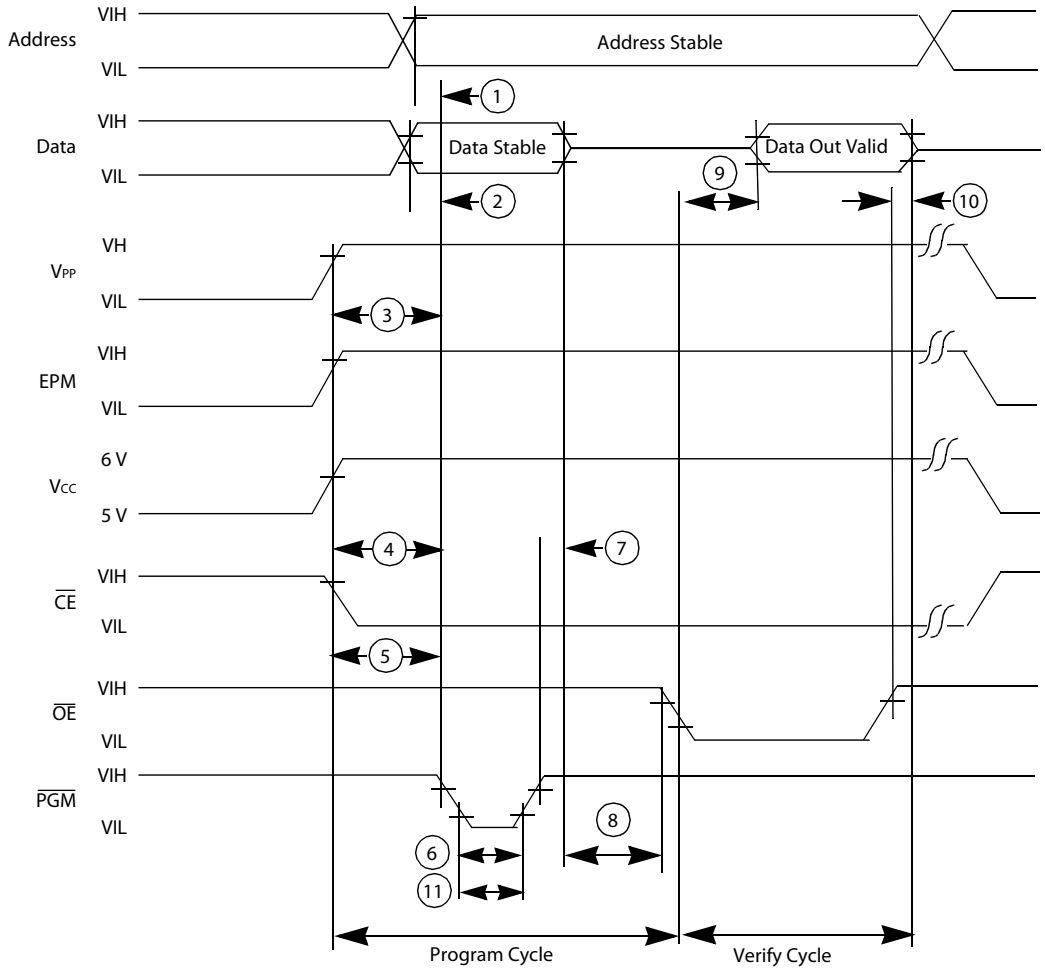

Figure 21. EPROM Program and Verify Timing

User Mode 3: PROM Verify

The Program Verify cycle is used as part of the intelligent programming algorithm to insure data integrity under worst-case conditions. It differs from the EPROM Read cycle in that V_{PP} is active and V_{CC} must be driven to 6.0V. Timing is shown in Figure 21.

User Modes 4 and 5: EPROM and RAM Protect

To extend program security, EPROM and RAM protect cycles are provided for the Z86E61/Z86E63 MCU. Execution of the EPROM protect cycle prohibits proper execution of the EPROM Read, EPROM Verify, and EPROM programming cycles. Execution of the RAM protect cycle disables accesses to the upper 128 bytes of register memory (excluding

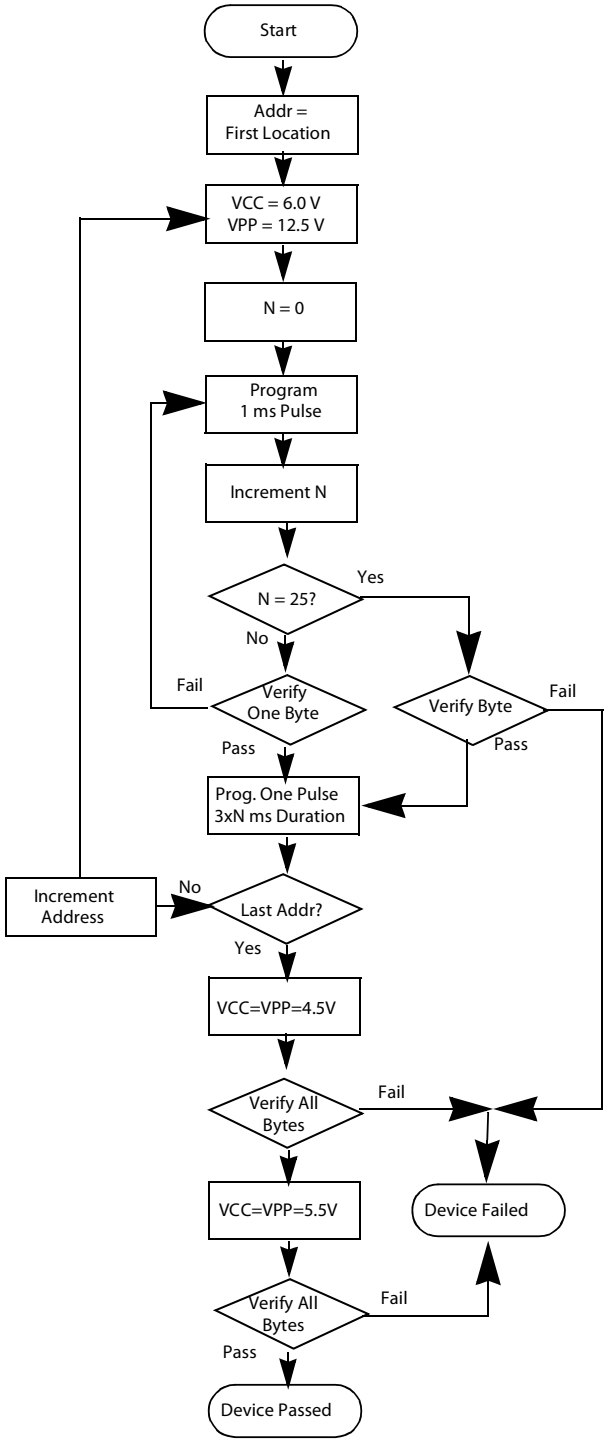

Figure 23. Intelligent Programming Flowchart

Absolute Maximum Ratings

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Table 34 lists the absolute maximum ratings of the Z86E61/Z86E63 MCU.

Table 34. Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
V_{CC}	Supply Voltage[1]	–0.3	+7.0	V
T_{STG}	Storage Temperature	–65	+150	°C
T_A	Operating Ambient Temperature		See Note 2	°C

Notes:
1. Voltages on all pins with respect to GND.
2. See Ordering Information on page 60.

Standard Test Conditions

The characteristics described in this document apply to standard test conditions, as noted. All voltages are referenced to GND, and positive current flows into the referenced pin; see Figure 24.

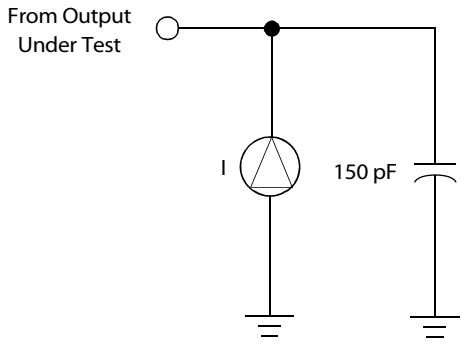

Figure 24. Test Load Diagram

DC Characteristics

Table 35 lists voltage and direct current characteristics for the Z86E61/Z86E63 MCU under differing conditions. Be advised that I_{CC2} requires loading TMR (F1Hh) with any value prior to STOP execution. Use the following sequence:

```
LD TMR,#00
NOP
STOP
```

Table 35. Direct Current Characteristics

Symbol	Parameter	Min	Max	Typical @ 25°C	Units	Conditions
	Max Input Voltage		7		V	I_{IN} < 250µA.
	Max Input Voltage	13			V	P33–P30 Only.
V_{CH}	Clock Input High Voltage	3.8	V_{CC}+0.3		V	Driven by External Clock Generator.
V_{CL}	Clock Input Low Voltage	–0.3	0.8		V	Driven by External Clock Generator.
V_{IH}	Input High Voltage	2.0	V_{CC}+0.3		V	
V_{IL}	Input Low Voltage	–0.3	0.8		V	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –2.0mA.
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = +2.0mA.
V_{RH}	Reset Input High Voltage	3.8	V_{CC}+0.3		V	
V_{RL}	Reset Input Low Voltage	–0.3	0.8		V	
I_{IL}	Input Leakage	–10	10		µA	V_{IN} = 0V, 5.25V.
I_{OL}	Output Leakage	–10	10		µA	V_{IN} = 0V, 5.25V.
I_{IR}	Reset Input Current		–50		µA	V_{CC}=+5.25V; V_{RL}=0V.
I_{CC}	Supply Current		50	25	mA	@ 16MHz.
			60	35	mA	@ 20MHz.
I_{CC1}	Standby Current		15	5	mA	HALT Mode @ 16MHz; V_{IN}=0V, V_{CC}
			20	10	mA	HALT Mode @ 20MHz; V_{IN}=0V, V_{CC}
I_{CC2}	Standby Current		20	5	µA	STOP Mode V_{IN}=0V, V_{CC}

Supply Current

Figure 25 shows the typical supply current values (in milliamps), for the Z86E61/Z86E63 MCU as a function of frequency (in megahertz).

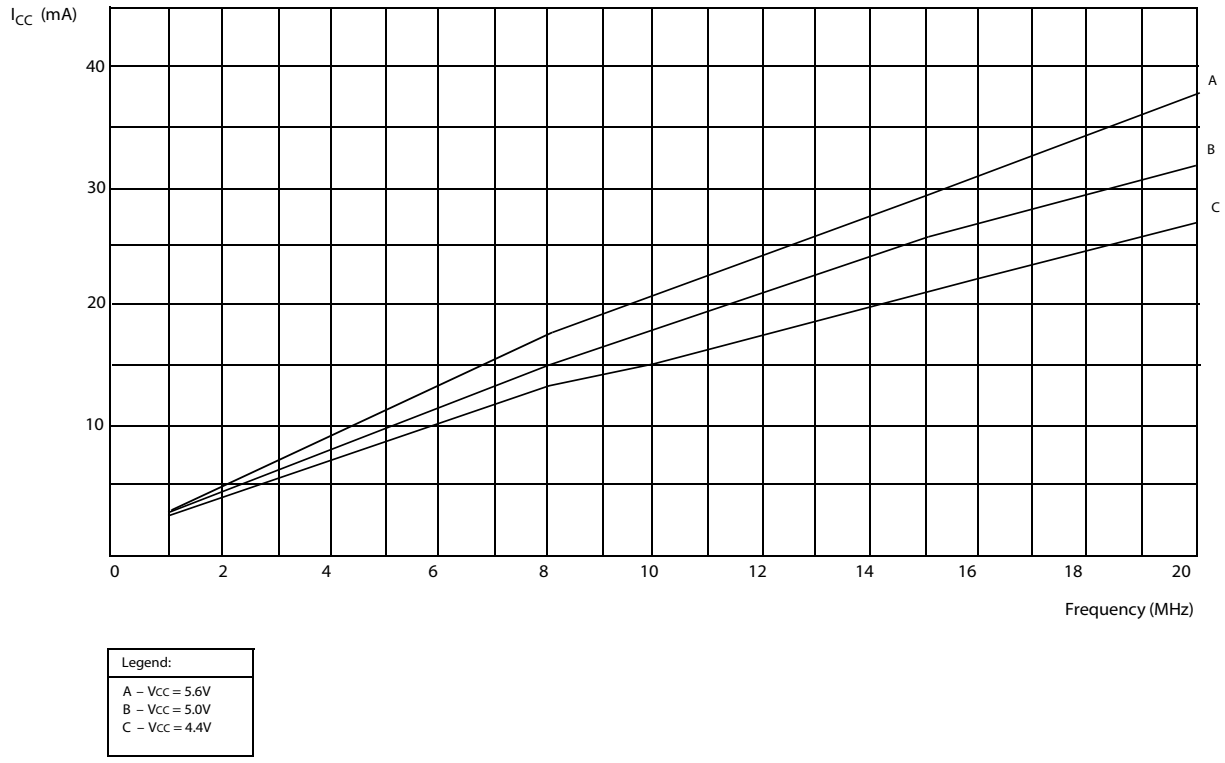

Figure 25. Typical I_{CC} vs. Frequency

Table 36 lists the alternating current characteristics for the Z86E61/Z86E63 MCU as they relate to Figure 27. Formulas for each parameter are listed in Table 37.

Table 36. External I/O or Memory Read and Write Timing

			T_A = 0°C to +70°C					
			16MHz[1]		20MHz			
No.	Symbol	Parameter	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to $\overline{AS}$ Rise Delay	20		26		ns	2,3
2	TdAS(A)	$\overline{AS}$ Rise to Address Float Delay	30		28		ns	2,3
3	TdAS(DR)	$\overline{AS}$ Rise to Read Data Req'd Valid		180		160	ns	2,3,4
4	TwAS	$\overline{AS}$ Low Width	35		36		ns	2,3
5	TdAZ(DS)	Address Float to DS Fall	0		0		ns	
6	TwDSR	$\overline{DS}$ (Read) Low Width	135		130		ns	2,3,4
7	TwDSW	$\overline{DS}$ (Write) Low Width	80		75		ns	2,3,4
8	TdDSR(DR)	$\overline{DS}$ Fall to Read Data Req'd Valid		75		100	ns	2,3,4
9	ThDR(DS)	Read Data to DS Rise Hold Time	0		0		ns	2,3
10	TdDS(A)	$\overline{DS}$ Rise to Address Active Delay	35		48		ns	2,3
11	TdDS(AS)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay	30		36		ns	2,3
12	TdR/W(AS)	R/W Valid to $\overline{AS}$ Rise Delay	20		32		ns	2,3
13	TdDS(R/W)	$\overline{DS}$ Rise to R//W Not Valid	30		36		ns	2,3
14	TdDW(DSW)	Write Data Valid to $\overline{DS}$ Fall (Write) Delay	25		40		ns	2,3
15	TdDS(DW)	$\overline{DS}$ Rise to Write Data Not Valid Delay	30		40		ns	2,3
16	TdA(DR)	Address Valid to Read Data Req'd Valid		200		200	ns	2,3,4
17	TdAS(DS)	AS Rise to $\overline{DS}$ Fall Delay	40		48		ns	2,3
18	TdDM(AS)	$\overline{DM}$ Valid to $\overline{AS}$ Fall Delay	30		36		ns	2,3

Notes:
1. All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
2. Timing numbers given are for minimum TpC.
3. See Table 37.
4. When using extended memory timing, add 2 TpC.

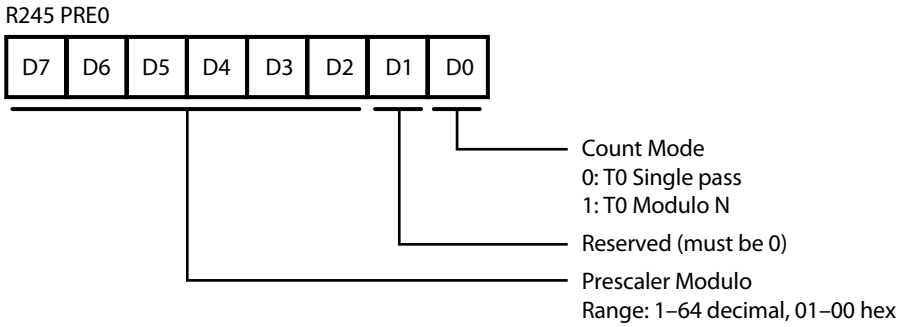

Figure 36. Prescaler 0 Register (F5H: Write Only)

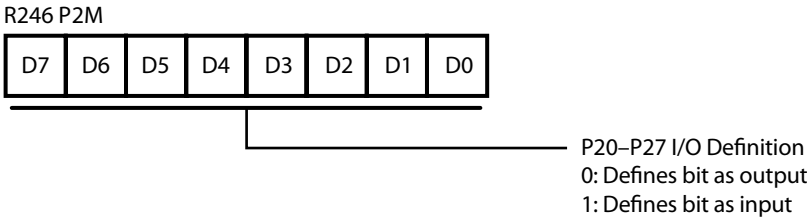

Figure 37. Port 2 Mode Register (F6H: Write Only)

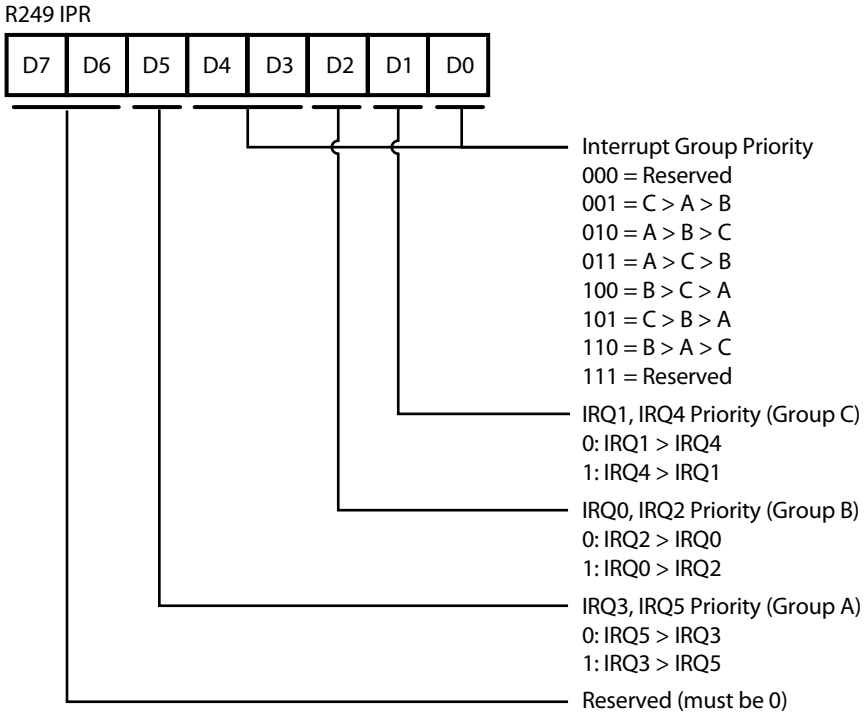

Figure 40. Interrupt Priority Register (F9H: Write Only)

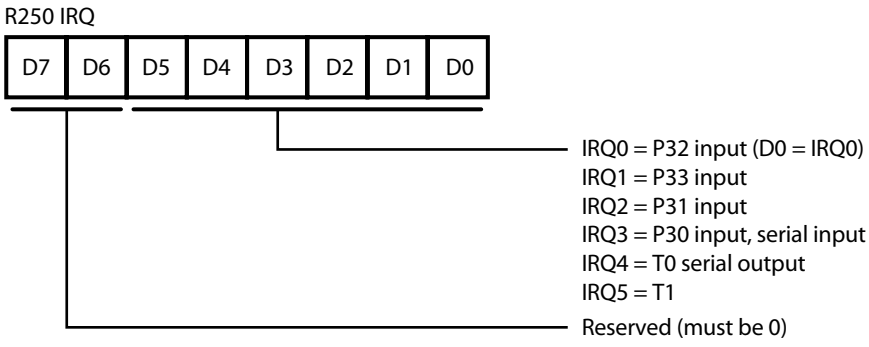

Figure 41. Interrupt Request Register (FAH: Read/Write)

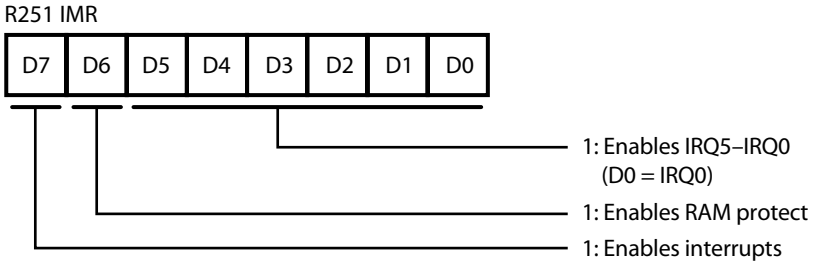

Figure 42. Interrupt Mask Register (FBH: Read/Write)

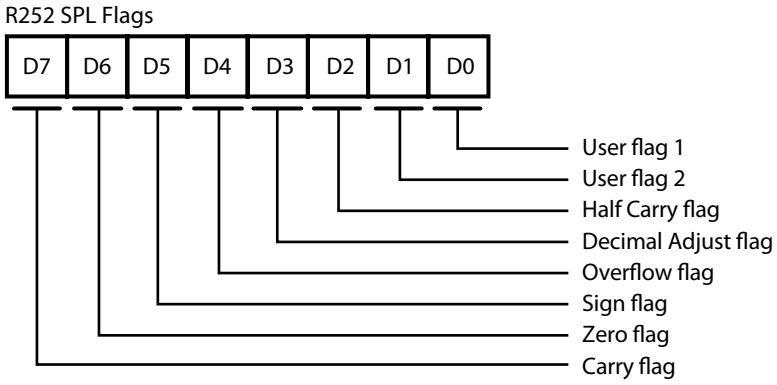

Figure 43. Flag Register (FCH: Read/Write)

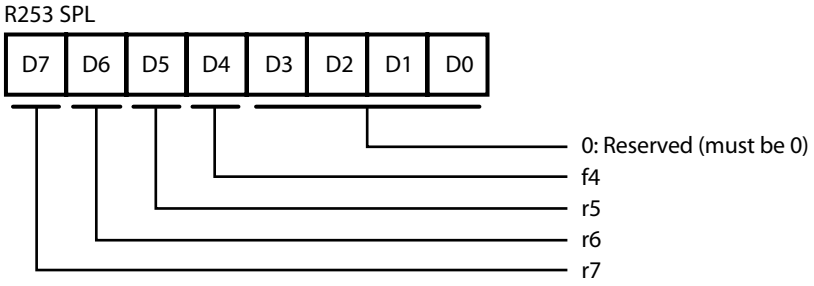

Figure 44. Register Pointer Register (FDH: Read/Write)

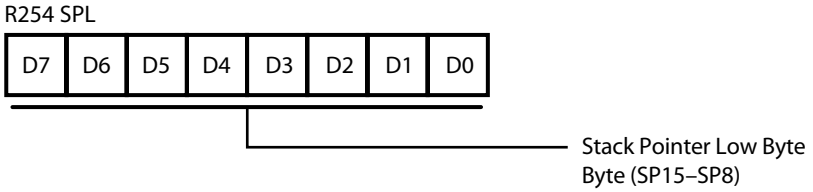

Figure 45. Stack Pointer Register (FEH: Read/Write)

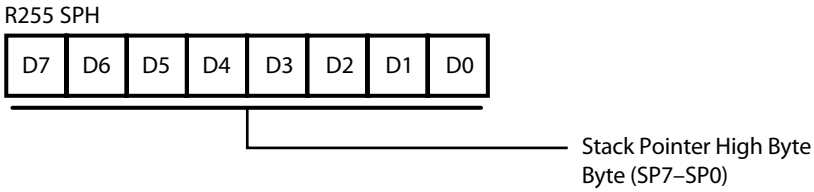

Figure 46. Stack Pointer Register (FFH: Read/Write)