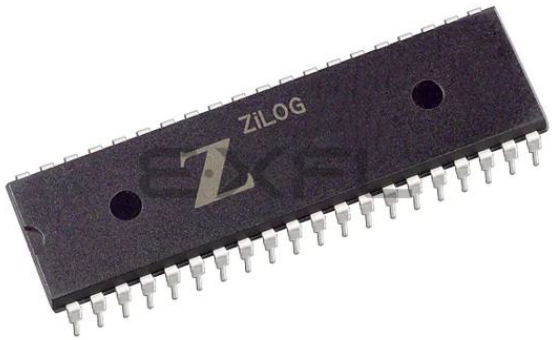

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e6316psg

Revision History

Each instance in the following revision history table reflects a change to this document from its previous version. For more details, refer to the corresponding pages or appropriate links provided in the table.

Date	Revision Level	Description	Page
Feb 2012	04	Globally updated for style and content.	All
Oct 2008	03	Updated pin descriptions.	11
May 2008	02	Added LQFP pin diagram (Standard and Programming modes); replaced 44-pin QFP with 44-pin LQFP for CR #10886.	7, 8
Nov 2001	01	Original issue.	All

Pin Functions

The Z86E61/Z86E63 MCU is available in variety of package styles, programming modes and pin configurations. This section describes the pin signals and configurations for each of the 40-pin PDIP, 44-pin PLCC and 44-pin LQFP packages in both Standard and EPROM Programming modes.

Pin Signals

Figure 2 shows the pin-outs for the 40-pin PDIP Standard Mode package; Table 25 describes each pin.

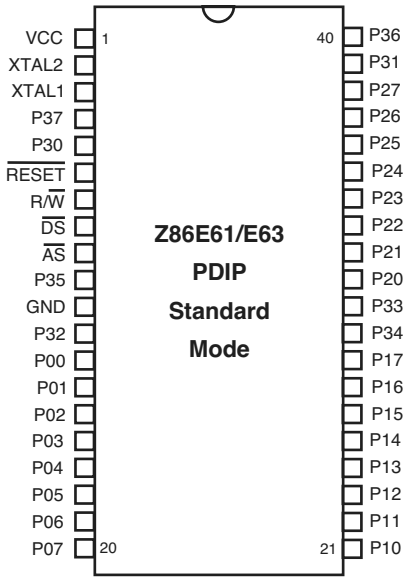

Figure 2. Z86E61/Z86E63 PDIP Pin Diagram, Standard Mode

Table 25. Z86E61/Z86E63 PDIP Pin Description, Standard Mode

Pin Signal	Description	I/O
XTAL2	Crystal Oscillator Clock	Output
XTAL1	Crystal Oscillator Clock	Input
$\overline{\text{RESET}}$	Reset	Input
R/$\overline{\text{W}}$	Read/Write	Output

Table 25. Z86E61/Z86E63 PDIP Pin Description, Standard Mode (Continued)

Pin Signal	Description	I/O
$\overline{DS}$	Data Strobe	Output
$\overline{AS}$	Address Strobe	Output
P00–P07 Port 0	8-bit General I/O	Input/Output
P10–P17 Port 1	8-bit General I/O	Input/Output
P20–P27 Port 2	8-bit General I/O	Input/Output
P30–P33 Port 3	4-bit Input	Input
P34–P37 Port 3	4-bit Output	Output
R/$\overline{RL}$	ROM/ROMless Control	Input
GND	Ground	Input
V_{CC}	Power Supply	Input

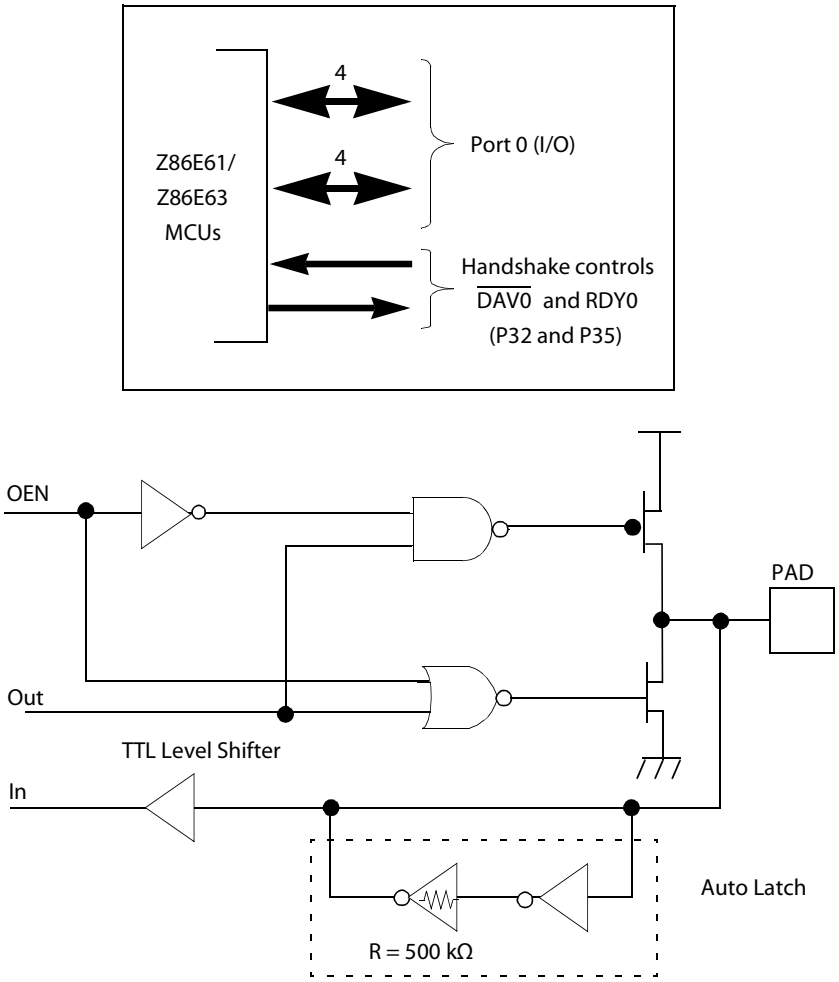

Figure 8. Port 0 Configuration

Port 1 (P17–P10)

Port 1 is an 8-bit, byte programmable, bidirectional, TTL compatible port. It has multiplexed Address (A7–A0) and Data (D7–D0) ports. For the Z86E61/Z86E63 MCU, these eight I/O lines can be programmed as input or output lines or are configured under software control as an address/data port for interfacing external memory. When used as an I/O port, Port 1 can be placed under handshake control. In this configuration, Port 3 lines, P33 and P34, are used as the handshake controls RDY1 and DAV1.

Memory locations greater than 16384 (Z86E61) or 32768 (Z86E63) are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multi-

Port 3 (P37–P30)

Port 3 is an 8-bit, CMOS compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33–P30) input and four-fixed (P37–P34) output ports. Port 3, when used as serial I/O, is programmed as serial in and serial out, respectively; see Figure 11.

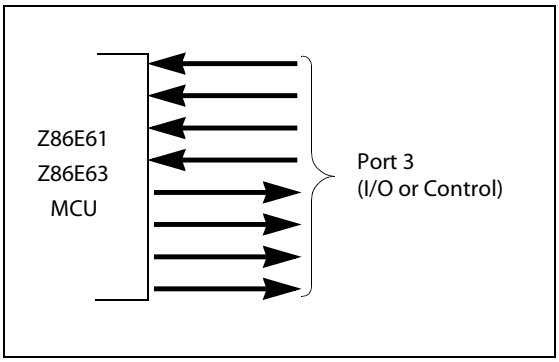

Figure 11. Port 3 Configuration

Port 3 is configured under software control to provide the following control functions: handshake for Ports 0 and 2 (DAV and RDY); four external interrupt request signals (IRQ3–IRQ0); timer input and output signals (T_{IN} and T_{OUT}) Data Memory Select ($\overline{DM}$) and EPROM control signals (P30 = $\overline{CE}$, P31 = $\overline{OE}$, P32 = EPM and P33 = V_{PP}).

Table 31 lists the pin assignments for Port 3.

Table 31. Port 3 Pin Assignments*

Pin	I/O	CTCI	Interrupt	P0 HS	P1 HS	P2 HS	UART	Ext	EPROM
P30	In	T_{IN}	IRQ3				Serial In		$\overline{CE}$
P31	In	T_{IN}	IRQ2			D/R			$\overline{OE}$
P32	In	T_{IN}	IRQ0	D/R					EPM
P33	In	T_{IN}	IRQ1		D/R				V_{PP}
P34	Out	T_{OUT}			R/D			$\overline{DM}$	
P35	Out	T_{OUT}		R/D					
P36	Out	T_{OUT}				R/D			
P37	Out	T_{OUT}					Serial Out		
T0			IRQ4						
T1			IRQ5						

Note: *HS = Handshake Signals; D = Data Available; R = Ready.

UART Operation. Port 3 lines, P37 and P30, are programmed as serial I/0 lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/ Timer0.

The Z86E61/Z86E63 MCU automatically adds a start bit and two stop bits to transmitted data; see Figure 12. Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits, and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

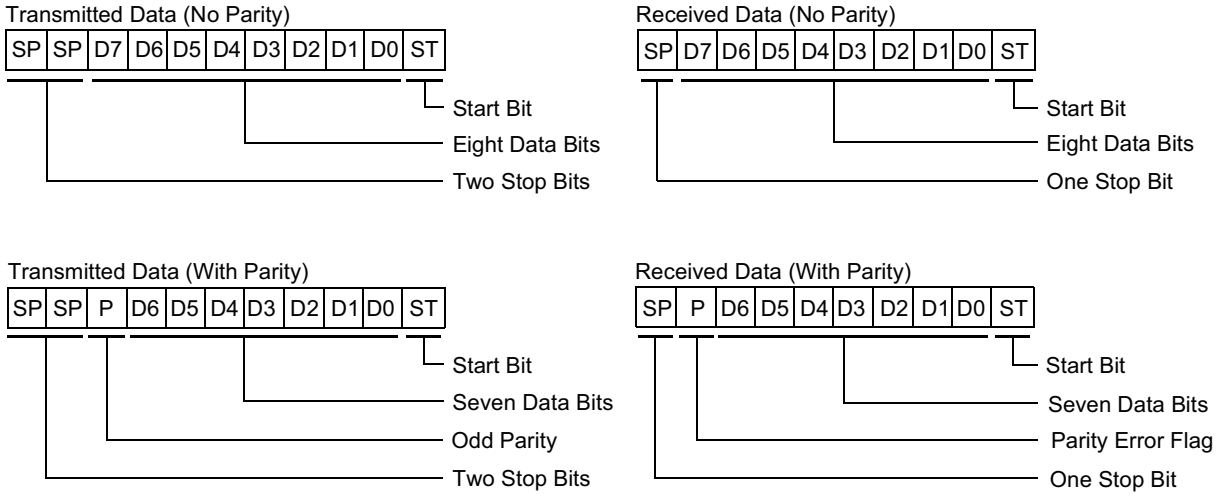

Figure 12. Serial Data Formats

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not driven by any source.

Note: P33–P30 inputs differ from the Z86C61/C63 in that there is no clamping diode to V_{CC} because of the EPROM high voltage detection circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM Mode.

Data Memory

The EPROM version can address up to 48KB (Z86E61) or 32KB (Z86E63) of external data memory (DM) space beginning at location 16384 (Z86E61) or 32768 (Z86E63). The ROMless version can address up to 64KB of external data memory. External data memory may be included with, or separated from, the external program memory space. DM, an optional I/0 function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space; see Figure 14. The state of the DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (DM inactive) memory, and an LDE instruction references DATA (DM active Low) memory.

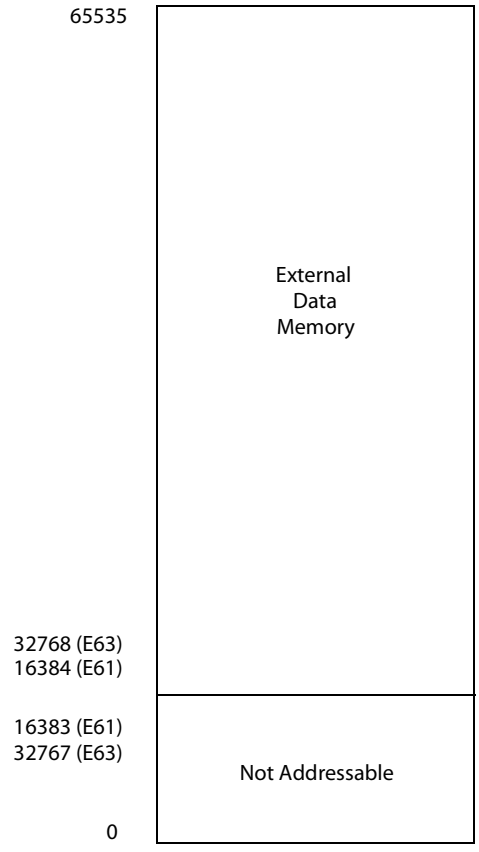

Figure 14. Data Memory Configuration

Register File

The register file consists of four I/0 port registers, 236 general-purpose registers, and 16 control and status registers, as shown in Figure 15. The instructions can access registers directly or indirectly through an 8-bit address field. The Z86E61/Z86E63 MCU also allows short 4-bit register addressing using the Register Pointer, which is shown in Figure 16. In 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

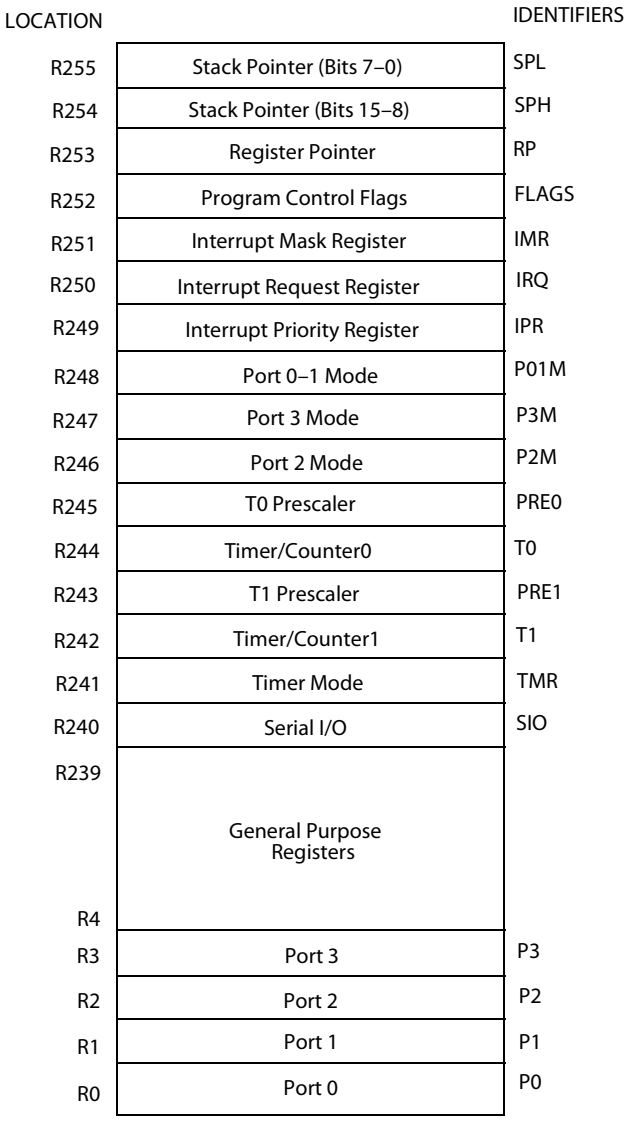

Figure 15. Register File

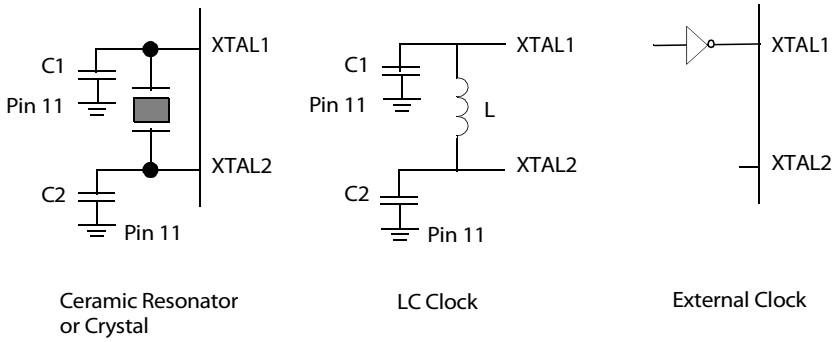

Figure 19. Oscillator Configuration

Note: The actual capacitor value is specified by the crystal manufacturer.

HALT

Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP

This instruction turns off the internal clock and external crystal oscillation, and reduces the standby current to 5µA (typical) or less. The STOP Mode is terminated by a reset, which causes the processor to restart the application program at address 000Ch.

To enter STOP (or HALT) Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = 0FFH) immediately before the appropriate SLEEP instruction, as shown in the following code segment.

```
FF          NOP         ; clear the pipeline
6F          STOP        ; enter STOP Mode
 or
FF          NOP         ; clear the pipeline
7F          HALT        ; enter HALT Mode
```

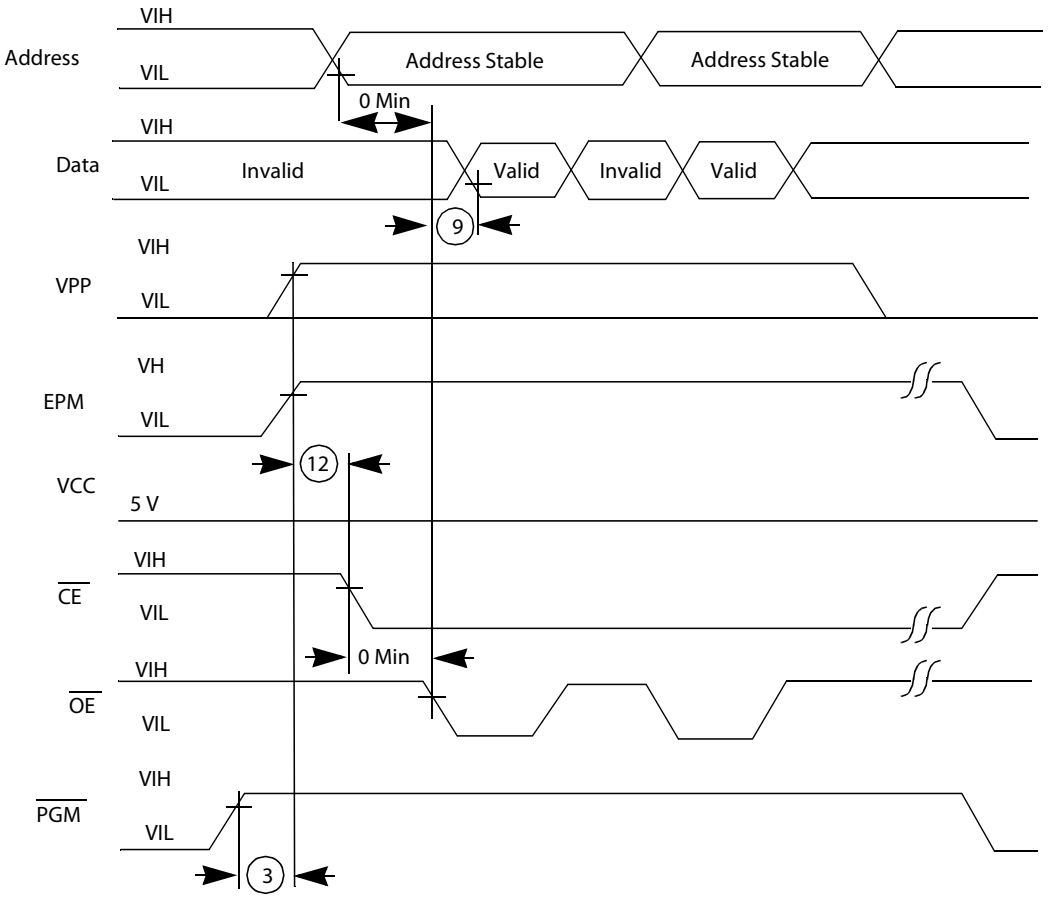

Figure 20. EPROM Read Timing

User MODE 2: EPROM Program

The Z86E61/Z86E63 MCU's Program function conforms to the Intelligent programming algorithm. The device is programmed with V_{CC}, at 6.0V and V_{PP} = 12.5V. Programming pulses are applied in 1 ms increments to a maximum of 25 pulses before proper verification. After verification, a programming pulse of three times the duration of the cycles necessary to program the device is issued to ensure proper programming. After all addresses are programmed, a final data comparison is executed and the programming cycle is complete. Timing for the Z86E61/Z86E63 MCU programming cycle is shown in Figure 21.

DC Characteristics

Table 35 lists voltage and direct current characteristics for the Z86E61/Z86E63 MCU under differing conditions. Be advised that I_{CC2} requires loading TMR (F1Hh) with any value prior to STOP execution. Use the following sequence:

```
LD TMR,#00
NOP
STOP
```

Table 35. Direct Current Characteristics

Symbol	Parameter	Min	Max	Typical @ 25°C	Units	Conditions
	Max Input Voltage		7		V	I_{IN} < 250µA.
	Max Input Voltage	13			V	P33–P30 Only.
V_{CH}	Clock Input High Voltage	3.8	V_{CC}+0.3		V	Driven by External Clock Generator.
V_{CL}	Clock Input Low Voltage	–0.3	0.8		V	Driven by External Clock Generator.
V_{IH}	Input High Voltage	2.0	V_{CC}+0.3		V	
V_{IL}	Input Low Voltage	–0.3	0.8		V	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –2.0mA.
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = +2.0mA.
V_{RH}	Reset Input High Voltage	3.8	V_{CC}+0.3		V	
V_{RL}	Reset Input Low Voltage	–0.3	0.8		V	
I_{IL}	Input Leakage	–10	10		µA	V_{IN} = 0V, 5.25V.
I_{OL}	Output Leakage	–10	10		µA	V_{IN} = 0V, 5.25V.
I_{IR}	Reset Input Current		–50		µA	V_{CC}=+5.25V; V_{RL}=0V.
I_{CC}	Supply Current		50	25	mA	@ 16MHz.
			60	35	mA	@ 20MHz.
I_{CC1}	Standby Current		15	5	mA	HALT Mode @ 16MHz; V_{IN}=0V, V_{CC}
			20	10	mA	HALT Mode @ 20MHz; V_{IN}=0V, V_{CC}
I_{CC2}	Standby Current		20	5	µA	STOP Mode V_{IN}=0V, V_{CC}

AC Characteristics

Figure 27 displays the timing characteristics for the Z86E61/Z86E63 MCU. The circled numbers in this figure reference a description in Table 36 of each symbol, its parameter and its frequency range for these 16MHz and 20MHz parts.

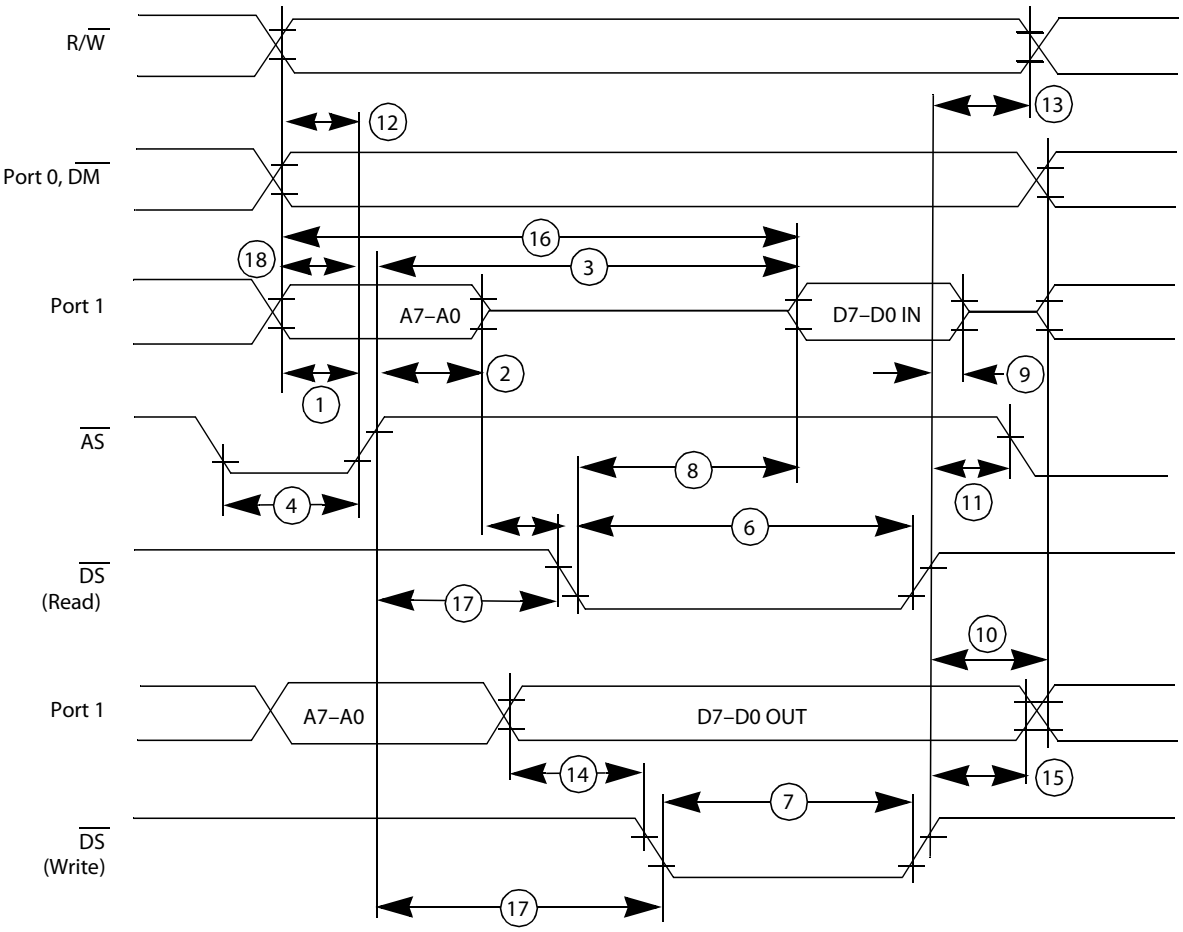

Figure 27. External I/O or Memory Read/Write Timing

Additional timing characteristics are shown in Figure 30 and described in Table 39.

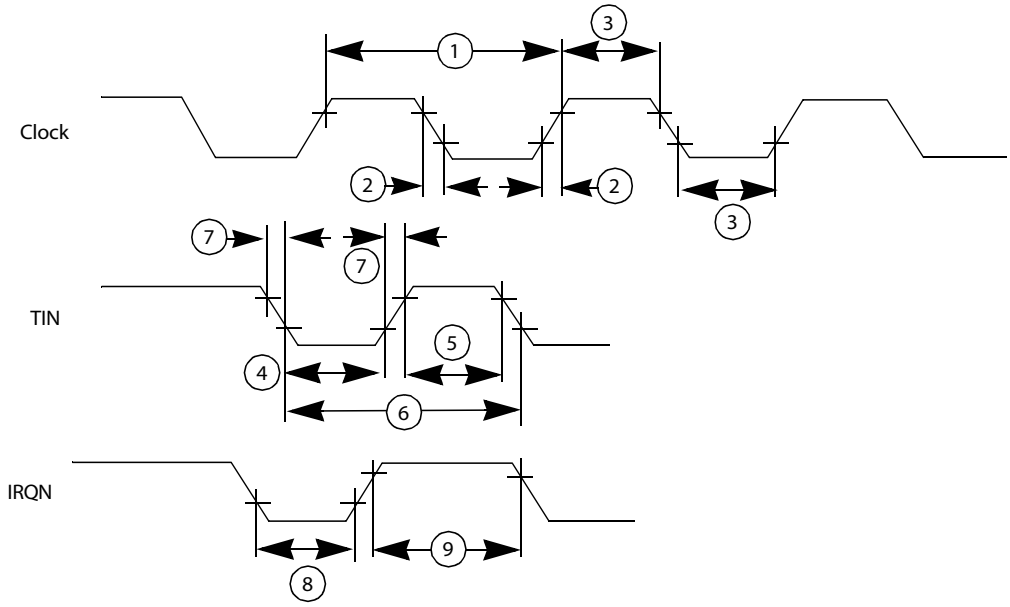

Figure 30. Additional Timing

Table 39. Additional Timing

			TA = 0°C to +70°C					
			16MHz[1]		20MHz			
No.	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	62.5	1000	50	1000	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times		10		15	ns	1
3	TwC	Input Clock Width	21		37		ns	1
4	$TwT_{IN}L$	Timer Input Low Width	50		75		ns	2
5	$TwT_{IN}H$	Timer Input High Width	5TpC		5TpC			2
6	TpT_{IN}	Timer Input Period	8TpC		8TpC			2
7	TrT_{IN},TfT_{IN}	Timer Input Rise & Fall times	100		100		ns	2

Notes:
1. Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
3. Interrupt request through Port 3 (P33–P31).
4. Interrupt request through Port 30.
5. Interrupt references request through Port 3.

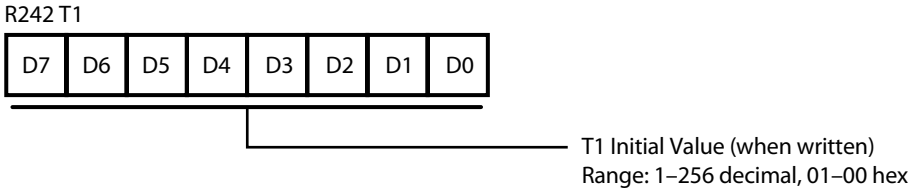

Figure 33. Counter/Timer 1 Register (F2H: Read/Write)

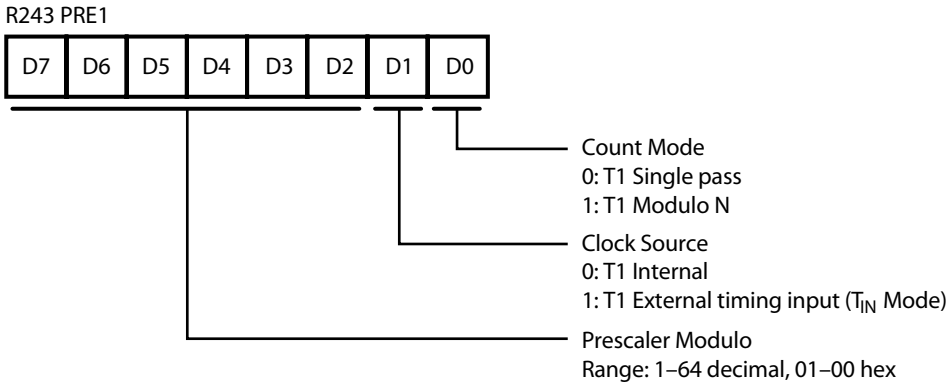

Figure 34. Prescaler 1 Register (F3H: Write Only)

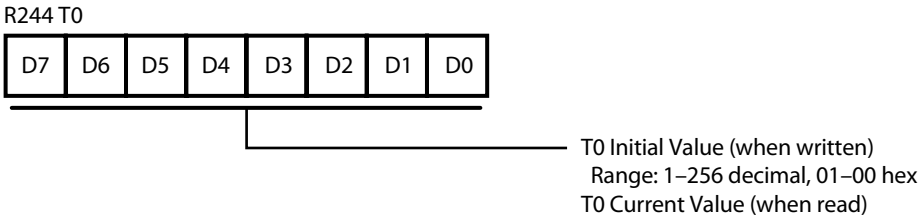

Figure 35. Counter/Timer 0 Register (F4H: Read/Write)

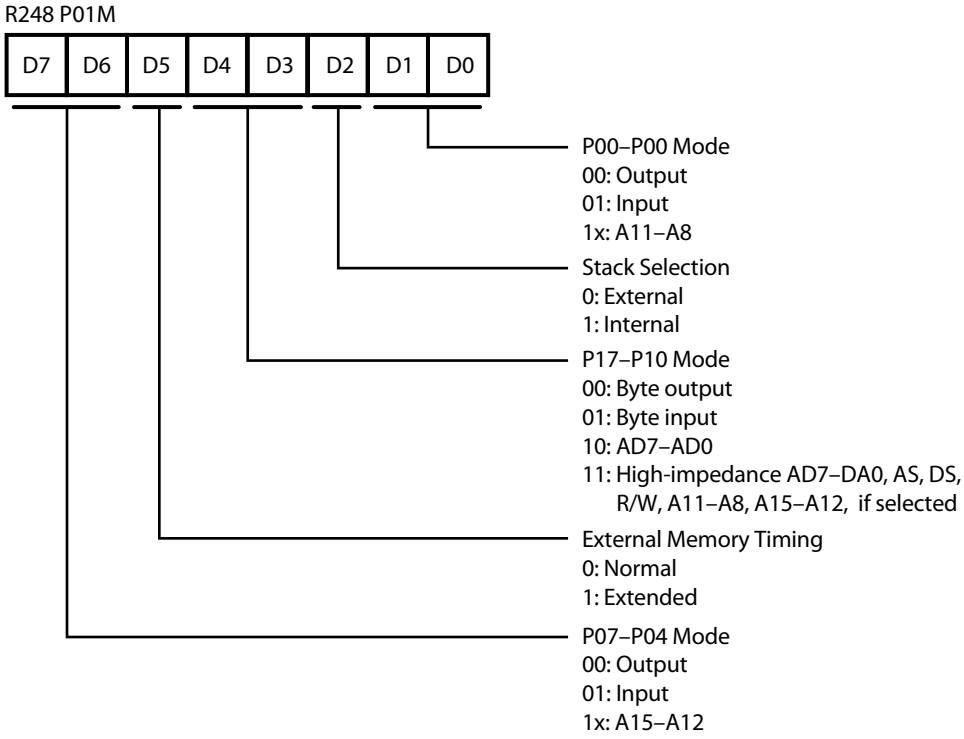

Figure 39. Port 0 and 1 Mode Register (F8H: Write Only)

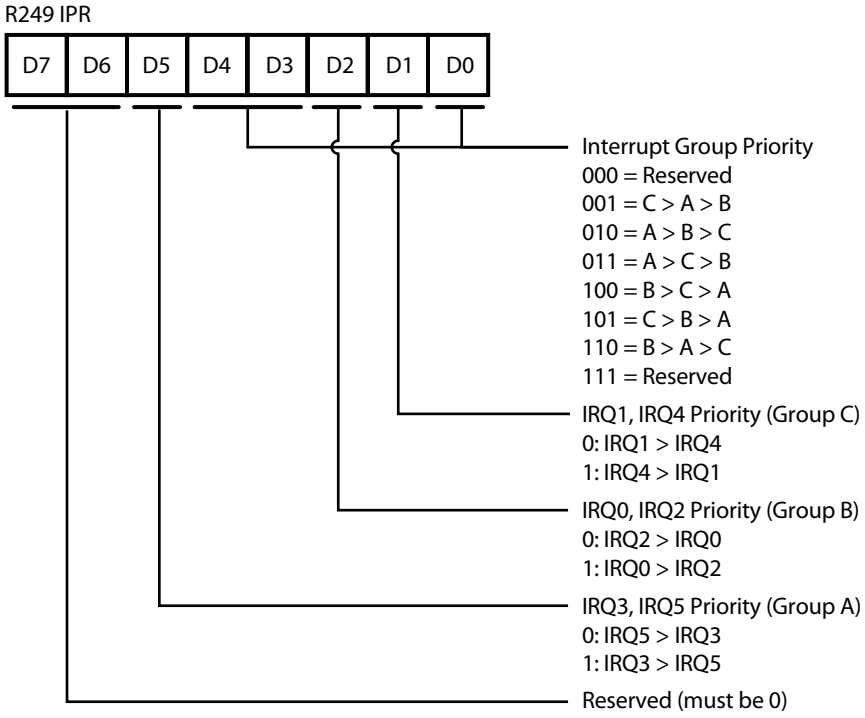

Figure 40. Interrupt Priority Register (F9H: Write Only)

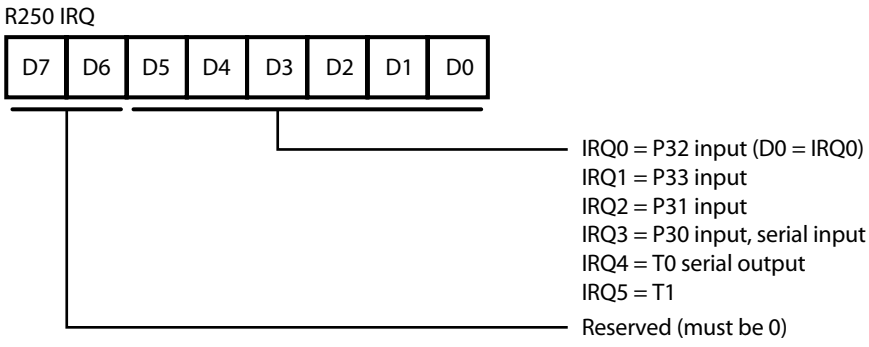

Figure 41. Interrupt Request Register (FAH: Read/Write)

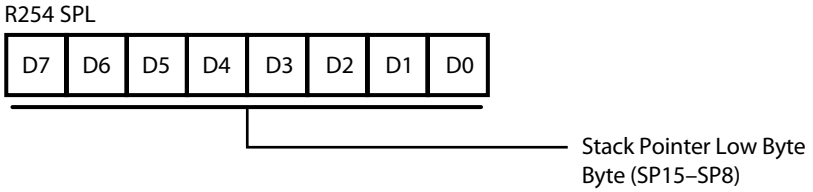

Figure 45. Stack Pointer Register (FEH: Read/Write)

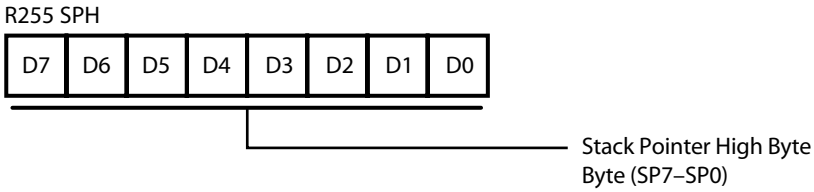

Figure 46. Stack Pointer Register (FFH: Read/Write)

Z8 Instruction Set

This section discusses the addressing modes, symbols, flags, condition codes and instruction formats that apply to the Z8 instruction set. A summary of the Z8 instruction set follows on page 55.

The notations listed in Table 40 are used to describe addressing modes and instruction operations.

Table 40. Instruction Set Notation

Notation	Definition
IRR	Indirect register pair or indirect working register pair address.
Irr	Indirect working register pair only.
X	Indexed address.
DA	Direct address.
RA	Relative address.
IM	Immediate.
R	Register or working register address.
r	Working register address only.
IR	Indirect register or indirect working register address.
Ir	Indirect working register address only.
RR	Register pair or working register pair address.

The symbols listed in Table 41are used to describe the Z8 instruction set.

Table 41. Instruction Set Symbols

Symbol	Definition
dst	Destination location or contents.
src	Source location or contents.
cc	Condition code.
@	Indirect address prefix.
SP	Stack Pointer.
PC	Program Counter.
FLAGS	Flag Register (Control Register 252).
RP	Register Pointer (R253).
IMR	Interrupt Mask Register (R251).

Table 45. Instruction Summary (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Op Code Byte (Hex)	Flags Affected C	Z	S	V	D	H
LD dst, src dst ← src	r	Im	rC	–	–	–	–	–	–
	r	R	r8						
	R	r	r9						
			r = 0 – F						
	r	X	C7						
	X	r	D7						
	r	Ir	E3						
	Ir	r	F3						
	R	R	E4						
	R	IR	E5						
	R	IM	E6						
	IR	IM	E7						
	IR	R	F5						
LDC dst, src dst ← src	r	Irr	C2	–	–	–	–	–	–
LDCI dst, src dst ← src r ← r + 1; rr ← rr + 1	Ir	Irr	C3	–	–	–	–	–	–
NOP			FF	–	–	–	–	–	–
OR dst, src dst ← dst OR src	See Note 1		4[1	–	*	*	0	–	–
POP dst ← @SP; SP ← SP + 1	R		50	–	–	–	–	–	–
	IR		51						
PUSH src SP ← SP – 1; @SP ← src	R		70	–	–	–	–	–	–
	IR		71						
RCF C ← 0			CF	0	–	–	–	–	–
RET PC ← @SP; SP ← SP + 2			AF	–	–	–	–	–	–
RL dst	R		90	*	*	*	*	–	–
	IR		91						

Note: These instructions have an identical set of addressing modes, which are encoded for brevity. The first Op Code nibble is found in this instruction set table. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found on the left of the applicable addressing mode pair in the Op Code Map in Figure 48.

For example, the op code of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Table 45. Instruction Summary (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Op Code Byte (Hex)	Flags Affected C	Z	S	V	D	H
RLC dst	R IR		10 11	*	*	*	*	–	–
RR dst	R IR		E0 E1	*	*	*	*	–	–
RRC dst	R IR		C0 C1	*	*	*	*	–	–
SBC dst, src dst ← dst ← src ← C	See Note 1		3[]	*	*	*	*	1	*
SCF C ← 1			DF	1	–	–	–	–	–
SRA dst	R IR		D0 D1	*	*	*	0	–	–
SRP dst RP ← src	Im		31	–	–	–	–	–	–
STOP			6F	1	–	–	–	–	–
SUB dst, src dst ← dst ← src	See Note 1		2[ ]	[	[	[	[	1	[
SWAP dst	R IR		F0 F1	X	*	*	X	–	–
TCM dst, src (NOT dst) AND src	See Note 1		6[ ]	–	*	*	0	–	–
TM dst, src dst AND src	See Note 1		7[ ]	–	*	*	0	–	–
XOR dst, src dst ← dst XOR src	See Note 1		B[ ]	–	*	*	0	–	–

Note: These instructions have an identical set of addressing modes, which are encoded for brevity. The first Op Code nibble is found in this instruction set table. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found on the left of the applicable addressing mode pair in the Op Code Map in Figure 48.

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