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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Multimedia
Core Processor	TM3260
Program Memory Type	-
Controller Series	Nexperia
RAM Size	-
Interface	I²C, 2-Wire Serial
Number of I/O	61
Voltage - Supply	1.23V ~ 1.37V
Operating Temperature	0°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	456-BGA
Supplier Device Package	456-BGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pnx1502e-557

Chapter 6: Boot Module

Chapter 7: PCI-XIO Module

Chapter 8: General Purpose Input Output Pins

PNX1500 uses different I/Os depending on the type of the interface, e.g. PCI, or electrical characteristics needed for the functionality, e.g. a clock signal requires sharper edges than a regular signal. The following table summarizes the types of I/Os, a.k.a. pads, used in PNX1500.

Table 1: PNX1500 I/O Types

Pad Type	Description
PCIT5V	PCI 2.2 compliant I/O using 3.3- or 5- V PCI signaling conventions.
IIC3M4SDAT5V IIC3M4SCLT5V	Open drain 3.3- or 5- V I^2C I/Os.
BPX2T14MCP	3.3-V low impedance output, with fast rise/fall time, combined with 3.3-V input only. Used for Clock signals requires board level 27-33 Ω series terminator resistor to match 50 Ω PCB trace.
BPTS1CP	3.3-V regular impedance output, with fast rise/fall time, combined with 3.3-V input only.
BPTS1CHP	3.3-V regular impedance output, with fast rise/fall time, combined with 3.3-V input only with hysteresis.
BPTS3CP	3.3-V regular impedance output, with slow rise/fall time, combined with 3.3-V input only.
BPTS3CHP	3.3-V regular impedance output, with slow rise/fall time, combined with 3.3-V input only with hysteresis.
BPT3MCHT5V	3.3-V regular impedance output, with slow rise/fall time, combined with 5-V tolerant input with hysteresis.
BPT3MCHDT5V	3.3-V regular impedance output, with slow rise/fall time, combined with 5-V tolerant input with hysteresis and internal pull-down. **Note:** The pull-down is NOT strong enough to actually pull down a 5-V TTL input. Instead the TTL input pin sees a ‘1’.
IPCP	3.3-V input only.
IPCHP	3.3-V input only with hysteresis.
SSTLCLKIO	SSTL_2 low impedance, e.g. DDR SDRAM clocks. Requires a board level 10 Ω series terminator resistor to match a 50 Ω PCB trace.
SSTLADDIO	SSTL_2 low impedance for output signals, e.g. DDR SDRAM address and control signals. Requires a board level matched 50 Ω PCB trace.
SSTLDATIO	SSTL_2 low impedance for DDR SDRAM data signals. Requires a board level matched 50 Ω PCB trace.

The above pad types are used in the modes listed in the following table

Table 2: PNX1500 I/O Modes

Modes	Description
IN	Input only, except during boundary scan or GPIO mode.
OUT	Output only, except when used as a GPIO pin.
OD	Open drain output - active pull low, no active drive high, requires external pull-up.
I/O	Input or Output.
I/OD	Input or open drain output - active pull low, no active drive high, requires external pull-up.
I/O/D	Input or output or open drain output with input - active pull low, no active drive high, requires external pull-up when operated in open drain mode.
O	Output or floating.

Unused pins may remain unconnected, i.e. floating if they contain an internal pull-up or pull-down. More specifically,

6.1 Input Clock Specification

Table 20: Specification of HC-49U 27.00000 MHZ Crystal

Frequency	27.00000 MHZ fundamental
Temperature range	0˚C to 85˚C
Typical Load Capacitance (C_L)	10 pF
Frequency accuracy (all included: temperature, aging, frequency at 0 to 85˚C)	+/- 30 ppm
Series resonance resistor	130 Ω max.
Shunt capacitance (C_P)	7 pF max.
Drive level	1mW max.
External capacitance (C_{X1}, C_{X2} Figure 1)	18 pF max. each

Table 21: Specification of the Oscillator Mode

Frequency	27.00000 MHZ
Temperature range	0˚C to 85˚C
Duty Cycle	45-55% maximum assymetry
Frequency accuracy (all included: temperature, aging, frequency at 0 to 85˚C)	+/-50 ppm
Rising/Falling Times	Maximum 3ns, Minimum 1 ns
Minimum Input High Voltage, V_{IH}	0.8*V_{DD}
Maximum Input Low Voltage, V_{IL}	0.2*V_{DD}

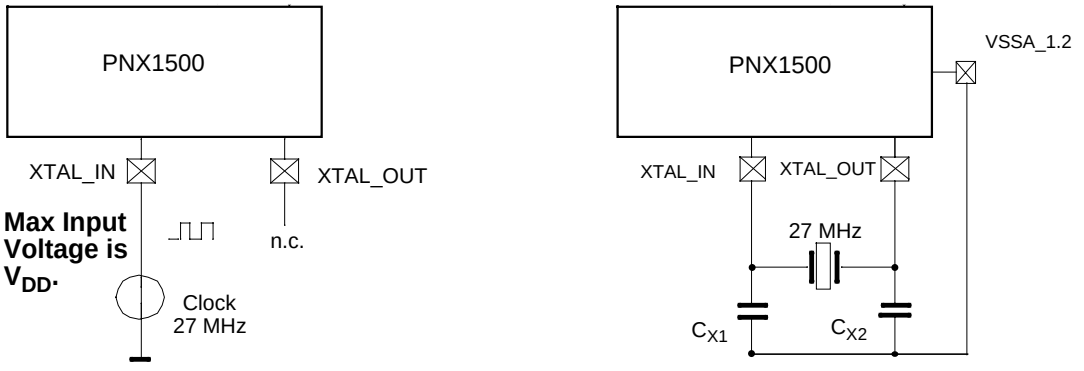


Figure 1: Application Diagram of the Crystal Oscillator

6.2 SSTL_2 type I/O Circuit

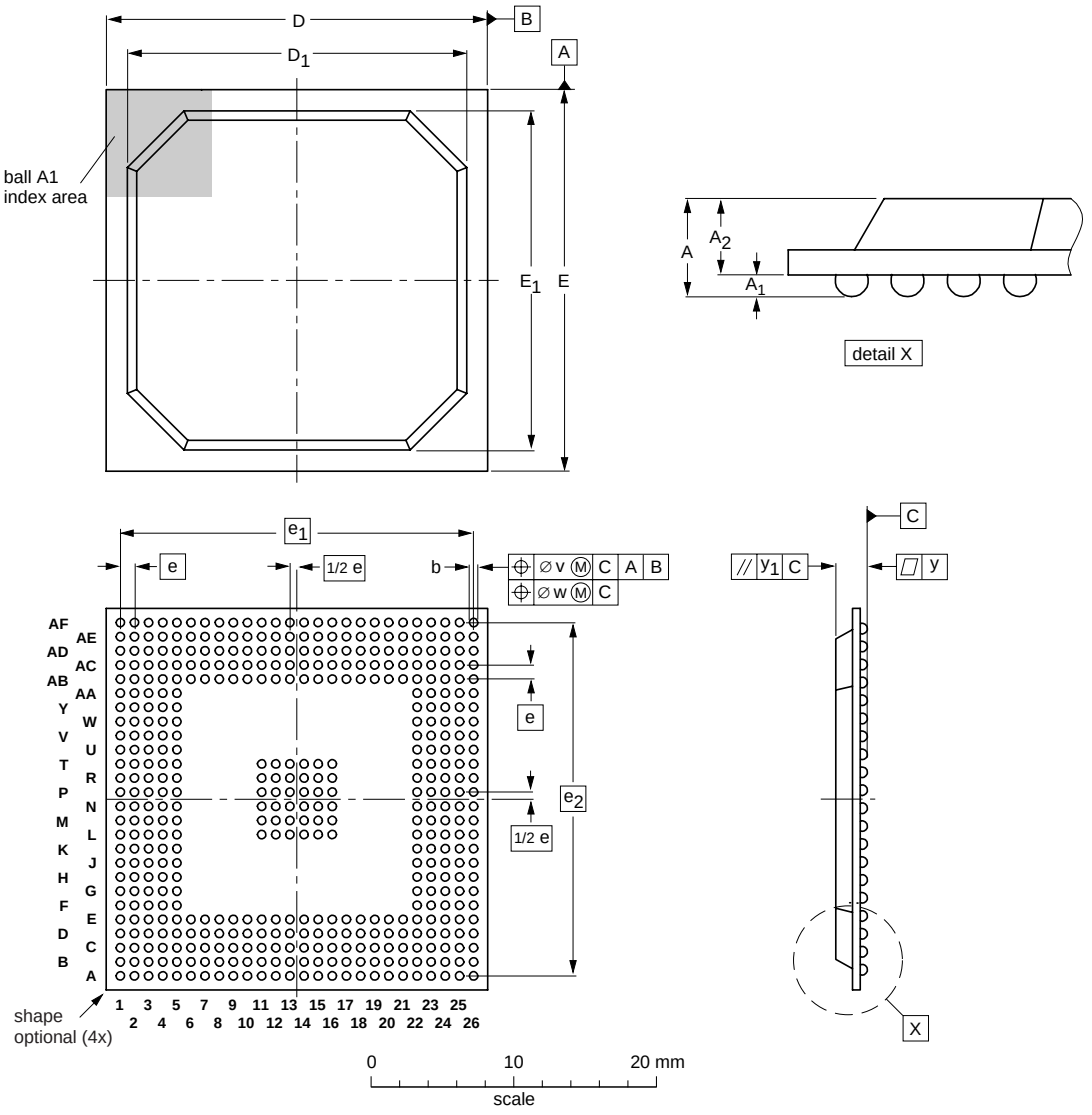
Table 22: SSTL_2 AC/DC Characteristics

Symbol	Parameter	Condition/Notes	Min	Typ	Max	Unit	Notes
V_{OH}	Output High Voltage		0.9V_{CCM}			V	
V_{OL}	Output Low Voltage				0.1V_{CCM}	V	
V_{IH}	DC Input High Voltage	This is the overshoot/ undershoot protection specification of the pad			V_{CCM} + 0.3	V	
V_{IL}	DC Input Low Voltage		-0.3			V	

8. Package Outline

Latest information may be found at http://www.semiconductors.philips.com/package/SOT795-1.html

BGA456: plastic ball grid array package; 456 balls; body 27 x 27 x 1.75 mm **SOT795-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	D_1	E	E_1	e	e_1	e_2	v	w	y	y_1
mm	2.45	0.6 0.4	1.85 1.60	0.7 0.5	27.2 26.8	24.75 23.75	27.2 26.8	24.75 23.75	1	25	25	0.3	0.15	0.2	0.35

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT795-1	144E	MS-034	- - -			02-11-18

Figure 23: BGA456 Plastic Ball grid Array; 456 Balls; body 27 x 27 x 1.75 mm

Table 7: External Clocks

Signal Name	Frequency	IN/OUT	PIN I/O Name	Description
mm_clk_out, clk_mem	up to 200 MHz	OUT	MM_CLK MM_CLK#	DDR SDRAM clock output
clk_vip	up to 81 MHz	IN/OUT	VDI_CLK1	VIP clock
clk_fgpi	up to 100 MHz	IN/OUT	VDI_CLK2	FGPI clock
clk_qvcp	up to 81 MHz	IN/OUT	VDO_CLK1	QVCP clock
clk_fgpo	up to 100 MHz	IN/OUT	VDO_CLK2	FGPO clock
ai_osclk	up to 50 MHz	OUT	AI_OSCLK	Audio Input oversampling clock
ai_sck	up to 25 MHz	IN/OUT	AI_SCK	Audio Input input/output bit clock
ao_osclk	up to 50 MHz	OUT	AO_OSCLK	Audio Output oversampling clock
ao_sck	up to 25 MHz	IN/OUT	AO_SCK	Audio Output input/output bit clock
clk_lan	up to 50 MHz	OUT	LAN_CLK	To 10/100 MAC PHY clock
clk_lan_tx	up to 27 MHz	IN	LAN_TX_CLK	From 10/100 MAC PHY transmit clock
clk_lan_rx	up to 27 MHz	IN	LAN_RX_CLK	From 10/100 MAC PHY receive clock
clk_gpio_4q	up to 108 MHz	IN/OUT	GPIO04	GPIO sampling/pattern generation clock
clk_gpio_5q	up to 108 MHz	IN/OUT	GPIO05	GPIO sampling/pattern generation clock
clk_gpio_6q_12	up to 108 MHz	IN/OUT OUT	GPIO06 GPIO12	GPIO sampling/pattern generation clock GPIO board level clock
clk_gpio_13	up to 108 MHz	OUT	GPIO13	GPIO board level clock
clk_gpio_14	up to 108 MHz	OUT	GPIO14	GPIO board level clock

Remark: Refer to Chapter _ to see series resistors board requirements.

Table 8: Bypass Clock Sources

Clocks from Clock Module	Bypass Control Register	GPIO pin Assignment
clk_qvcp	CLK_QVCP_OUT_CTL	XIO_ACK
clk_qvcp_pix	CLK_QVCP_PIX_CTL	XIO_D[8]
clk_qvcp_proc	CLK_QVCP_PROC_CTL	XIO_D[9]
clk_lcd_tstamp	CLK_LCD_TSTAMP_CTL	XIO_D[10]
clk_vip	CLK_VIP_CTL	XIO_D[11]
clk_vld	CLK_VLD_CTL	XIO_D[12]
ai_osclk	AI_OSCLK_CTL	XIO_D[13]
ao_osclk	AO_OSCLK_CTL	XIO_D[14]
clk_spdo	CLK_SPDO_CTL	XIO_D[15]
clk_spdi	CLK_SPDI_CTL	LAN_TXD[0]
clk_gpio_q4	CLK_GPIO_Q4_CTL	LAN_TXD[1]
clk_gpio_q5	CLK_GPIO_Q5_CTL	LAN_TXD[2]
clk_gpio_q6_12	CLK_GPIO_Q6_12_CTL	LAN_TXD[3]
clk_gpio_13	CLK_GPIO_13_CTL	LAN_RXD[0]
clk_gpio_14	CLK_GPIO_14_CTL	LAN_RXD[1]
clk_fgpo	CLK_FGPO_CTL	LAN_RXD[2]
clk_fgpi	CLK_FGPI_CTL	LAN_RXD[3]

2.5 Power-up and Reset sequence

On power-up, the Clock module outputs the default 27 MHz clocks to all the PNX15xx Series modules. Once the Reset module has released the internal module resets, the boot-up sequence executed by the Boot module starts off the 27 MHz clock. At some point in the boot up sequence, the Boot module switches TM3260 and the DDR clocks to the associated PLLs, PLL0 and PLL2. The Clock module keeps feeding the other PNX15xx Series modules with the initial 27 MHz clock until the software decides otherwise.

2.6 Clock Stretching

The TM3260 clock, clk_tm, can be paused or stretched for one clock pulse. A counter counts to a pre-programmed value. When this value is reached the clock gating circuit will turn off the TM3260 clock for one clock period. Then the TM3260 clock is turned back on.

The procedure to operate the clock stretching circuit is to program the CLK_STRETCHER_CTL MMIO register to the value desired between clock stretches. For example a value of 3 turns off the clock every 3 clocks as pictured in Figure 5.

A Write to the CLK_STRETCHER_CTL register acts as the enable for the feature.

4. MMIO Registers

Table 6: Register Summary

	Name	Description
0x10,4000	Mode Control 0	The Mode Control bit pairs which control GPIO pins 15-0.
0x10,4004	Mode Control 1	The Mode Control bit pairs which control GPIO pins 31-16.
0x10,4008	Mode Control 2	The Mode Control bit pairs which control GPIO pins 47-32.
0x10,400C	Mode Control 3	The Mode Control bit pairs which control GPIO pins 60-48.
0x10,4010	MASK and IO Data 0	MASK and IO data for GPIO pins 15-0.
0x10,4014	MASK and IO Data 1	MASK and IO data for GPIO pins 31-16.
0x10,4018	MASK and IO Data 2	MASK and IO data for GPIO pins 47-32.
0x10,401C	MASK and IO Data 3	MASK and IO data for GPIO pins 60-48.
0x10,4020	Internal Signals	Internal signals to be timestamped, software readable.
0x10,4024	GPIO_EV0	GPIO signal monitoring OR pattern generation control register for FIFO queue 0.
0x10,4028	GPIO_EV1	GPIO signal monitoring OR pattern generation control register for FIFO queue 1.
0x10,402C	GPIO_EV2	GPIO signal monitoring OR pattern generation control register for FIFO queue 2.
0x10,4030	GPIO_EV3	GPIO signal monitoring OR pattern generation control register for FIFO queue 3.
0x10,4034	GPIO_EV4	GPIO signal monitoring control register for timestamp unit 0
0x10,4038	GPIO_EV5	GPIO signal monitoring control register for timestamp unit 1
0x10,403C	GPIO_EV6	GPIO signal monitoring control register for timestamp unit 2
0x10,4040	GPIO_EV7	GPIO signal monitoring control register for timestamp unit 3
0x10,4044	GPIO_EV8	GPIO signal monitoring control register for timestamp unit 4
0x10,4048	GPIO_EV9	GPIO signal monitoring control register for timestamp unit 5
0x10,404C	GPIO_EV10	GPIO signal monitoring control register for timestamp unit 6
0x10,4050	GPIO_EV11	GPIO signal monitoring control register for timestamp unit 7
0x10,4054	GPIO_EV12	GPIO signal monitoring control register for timestamp unit 8
0x10,4058	GPIO_EV13	GPIO signal monitoring control register for timestamp unit 9
0x10,405C	GPIO_EV14	GPIO signal monitoring control register for timestamp unit 10
0x10,4060	GPIO_EV15	GPIO signal monitoring control register for timestamp unit 11
0x10,4064	IO_SEL0	IO Select register for FIFO queue 0
0x10,4068	IO_SEL1	IO Select register for FIFO queue 1
0x10,406C	IO_SEL2	IO Select register for FIFO queue 2
0x10,4070	IO_SEL3	IO Select register for FIFO queue 3
0x10,4074	PG_BUF_CTRL0	Pattern Generation DMA buffer control register. for FIFO queue 0
0x10,4078	PG_BUF_CTRL1	Pattern Generation DMA buffer control register. for FIFO queue 1
0x10,407C	PG_BUF_CTRL2	Pattern Generation DMA buffer control register for FIFO queue 2.
0x10,4080	PG_BUF_CTRL3	Pattern Generation DMA buffer control register for FIFO queue 3.
0x10,4084	BASE1_PTR0	Base address for DMA buffer 1 of FIFO queue 0.
0x10,4088	BASE1_PTR1	Base address for DMA buffer 1 of FIFO queue 1.
0x10,408C	BASE1_PTR2	Base address for DMA buffer 1 of FIFO queue 2.

Table 18: GPIO Module Status Register for all 12 Timestamp Units

Bit	Symbol	Access	Value	Description
5	DATA_VALID_5	R	0	Data in TSU 5 is ready to be read.
4	DATA_VALID_4	R	0	Data in TSU 4 is ready to be read.
3	DATA_VALID_3	R	0	Data in TSU 3 is ready to be read.
2	DATA_VALID_2	R	0	Data in TSU 2 is ready to be read.
1	DATA_VALID_1	R	0	Data in TSU 1 is ready to be read.
0	DATA_VALID_0	R	0	Data in TSU 0 is ready to be read.
Offset 0x10,4FE4	***INT_ENABLE4***			
31:24	Unused		-	
23	INT_OE_11_EN	R/W	0	Internal overrun interrupt enable register for TSU 11 0 - Interrupt disabled 1 - Interrupt enabled
22	INT_OE_10_EN	R/W	0	Internal overrun interrupt enable register for TSU 10 0 - Interrupt disabled 1 - Interrupt enabled
21	INT_OE_9_EN	R/W	0	Internal overrun interrupt enable register for TSU 9 0 - Interrupt disabled 1 - Interrupt enabled
20	INT_OE_8_EN	R/W	0	Internal overrun interrupt enable register for TSU 8 0 - Interrupt disabled 1 - Interrupt enabled
19	INT_OE_7_EN	R/W	0	Internal overrun interrupt enable register for TSU 7 0 - Interrupt disabled 1 - Interrupt enabled
18	INT_OE_6_EN	R/W	0	Internal overrun interrupt enable register for TSU 6 0 - Interrupt disabled 1 - Interrupt enabled
17	INT_OE_5_EN	R/W	0	Internal overrun interrupt enable register for TSU 5 0 - Interrupt disabled 1 - Interrupt enabled
16	INT_OE_4_EN	R/W	0	Internal overrun interrupt enable register for TSU 4 0 - Interrupt disabled 1 - Interrupt enabled
15	INT_OE_3_EN	R/W	0	Internal overrun interrupt enable register for TSU 3 0 - Interrupt disabled 1 - Interrupt enabled
14	INT_OE_2_EN	R/W	0	Internal overrun interrupt enable register for TSU 2 0 - Interrupt disabled 1 - Interrupt enabled
13	INT_OE_1_EN	R/W	0	Internal overrun interrupt enable register for TSU 1 0 - Interrupt disabled 1 - Interrupt enabled

Table 21: GPIO IO_SEL Selection Values

Signal	CLOCK_SEL/ IO_SEL (hex)	MODE
SPDIF_O	0x39	Signal Monitoring; Pattern Generation
SPDIF_I	0x38	Signal Monitoring; Pattern Generation
VDO_AUX	0x37	Signal Monitoring; Pattern Generation
VDO_D[33]	0x36	Signal Monitoring; Pattern Generation
VDO_D[32]	0x35	Signal Monitoring; Pattern Generation
VDI_D[33]	0x34	Signal Monitoring; Pattern Generation
VDI_D[32]	0x33	Signal Monitoring; Pattern Generation
LAN_MDC	0x32	Signal Monitoring; Pattern Generation
LAN_MDIO	0x31	Signal Monitoring; Pattern Generation
LAN_RX_ER	0x30	Signal Monitoring; Pattern Generation
LAN_RX_DV	0x2F	Signal Monitoring; Pattern Generation
LAN_RXD[3]	0x2E	Signal Monitoring; Pattern Generation
LAN_RXD[2]	0x2D	Signal Monitoring; Pattern Generation
LAN_RXD[1]	0x2C	Signal Monitoring; Pattern Generation
LAN_RXD[0]	0x2B	Signal Monitoring; Pattern Generation
LAN_COL	0x2A	Signal Monitoring; Pattern Generation
LAN_CRS	0x29	Signal Monitoring; Pattern Generation
LAN_TX_ER	0x28	Signal Monitoring; Pattern Generation
LAN_TXD[3]	0x27	Signal Monitoring; Pattern Generation
LAN_TXD[2]	0x26	Signal Monitoring; Pattern Generation
LAN_TXD[1]	0x25	Signal Monitoring; Pattern Generation
LAN_TXD[0]	0x24	Signal Monitoring; Pattern Generation
LAN_TX_EN	0x23	Signal Monitoring; Pattern Generation
XIO_D[7]	0x22	Signal Monitoring; Pattern Generation
XIO_D[6]	0x21	Signal Monitoring; Pattern Generation
XIO_D[5]	0x20	Signal Monitoring; Pattern Generation
XIO_D[4]	0x1F	Signal Monitoring; Pattern Generation
XIO_D[3]	0x1E	Signal Monitoring; Pattern Generation
XIO_D[2]	0x1D	Signal Monitoring; Pattern Generation
XIO_D[1]	0x1C	Signal Monitoring; Pattern Generation
XIO_D[0]	0x1B	Signal Monitoring; Pattern Generation
XIO_ACK	0x1A	Signal Monitoring; Pattern Generation
AO_SD[3]	0x19	Signal Monitoring; Pattern Generation
AO_SD[2]	0x18	Signal Monitoring; Pattern Generation
AO_SD[1]	0x17	Signal Monitoring; Pattern Generation
AO_SD[0]	0x16	Signal Monitoring; Pattern Generation
AO_WS	0x15	Signal Monitoring; Pattern Generation

Table 20: QVCP 1 Registers *...Continued*

Bit	Symbol	Access	Value	Description
Offset 0x10 E2F8	***LSHR_E_max***			
31:10	Unused		-	
9:0	LSHR_E_max	R	0	Statistics on one of the sharpness filter max measurement value = 10bU
Offset 0x10 E2FC	***LSHR_E_sum***			
31:26	Unused		-	
25:0	LSHR_E_sum	R	0	Statistics on one of the sharpness filter sum of abs max energy value = 26bU
Offset 0x10 E300	***LSHR Measurement Window Start***			
31:27	Reserved			
26:16	LSHR_MW_START_Y	R/W	0	LSHR measurement window start line (The first line included in the measurement window, the layer start position is (0,0)).
15:11	Reserved			
10:0	LSHR_MW_START_X	R/W	0	LSHR measurement window start pixel
Offset 0x10 E304	***LSHR Measurement Window End***			
31:27	Reserved			
26:16	LSHR_MW_END_Y	R/W	7FF	LSHR measurement window end line (The last line included in the measurement window)
15:11	Reserved			
10:0	LSHR_MW_END_X	R/W	7FF	LSHR measurement window end pixel
Offset 0x10 E320	***Layer Solid Color***			
31	SC_enable	R/W	0	This bit enables the replacement of the layer input by the specified color. 1 = Replace 0 = Use layer input
30:24	Unused		-	
23:16	Upper	R/W	0	Upper channel of the replacement color (R/Y) (two's complement)
15:8	Middle	R/W	0	Middle channel of the replacement color (G/U) (two's complement)
7:0	Lower	R/W	0	Lower channel of the replacement color (B/V) (two's complement)
Offset 0x10 E324	***Layer LUT-HIST Bins 00 to 03***			
31:24	bin03	R/W	0	8-bit signed offset from a Yout=Yin Curve for Yin=-192+ped register
23:16	bin02	R/W	0	8-bit signed offset from a Yout=Yin Curve for Yin=-208+ped register
15:8	bin01	R/W	0	8-bit signed offset from a Yout=Yin Curve for Yin=-224+ped register
7:0	bin00	R/W	0	8-bit signed offset from a Yout=Yin Curve for Yin=-240+ped register
Offset 0x10 E328	***Layer LUT-HIST Bins 04 to 07***			
31:24	bin07	R/W	0	8-bit signed offset from a Yout=Yin Curve for Yin=-128+ped register
23:16	bin06	R/W	0	8-bit signed offset from a Yout=Yin Curve for Yin=-144+ped register
15:8	bin05	R/W	0	8-bit signed offset from a Yout=Yin Curve for Yin=-160+ped register
7:0	bin04	R/W	0	8-bit signed offset from a Yout=Yin Curve for Yin=-176+ped register

Table 3: Fast general purpose output (FGPO) *…Continued*

Bit	Symbol	Access	Value	Description
1:0	Reserved	R	0	Always 0.
Offset 0x07,1018	***FGPO_NREC1***			
31:24	Reserved	R	0	To ensure software backward compatibility unused or reserved bits must be written as zeros and ignored upon read.
23:0	NREC1	R	0	Number of records/messages output from buffer 1. Cleared to zero when FGPO_BASE1 register is written to.
Offset 0x07,101C	***FGPO_NREC2***			
31:24	Reserved	R	0	To ensure software backward compatibility unused or reserved bits must be written as zeros and ignored upon read.
23:0	NREC2	R	0	Number of records/messages output from buffer 2. Cleared to zero when FGPO_BASE1 register is written to.
Offset 0x07,1020	***FGPO_THRESH1***			
31:24	Reserved	R	0	To ensure software backward compatibility unused or reserved bits must be written as zeros and ignored upon read.
23:0	THRESH1	R/W	0	THRESH1_REACHED interrupt generated when FGPO_NREC1 count equals this register value. Range: **1 to 2^{24}-1**
Offset 0x07,1024	***FGPO_THRESH2***			
31:24	Reserved	R	0	To ensure software backward compatibility unused or reserved bits must be written as zeros and ignored upon read.
23:0	THRESH2	R/W	0	THRESH2_REACHED interrupt generated when FGPO_NREC2 count equals this register value. Range: **1 to 2^{24}-1**
Offset 0x07,1028	***FGPO_REC_GAP***			
31:24	Reserved	R	0	To ensure software backward compatibility unused or reserved bits must be written as zeros and ignored upon read.
23:0	REC_GAP	R/W	0	Clock delay after a record/message is output before the next record/message is output. Range: **1 to 2^{24}-1**
Offset 0x07,102C	***FGPO_BUF_GAP***			
31:24	Reserved	R	0	To ensure software backward compatibility unused or reserved bits must be written as zeros and ignored upon read.
23:0	BUF_GAP	R/W	0	Clock delay after a buffer is output before the next buffer is output. Range: **1 to 2^{24}-1**
Offset 0x07,1030	***FGPO_TIME1***			
31:0	TIME1	R	0	Holds timestamp when buffer 1 completed.
Offset 0x07,1034	***FGPO_TIME2***			
31:0	TIME2	R	0	Holds timestamp when buffer 2 completed.

4.2 Status Registers

3.3 PNX1300 Series Message Passing Mode

PNX1300 Series Message Passing mode can be emulated by setting FGPI_SIZE to 1 and only enabling buffer 1 (FGPI_CTL.CAPTURE_ENABLE_1 = ‘1’).

3.4 Record Capture Mode

Only active clock edges where fgpi_d_valid is asserted ‘1’ allow data samples to be captured.

If FGPI_REC_SIZE is not a multiple of 4 bytes, the record will be written to main memory as a series of 32-bit words. Only the last word is padded with zeroes in the unused bit positions.

Record start is signaled on the fgpi_start (fgpi_rec_start) pin. See FGPI_CTL.MSG_START (REC_SYNC) for selecting which edge will be active.

Buffer switching is signaled on the fgpi_stop (fgpi_buf_start) pin. See FGPI_CTL.MSG_STOP (BUF_SYNC) for selecting which buffer sync method will be used.

3.4.1 Record Synchronization

Starting capture of sample data for each record is signaled by a record start event (selected by the FGPI_CTL.REC_SYNC bits):

- a rising edge on fgpi_start (fgpi_rec_start) pin
- a falling edge on fgpi_start (fgpi_rec_start) pin
- occur immediately after the previous buffer is filled or when capture is started

(see Section 3.1.5 on page 14-13 for signal definitions for rising and falling edges).

The record ends by reaching the programmed record size in the FGPI_REC_SIZE register or by the next record start event, whichever comes first.

For rising and falling edge record start events the record may reach the programmed record size before the next record start event starts a new record. In this case the FGPI will stop sampling data and wait for the next record start event to continue filling the current buffer. The record may also be terminated by receiving the next record start event before the end of the current record. In this case the record is only partially filled, the content of the rest of the record is undefined.

When no record sync is used data is sampled continuously. This leads to back-to-back recording of consecutive records, independent of the fgpi_start (fgpi_rec_start) pin state. Each record is exactly the programmed size in the FGPI_REC_SIZE register.

3.4.2 Buffer Synchronization

Refer to Figure 5 on page 14-12 for the following section.

It is possible to further synchronize the recording of sample data to a buffer start event. (selected by the FGPI_CTL.BUF_SYNC bits):

It is legal to program the control field positions within the frame such that CC1 and CC2 overlap each other and/or left and right data fields. If two fields are defined to start at the same bit position, the priority is left (highest), right, CC1 then CC2. The field with the highest priority will be emitted starting at the conflicting bit position. If a field *f2* is defined to start at a bit position *i* that falls within a field *f1* starting at a lower bit position, *f2* will be emitted starting from *i* and the rest of *f1* will be lost. Any bit positions not belonging to a data or control field will be emitted as zero.

If a field is defined to start at a bit position such that the end of the field goes beyond the end of the frame, the data beyond the end of the frame (as defined by the active edge of WS) is lost.

Figure 5 shows a 64-bit frame suitable for use with the CS4218 codec. It is obtained by setting POLARITY=1, LEFTPOS=0, RIGHTPOS=32, DATAMODE=0, SSPOS=0, CLOCK_EDGE=1, WS_PULSE=1, CC1_POS= 16, CC1_EN=1, CC2_POS=48 and CC2_EN=1.

Note that frames are generated (externally or internally) even when TRANS_ENABLE is de-asserted. Writes to CC1 and CC2 should only be done after TRANS_ENABLE is asserted. The ‘first’ CC values will then go out on the next frame.

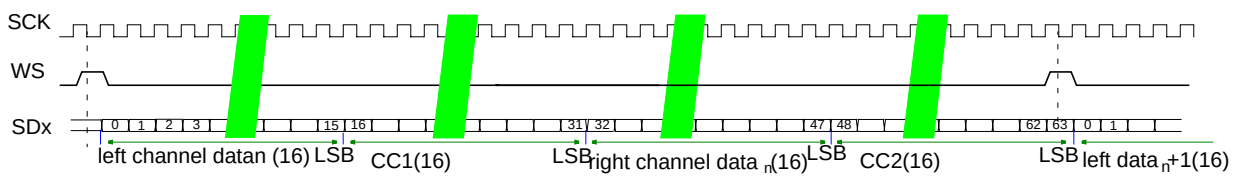


Figure 5: Example Codec Frame Layout for a Crystal Semiconductor CS4218

2.8 Data Bus Latency and HBE

The Audio Out unit relies on the FIFO buffers within the DMA interface adapter as well as an output holding register that holds a single mono sample or single stereo sample pair. For Audio Out there are four separate stereo output channels and each output channel has one output holding register. The holding register width is 64 bits.

Under normal operation, the DMA interface adapter provides samples from memory fast enough to avoid any missing samples. Meanwhile, data is being emitted from one 64-byte hardware buffer and holding register. If the data bus arbiter is set up with an insufficient latency guarantee, the situation can arise that the hardware FIFO buffer within the DMA interface adapter is not refilled in time and the buffer and holding register are exhausted by the time a new output sample is due. In that case the HBE flag is raised to indicate a bandwidth error. The last sample for each channel will be repeated until the buffer is refreshed. The HBE condition is sticky and can only be cleared by an explicit ACK_HBE. This condition indicates an incorrect setting of the data bus bandwidth arbiter.

Table 6 shows the maximum tolerable latency for a number of common operating modes. The right most column in the table indicates the maximum tolerable latency for Audio Out under normal operating condition. To sustain error free audio playback, one 64-byte DMA transfer must be completed within the maximum latency period

Table 6: SPDIF Input Registers *…Continued*

Bit	Symbol	Access	Value	Description
Offset 0x10 A034 SPDI_UBITS2				
31:0	UBITS [31:0]	R	0	User bit 2 contains the state of user bytes 4, 5, 6 and 7 of the block according to SPDI_CTL.UCBITS_SEL. The SPDI_UBITS register will always reflect the condition of the current decoded block of 192 frames. Register bit meaning will depend upon the source transmission.
Offset 0x10 A038 SPDI_UBITS3				
31:0	UBITS [31:0]	R	0	User bit 3 contains the state of user bytes 8, 9, 10 and 11 of the block according to SPDI_CTL.UCBITS_SEL. The SPDI_UBITS register will always reflect the condition of the current decoded block of 192 frames. Register bit meaning will depend upon the source transmission.
Offset 0x10 A03C SPDI_UBITS4				
31:0	UBITS [31:0]	R	0	User bit 4 contains the state of user bytes 12, 13, 14 and 15 of the block according to SPDI_CTL.UCBITS_SEL. The SPDI_UBITS register will always reflect the condition of the current decoded block of 192 frames. Register bit meaning will depend upon the source transmission.
Offset 0x10 A040 SPDI_UBITS5				
31:0	UBITS [31:0]	R	0	User bit 5 contains the state of user bytes 16, 17, 18 and 19 of the block according to SPDI_CTL.UCBITS_SEL. The SPDI_UBITS register will always reflect the condition of the current decoded block of 192 frames. Register bit meaning will depend upon the source transmission.
Offset 0x10 A044 SPDI_UBITS6				
31:0	UBITS [191:159]	R	0	User bit 6 contains the state of user bytes 20, 21, 22 and 23 of the block according to SPDI_CTL.UCBITS_SEL. The SPDI_UBITS register will always reflect the condition of the current decoded block of 192 frames. Register bit meaning will depend upon the source transmission.
Offset 0x10 A048—AFDC Reserved				
Offset 0x10 AFE0 SPDI_STATUS				
31:10	Unused		-	
9	UNLOCK	R	0	UNLOCK active. This flag gets set to logic ‘1’ if the SPDIF Input receiver is NOT locked onto an incoming stream. Programmers can use this UNLOCK indication, in conjunction with the LOCK bit, to determine the state of the receiver or to make a decision to adjust the oversampling frequency. See the definition of the LOCK bit. Possible causes of an out-of-lock state are: i) The oversampling frequency is too high or too low with respect to the applied input SPDIF sample rate. ii) Too much jitter in SPDIF input stream. iii) Absent, invalid or corrupted SPDIF stream applied to the interface/receiver. The flag can be cleared by a software write to UNLOCK_CLR.
8	UCBITS	R	0	User/Channel bits available. This flag is set if a new set of user data bits and channel status bits have been written to the SPDI_UBITSx and SPDI_CBITSx registers. Updated on a block basis.

2.4.11 Measurement Functions

All measurements in the MBS are based on analyzing a video stream, within a programmable window, using specific algorithms. The measurement results are stored in registers once per field/frame. A special interrupt is generated to indicate that the measurement is done. Based on the measurement results, software sets the control parameters for the picture processing units.

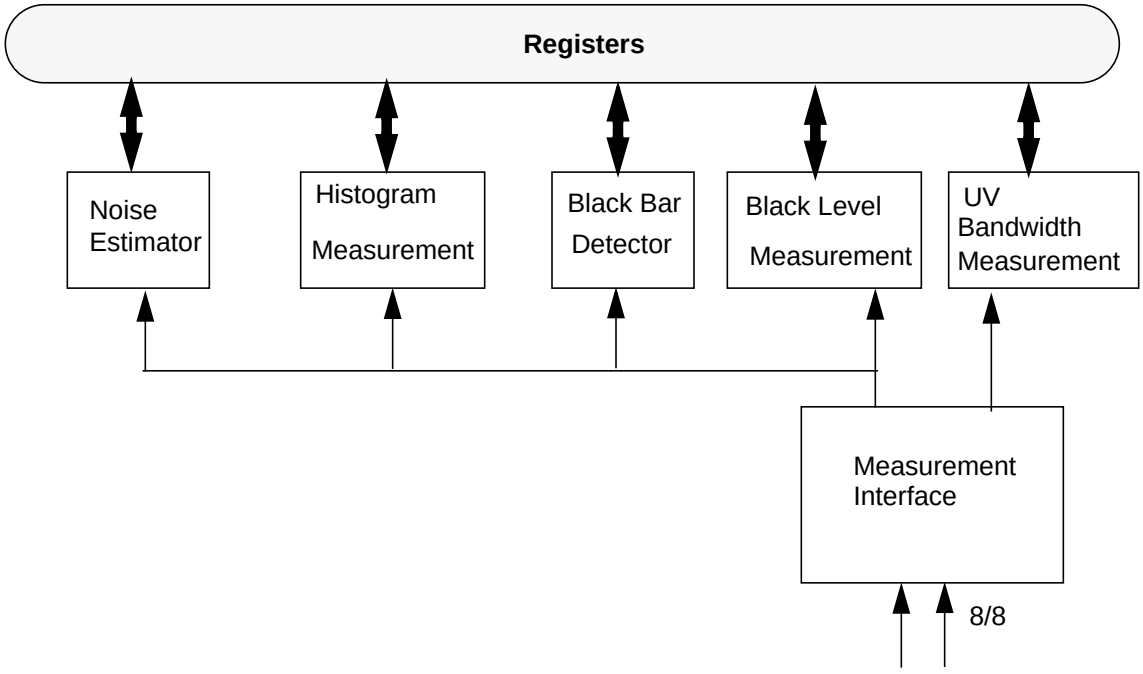


Figure 6: Measurement in the MBS

As shown in Figure 6, the MBS measurement block comprises:

- Measurement Block Interface

  Converts the inputs format (Y, U/V 8bits) into the format needed by the measurement units (Y, U/V 9bits).

- Histogram Measurement

  Analyses the Y component of the input data stream. Used for dynamic contrast improvement (i.e., histogram modification in QVCP).

- Noise Estimator

  Analyses the Y component. Controls the setting of LSHR pool ressource in QVCP.

- Black Bar Detector

  Analyses the Y component. Results are used to expand the picture to the display size in case of black bars at the top and/or bottom of the picture.

- Black Level Measurement

  Analyses the Y component. Used for black stretch.

Table 8: Memory Based Scaler (MBS) Registers *…Continued*

Bit	Symbol	Access	Value	Description
28:24	PFU_OFFS_C4 [4:0]	R/W	0	Offset component #4 (alpha or V) Index of MSB position within 32 bit word (0-31)
23:21	PFU_SIZE_C3 [2:0]	R/W	0	Size component #3 (V or B or Y2) number of bits minus 1 (e.g. 7 = 8 bits per component)
20:16	PFU_OFFS_C3 [4:0]	R/W	0	Offset component #3 (V or B or Y2) index of MSB position within 32 bit word (0-31)
15:13	PFU_SIZE_C2[2:0]	R/W	0	Size component #2 (U or G) number of bits minus 1 (e.g. 7 = 8 bits per component)
12:8	PFU_OFFS_C2[4:0]	R/W	0	Offset component #2 (U or G) index of MSB position within 32 bit word (0-31)
7:5	PFU_SIZE_C1[2:0]	R/W	0	Size component #1 (Y or R) number of bits minus 1 (e.g. 7 = 8 bits per component)
4:0	PFU_OFFS_C1[4:0]	R/W	0	Offset component #1 (Y or R) index of MSB position within 32 bit word (0-31)
Video Input Address Generation Control Registers				
Offset 0x10 C140	***Source Base Address #1***			
31:28	Unused		-	
27: 3	PFU_BASE1	R/W		Base address DMA #1 used depending on PFU_BAMODE setting
2:0	PFU_OFFSET1	R/W		Base address byte offset DMA #1 bits define pixel offset within multi pixel 64 bit words (e.g. a 16bit pixel can be placed on any 16 bit boundary)
Offset 0x10 C144	***Source Line Pitch #1***			
31:15	Unused		-	
14: 3	PFU_PITCH1	R/W	0	Line pitch DMA #1, signed value (two's complement) Used for all packed formats and for plane 1.
2:0	Unused		-	
Offset 0x10 C148	***Source Base Address #2***			
31:28	Unused		-	
27: 3	PFU_BASE2	R/W		Base address DMA #2 Used depending on PFU_BAMODE setting.
2:0	PFU_OFFSET2	R/W		Base address byte offset DMA #2 Bits define pixel offset within multi pixel 64-bit words (e.g., a 16-bit pixel can be placed on any 16-bit boundary).
Offset 0x10 C14C	***Source Line Pitch #2***			
31:15	Unused		-	
14: 3	PFU_PITCH2	R/W		Line pitch DMA #2, signed value (two's complement) Used for planes 2 and 3.
2:0	Unused		-	
Offset 0x10 C150	***Source Base Address #3***			
31:28	Unused		-	
27: 3	PFU_BASE3	R/W		Base address DMA #3 Used depending on PFU_BAMODE setting.

- A non-real-time queue sends packets immediately.

The two transmit queues can also be configured to support a generic Quality-of-Service (QoS) system: a high-priority queue provides high quality of service for packets; a low priority queue runs when possible.

A receive time-stamp indicates the exact moment in time a packet has been received.

Receive blocking filters are used to identify received packets that are not addressed to this Ethernet station, so that they can be discarded. The Rx filters include a perfect address filter, a hash filter, and four pattern-matching filters.

Wake-on-LAN power management support makes it possible to wake the system up from a power-down state (a state in which some of the clocks are switched off) when wake-up frames are received over the LAN. Wake-up frames are recognized by the receive filtering modules or by a Magic Frame detection technology. System wake-up occurs by triggering an interrupt.

An interrupt logic block raises and masks interrupts and keeps track of the cause of interrupts. The interrupt block sends interrupt request signals to the CPU. Interrupts can be enabled, cleared, and set by software.

Support for IEEE 802.3/clause 31 flow control is implemented in the Flow Control block. Receive flow-control frames are automatically handled by the LAN100. Transmit flow-control frames can be initiated by software. In half-duplex mode, the flow-control module will generate back pressure by sending out continuous preamble only interrupted by pauses to prevent the jabber limit.

The LAN100 has both a standard IEEE 802.3/clause 22 Media Independent Interface (MII) bus and a Reduced Media Independent Interface (RMII) to connect to an external Ethernet PHY chip [3]. MII or RMII mode can be selected by a bit in the LAN100 Command register. The standard nibble-wide MII interface allows a low-speed data connection to the PHY chip at speeds of 2.5 MHz at 10 Mbit/s or 25 MHz at 100 Mbit/s. The RMII interface allows connection to the PHY with low pin-count and double-speed data clock. Registers in the PHY chip are accessed via the MMIO interface through the serial management connection of the MII bus operating at 2.5 MHz.

3. Register Descriptions

3.1 Register Summary

The base address for LAN100 MMIO registers begins at offset 0x07,2000 with respect to MMIO_BASE.

After a hard or soft reset via the RegReset bit of the Command register, all bits in all registers are reset to 0, unless shown otherwise in Table 2.

Reading write-only registers will return a read error. Writing read-only registers will return a write error. Unused or resrved bits must be ignored on reads and written as 0.

Chapter 24: TM3260 Debug

PNX15xx Series Data Book – Volume 1 of 1

Rev. 3 — 17 March 2006 Product data sheet

1. Introduction

The TM3260 Debug (TM_DBG) interface consists of the Test Access Port (TAP), the TAP Controller, a JTAG Instruction register and internal debug registers. The TAP controller from which the TM_DBG module receives its commands resides in the test control block, which also facilitates boundary scanning and other DFT features.

1.1 Features

The TM_DBG has registers that can be programmed for control and communication with an on-chip TriMedia TM3260 CPU.

2. Functional Description

2.1 General Operations

2.1.1 Test Access Port (TAP)

The Test Access Port (TAP) includes four dedicated input pins and one output pin:

- TCK (Test Clock)
- TMS (Test Mode Select)
- TDI (Test Data In)
- TDO (Test Data Out)

TCK provides the clock for test logic required by the JTAG standard. TCK is asynchronous to any system clock. Stored state devices in the JTAG controller will retain their state indefinitely when TCK is stopped at 0 or 1.

The signal received at TMS is decoded by the TAP controller to control test functions. The test logic is required to sample TMS at the rising edge of TCK.

Serial test instructions and test data are received at TDI. The TDI signal is required to be sampled at the rising edge of TCK. When test data is shifted from TDI to TDO, the data must appear without inversion at TDO after a number of rising and falling edges of TCK determined by the length of the instruction or test data register selected.

Assuming the arbiter has been configured to include the priority list and both round-robin lists, any arbiter decision is made through the following four steps:

1. First the DMA requests are compared against the current entry in the TDMA timing wheel. If the agent in the current entry is requesting this agent will be granted.
2. If the agent in the current entry is not requesting the DMA requests will be compared against the agents in the priority list and if one or more of the agents in the priority list is requesting the one that has the highest priority will be granted.
3. If none of the DMA requests matches the current entry in the TDMA timing wheel or one or more entries in the priority list, the arbiter will grant the DMA agent that has not been served for the longest time by choosing from the round robin #1 list. Every time the arbiter provides a grant to any DMA agent, the round robin #1 arbiter checks if this agent is in it's list and makes that agent the lowest priority entry in the round robin #1 list. If a certain agent is granted because of its entry in the TDMA timing wheel or priority list and the same agent has also an entry in the round-robin #1 list, then in the next clock cycle this agent will have the lowest priority in the round-robin #1 list. Also, in case there are multiple entries of the same agent in the round-robin #1 list, the highest entry in the list gets the lowest priority during the next cycle. The other entries of the same agents do not get the lowest priority.
4. If none of the DMA requests matches: the current entry in the TDMA timing wheel, or one or more entries in the priority list or one or more entries in the first round-robin list, the arbiter will grant the DMA agent that has not been served for the longest time from the round robin #2 list of entries. The round-robin #2 list operates the same way as the round-robin #1 list but all entries in this list have a lower priority than the entries in the round-robin #1 list.

The TDMA wheel will proceed to the next entry if and only if one of the two following situations apply:

- when there is a grant at the level of the TDMA wheel
- when there is no match in the complete list (TDMA, priority and both round-robin lists)

All entries in the TDMA wheel, priority list and both round-robin lists are fully programmable via the DTL MMIO interface of the arbiter. The same is true for the number of entries in any of these four. It is also possible to set the number of entries in the TDMA wheel, priority list and/or round-robin lists to zero. This allows the user to use only one of the four mechanisms or any combination of them. In case all four are set to zero for the active set of entries, the arbiter defaults to a round-robin arbitration over all agents.

The arbitration algorithm only starts after the arbiter has been properly initialized via the programming registers. Following the de-assertion of a hard reset, the arbiter uses a simple counting algorithm to arbitrate between all request inputs. In this boot mode agents are granted in the order that they are internally wired.

The MBS supports all planar formats on input and output. The VIP can produce the planar and semi-planar YUV 4:2:2 planar formats. The semi-planar YUV 4:2:0 format is the only format produced by the MPEG video decoder hardware.

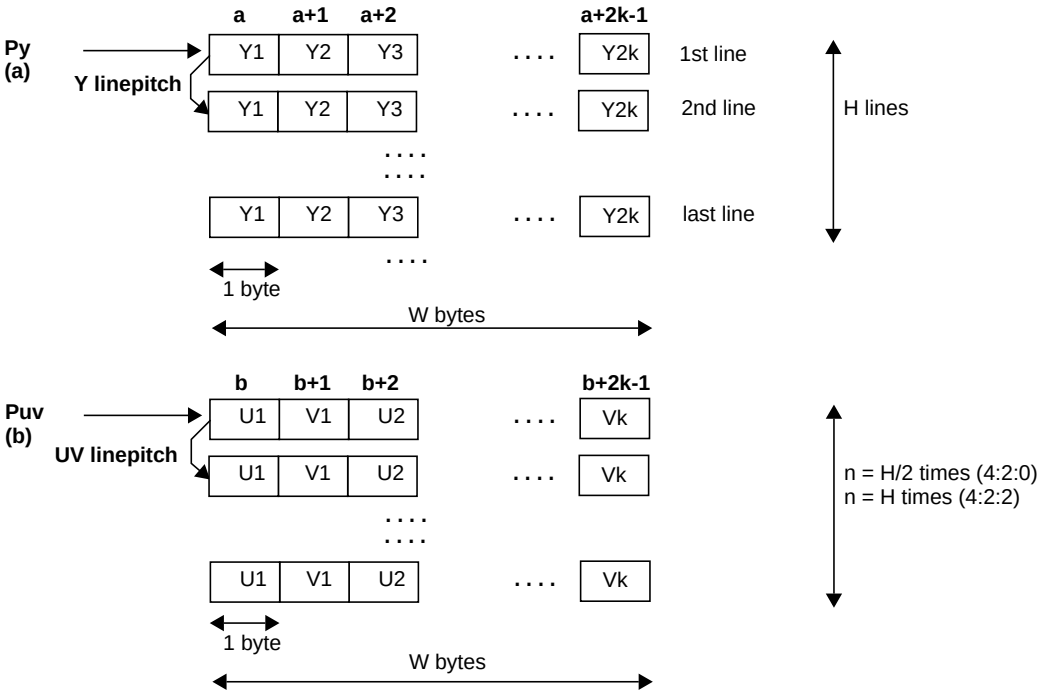


Figure 10: Semi-Planar YUV 4:2:0 and YUV 4:2:2 Formats