Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IrDA, LINbus, SCI, SSU, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f20103nfa-u0

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions may occur due to the false recognition of the pin state as an input signal. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

4.6.5 Changing PMR, ISCRH, ISCRL and INCCR

When the PMR, ISCRH, ISCRL, and INCCR are modified to change an IRQ7 to IRQ0 interrupt function, the interrupt request flag bit may be set to 1 at an unintended time. To prevent this, the pin function should be changed when the interrupt request is disabled, then the interrupt request flag should be cleared to 0 after a specific interval time*.

Figure 4.7 shows the procedure to modify PMR (port mode register), ISCRH, ISCRL, and INCCR and clear the interrupt request flags.

Note: Two states + a minimum interval for input (t_{IH}/t_{IL})

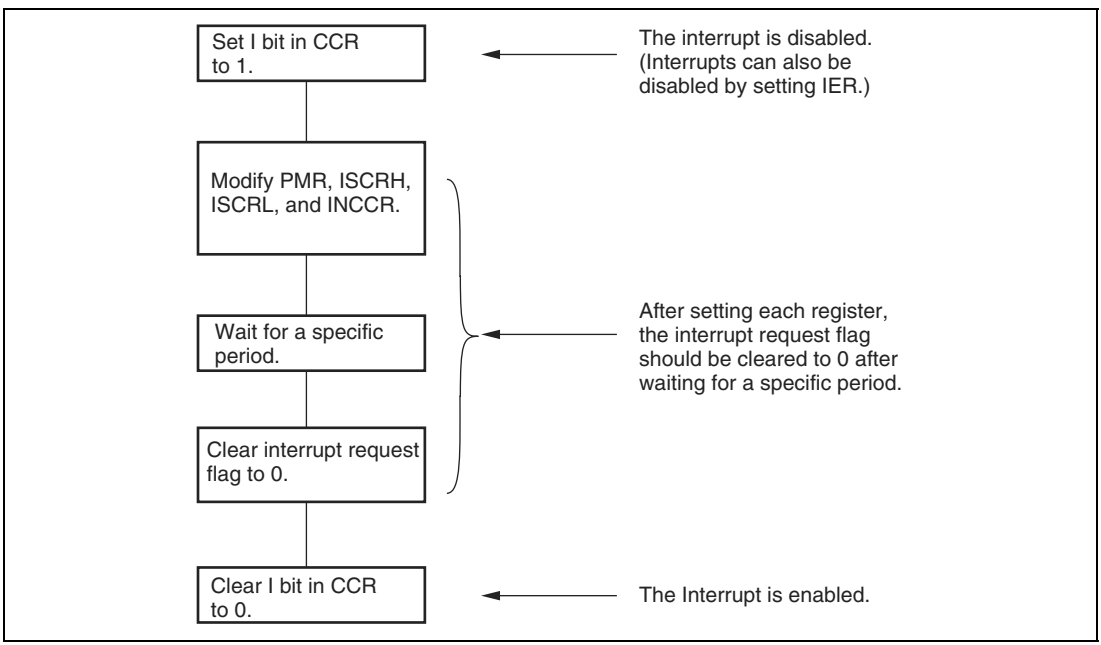


Figure 4.7 Procedure to Modify PMR, ISCRH, ISCRL, and INCCR and Clear Interrupt Request Flag

4.6.6 IRQ Status Register (ISR)

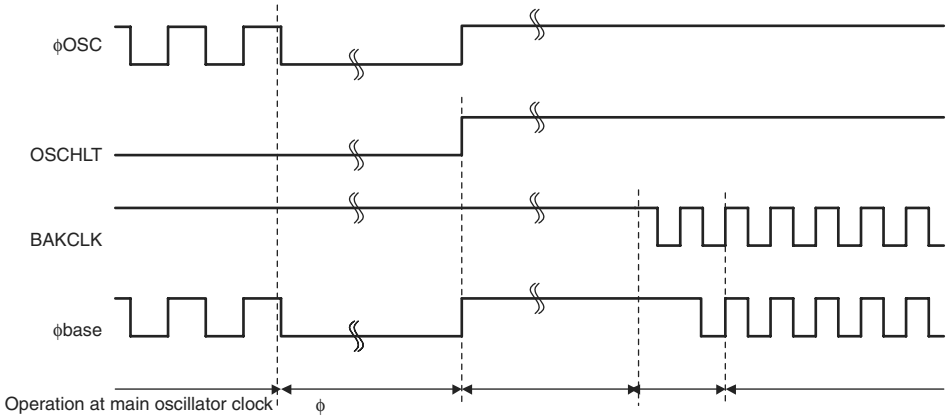
Depending on the pin state after a reset, IRQnF may be set to 1. Therefore, always read ISR and clear it to 0 after resets.

5.2.1 Backup Control Register (BAKCR)

Address: H'FF06D4

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	WI	WE	OSCBAKE	BAKCKSEL	CKSWIE	CKSWIF	OSCHLT	
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7	WI	Write inhibit	0: Writing is permitted. 1: Writing is inhibited.	W
6	WE	Write enable	0: Writing is disabled. 1: Writing is enabled. [Setting condition] When 0 is written to WI and 1 is written to WE at the same time. [Clearing condition] When 0 is written to WI and WE at the same time.	R/W
5	OSCBAKE	External clock backup enable	0: External clock backup is disabled. 1: External clock backup is enabled.*	R/W
4	BAKCKSEL	Backup destination clock source select	0: low 1: Setting prohibited	R/W
3	CKSWIE	Clock switching interrupt enable	0: Interrupt requests are disabled. 1: Interrupt requests are enabled.	R/W
2	CKSWIF	Clock switching interrupt flag	0: A clock switching interrupt request has not been generated. 1: A clock switching interrupt request has been generated. [Setting condition] When the system clock for the LSI is switched from osc to low while OSCBAKE is 1. [Clearing condition] When 1 is read from the bit and then 0 is written to the same bit.	R/W


ϕOSC
OSCHLT
BAKCLK
ϕbase
Operation at main oscillator clock
ϕ

10.10.3 Port Data Register J (PDRJ)

Address: H'FFFFEC

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
							PDRJ1	PDRJ0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7 to 2	—	Reserved	These bits are read as 0. The write value should be 0.	—
1	PDRJ1	Port J1 data	0: Low level	R/W
0	PDRJ0	Port J0 data	1: High level	R/W
			PDRJ is a register that stores output data for port J pins. When PCRJ bits are set to 1, the values stored in PDRJ are output. When PDRJ is read while PCRJ bits are set to 1, the values stored in PDRJ are read. If PDRJ is read while PCRJ bits are cleared to 0, the pin states are read regardless of the value stored in PDRJ.	

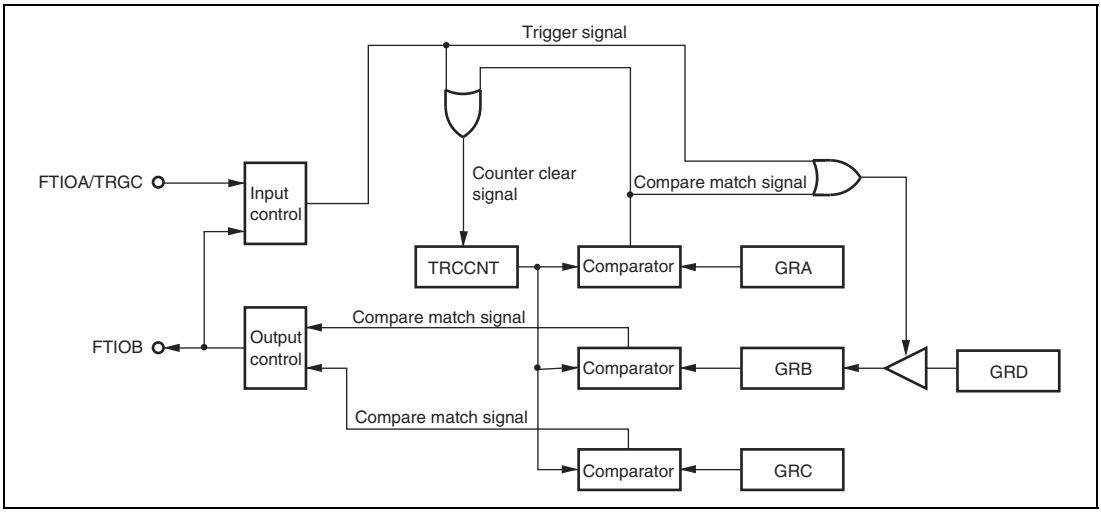


Figure 15.14 Block Diagram in PWM2 Mode

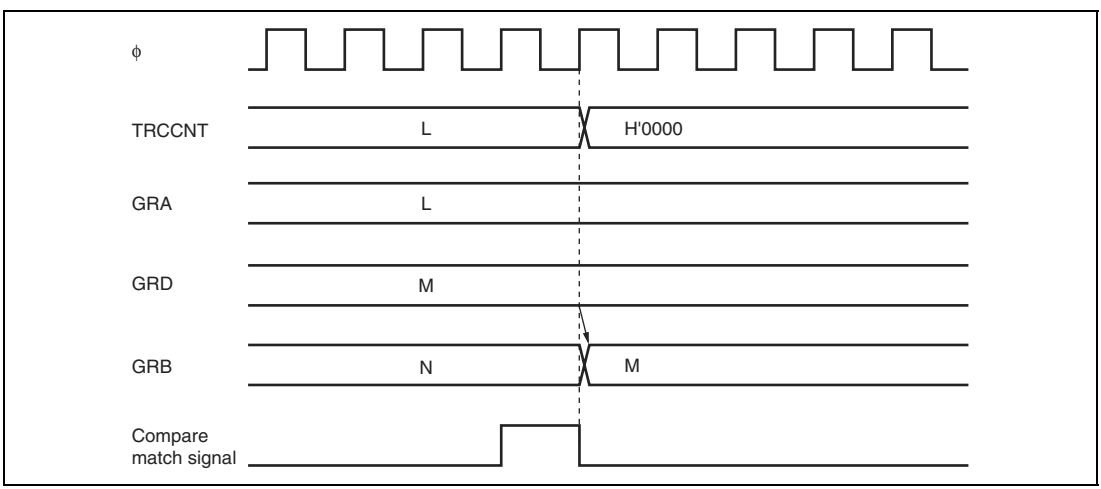


Figure 15.15 GRD and GRB Buffer Operating Timing in PWM2 Mode (1)

- High-speed access by the internal 16-bit bus

  16-bit TRDCNT and GR registers can be accessed in high speed by a 16-bit bus interface
- Any initial timer output value can be set
- Output of the timer is disabled by external trigger
- Eleven interrupt sources

  Four compare match/input capture interrupts and an overflow interrupt are available for each channel. An underflow interrupt can be set for channel 1.

Bit	Symbol	Bit Name	Description	R/W
2	TOC0	Output level select C0	0: 0 output at the FTIOC0 pin* 1: 1 output at the FTIOC0 pin*	R/W
1	TOB0	Output level select B0	• In modes other than PWM3 mode 0: 0 output at the FTIOB0 pin* 1: 1 output at the FTIOB0 pin* • In PWM3 mode 0: 1 output at the FTIOB0 pin on GRB_1 compare match and 0 output at the FTIOB0 pin on GRB_0 compare match 1: 0 output at the FTIOB0 pin on GRB_1 compare match and 1 output at the FTIOB0 pin on GRB_0 compare match	R/W
0	TOA0	Output level select A0	• In modes other than PWM3 mode 0: 0 output at the FTIOA0 pin* 1: 1 output at the FTIOA0 pin* • In PWM3 mode 0: 1 output at the FTIOB0 pin on GRA_1 compare match and 0 output at the FTIOB0 pin on GRA_0 compare match 1: 0 output at the FTIOB0 pin on GRA_1 compare match and 1 output at the FTIOB0 pin on GRA_0 compare match	R/W

Note: * The change of the setting is immediately reflected in the output value.

TRDOCR selects the initial outputs before the first occurrence of a compare match. Note that bits OLS1 and OLS0 in TRDFCR set these initial outputs in reset synchronous PWM mode and complementary PWM mode.

In PWM3 mode, TRDOCR selects the output level of the FTIOA0 and FTIOB0 pins.

(1) Example of Input Capture Operation

Figure 16.17 shows an example of input capture operation.

In this example, both rising and falling edges have been selected as the FTIOA pin input capture input edge, the falling edge has been selected as the FTIOB pin input capture input edge, and counter clearing by GRB input capture has been designated for TRDCNT.

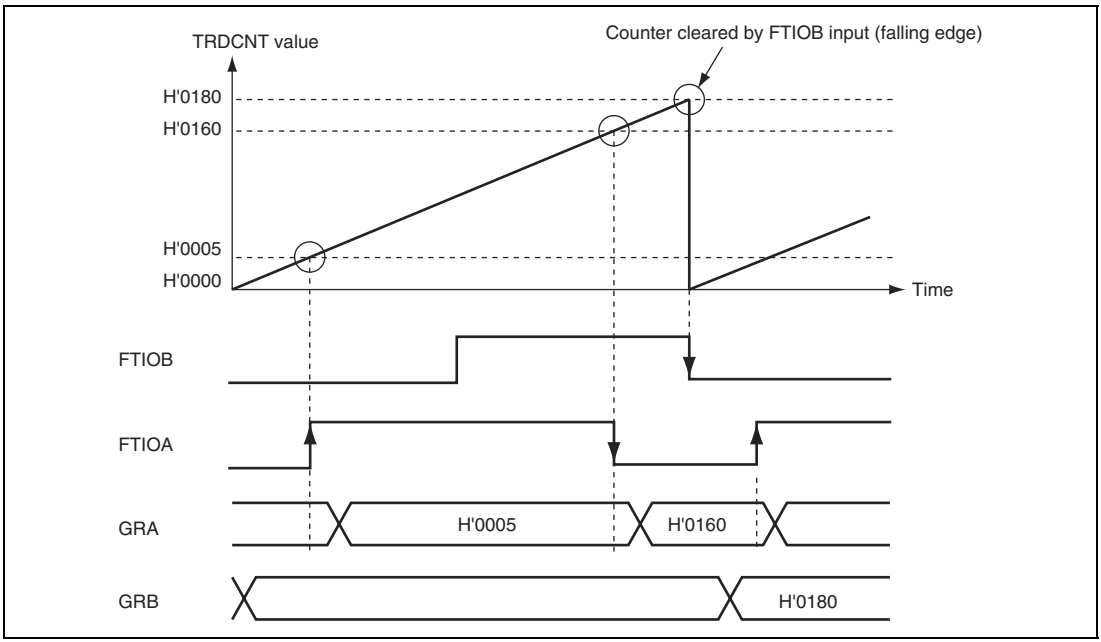


Figure 16.17 Example of Input Capture Operation

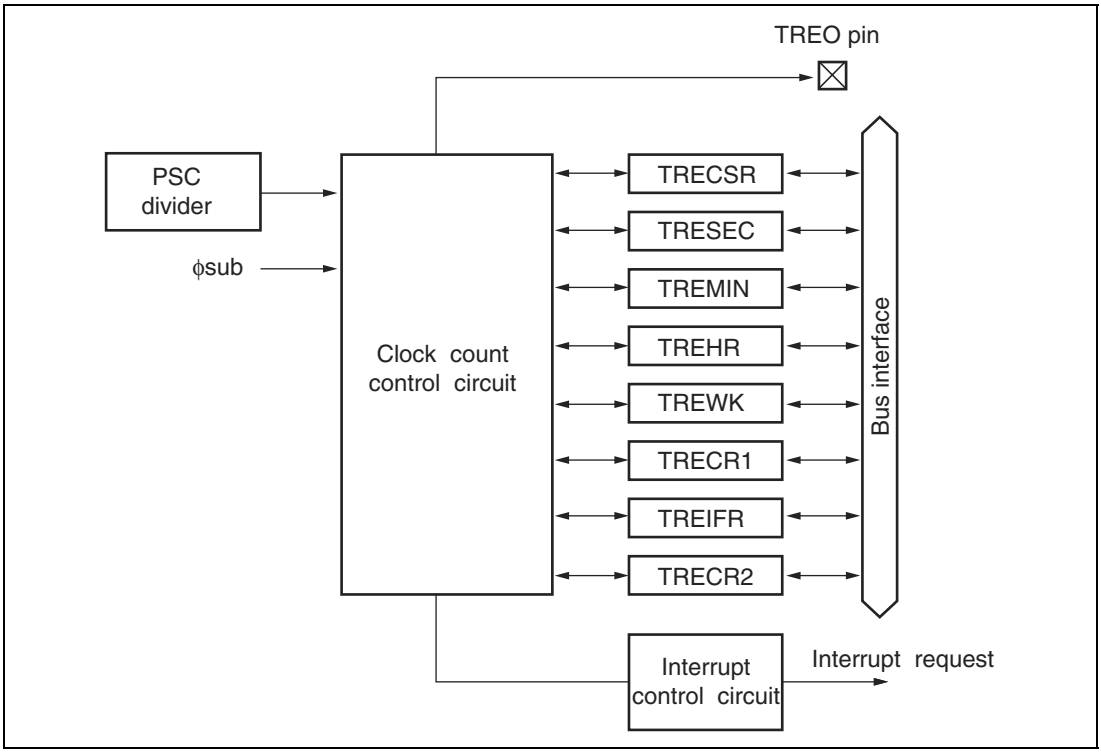


Figure 17.1 Block Diagram of Timer RE

Table 17.1 shows the timer RE input/output pin.

Table 17.1 Pin Configuration

Pin Name	I/O	Function
TREO	Output	Clock or compare-match output

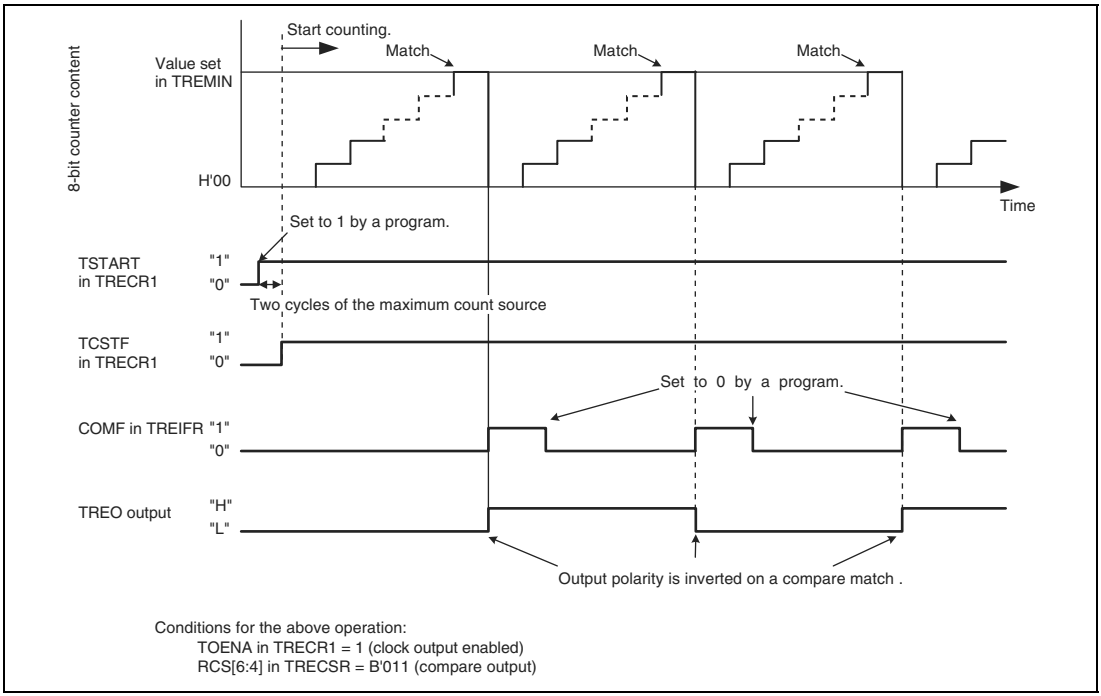


Figure 17.7 Example of Output Compare Mode Operation

18.2.8 General Registers A and B (GRA, GRB), GRA and GRB Buffer Registers (BRA, BRB)

GRA

Address: H'FF0642

Bit:	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GRB

Address: H'FF0644

Bit:	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

BRA

Address: H'FF064C

Bit:	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

BRB

Address: H'FF064E

Bit:	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Each of GRA and GRB is a 16-bit readable/writable register that can function as either an output-compare register or an input-capture register. The function is selected with TRGIOR.

When a general register is used as an output-compare register, its value is constantly compared with the TRGCNT value. When the two values match (a compare match), the corresponding flag (the IMFA or IMFB bit) in TRGSR is set to 1. A compare match output can be selected in TRGIOR.

When a general register is used as an input-capture register, an external input-capture signal is detected and the current TRGCNT value is stored in the general register. The corresponding flag (the IMFA or IMFB bit) in TRGSR is set to 1. The edge of the input-capture signal is selected in TRGIOR. The setting of TRGIOR is ignored in PWM mode.

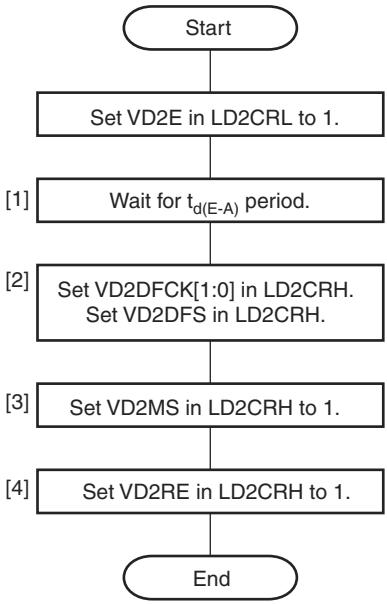
26.2.5 Low-Voltage Detection Circuit 1 Control Register L (LD1CRL)

Address: H'FF0625

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	VD1E	—	—	—	VD1LS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7	VD1E	LVD1 circuit enable	0: The LVD1 circuit is not used. (In standby mode) 1: The LVD1 circuit is used.	R/W
6 to 4	—	Reserved	These bits are read as 0. The write value should be 0.	—
3 to 0	VD1LS [3:0]	LVD1 detection voltage level select 3 to 0	0000: Setting prohibited 0001: Setting prohibited 0010: Setting prohibited 0011: Setting prohibited 0100: Setting prohibited 0101: Setting prohibited 0110: Setting prohibited 0111: 3.07 V (typ.) 1000: 3.22 V (typ.) 1001: 3.37 V (typ.) 1010: 3.52 V (typ.) 1011: 3.67 V (typ.) 1100: 3.82 V (typ.) 1101: 3.97 V (typ.) 1110: 4.12 V (typ.) 1111: 4.27 V (typ.)	R/W

Note: This register is not initialized by an LVD2 reset and LVD1 reset.



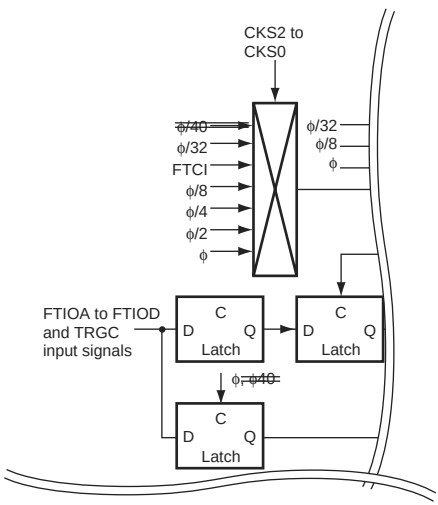
[1] Set VD2E in LD2CRL to activate the LVD2 circuit and wait for the stabilization.

[2] Set the digital filter.

[3] Set the LVD2 circuit to generate reset requests.

[4] Enable the LVD2 circuit reset requests.

Figure 26.7 Procedure to Set LVDR2

Item	Page	Revision (See Manual for Details)
Section 15 Timer RC 15.2 Register Descriptions 15.2.12 General Registers A, B, C, and D (GRA, GRB, GRC, and GRD)	462	Amended … If the corresponding interrupt-enable bit (the IMIEA, IMIEB, IMIEC, or IMIED bit) in TRCIER is set to 1 at this time, an interrupt request is generated. …
15.3 Operation 15.3.4 Digital Filtering Function for Input Capture Inputs	481	Amended Input signals on the FTIOA to FTIOD and TRGC pin can be input via the digital filters. The digital filter includes three latches connected in series and a match detector circuit.
Figure 15.22 Block Diagram of Digital Filter	481	Deleted 
15.3.7 Operation through an Event Link (2) Counting Event	486	Added … When the event specified in ELSR2 occurs, event counter operation proceeds with that event as the source to drive counting, regardless of the setting of the CKS[2:0] bits in TRCCR1 and the CTS bit in TRCMR. …