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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IrDA, LINbus, SCI, SSU, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f20103nfb-u0

1.4 Pin Assignments

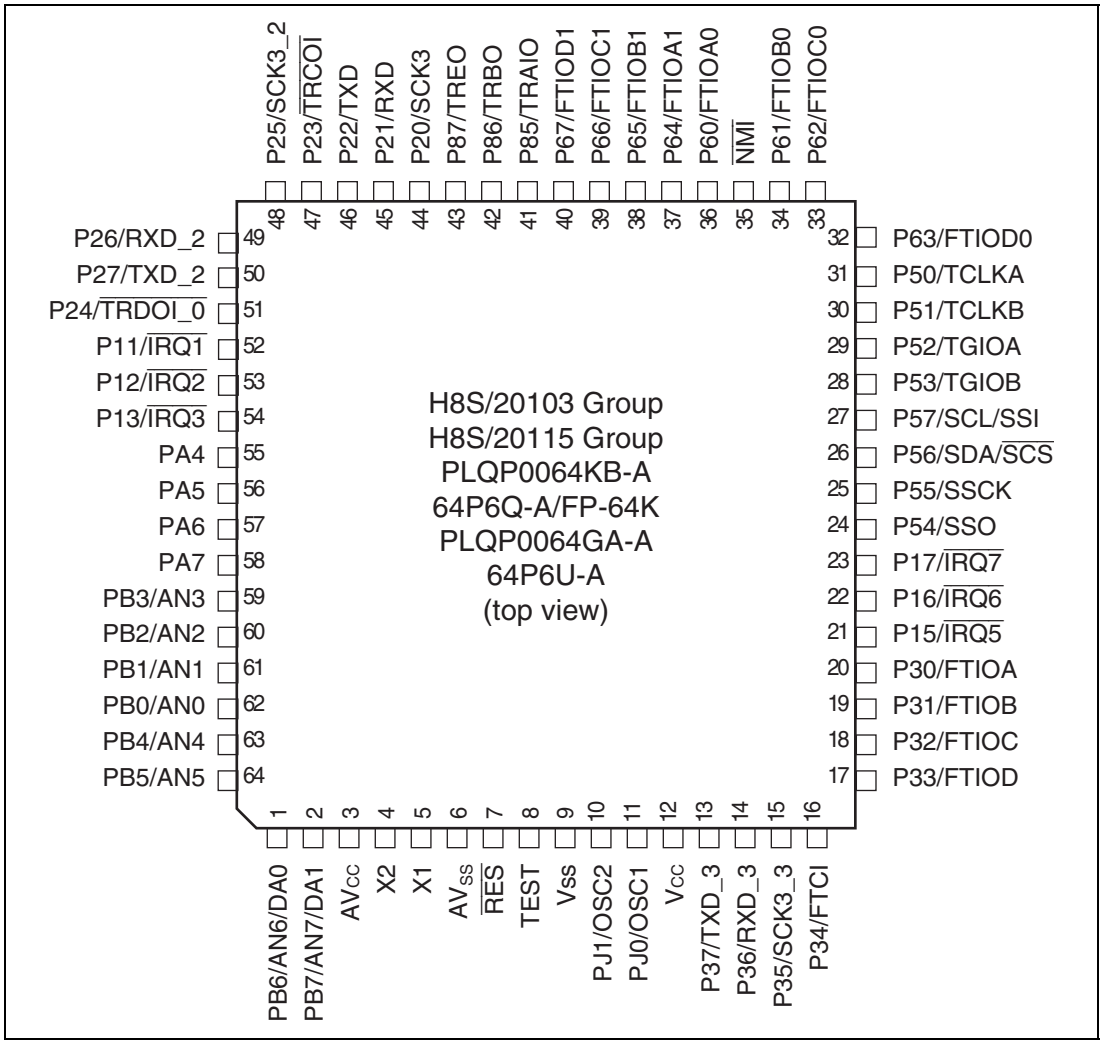


Figure 1.5 Pin Assignment of the H8S/20103 and H8S/20115 Groups

Table 2.7 Bit Manipulation Instructions (2)

Instruction	Size*	Function
BXOR	B	C ⊕ (<bit-No.> of <EAd>) → C Logically exclusive-ORs the carry flag with a specified bit in a general register or memory operand and stores the result in the carry flag.
BIXOR	B	C ⊕ ~ (<bit-No.> of <EAd>) → C Logically exclusive-ORs the carry flag with the inverse of a specified bit in a general register or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
BLD	B	(<bit-No.> of <EAd>) → C Transfers a specified bit in a general register or memory operand to the carry flag.
BILD	B	~ (<bit-No.> of <EAd>) → C Transfers the inverse of a specified bit in a general register or memory operand to the carry flag. The bit number is specified by 3-bit immediate data.
BST	B	C → (<bit-No.> of <EAd>) Transfers the carry flag value to a specified bit in a general register or memory operand.
BIST	B	~ C → (<bit-No.>. of <EAd>) Transfers the inverse of the carry flag value to a specified bit in a general register or memory operand. The bit number is specified by 3-bit immediate data.

Note: * Size refers to the operand size.
B: Byte

- STBYRS bit (ϕ source select for recovery from standby mode)
  Selects a clock source to be used when a transition is made from standby mode to active mode.

- PHIBSEL bit (ϕbase clock source select)
  Selects a clock source for the ϕbase to be used in active mode or sleep mode.

5.2.4 Power-Down Control Register 2 (LPCR2)

Address: H'FF06D2

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	WI	WE	—	—	—	PHI[2:0]		
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7	WI	Write inhibit	0: Writing is permitted. 1: Writing is inhibited.	W
6	WE	Write enable	0: Writing is disabled. 1: Writing is enabled. [Setting condition] When 0 is written to WI and 1 is written to WE at the same time. [Clearing condition] When 0 is written to WI and WE at the same time.	R/W
5 to 3	—	Reserved	These bits are read as 0. The write value should be 0.	—
2 to 0	PHI[2:0]	System clock ϕ select	000: ϕbase 001: ϕbase/2 010: ϕbase/4 011: ϕbase/8 100: ϕbase/16 101: ϕbase/32 110: ϕbase/64 111: ϕbase/128	R/W

Note: A MOV instruction should be used to write to this register.

On receiving the command with H'FF as the block number, the boot program terminates erasure processing and waits for the next programming/erasure selection command.

Command	H'58	Size	Block number	SUM

- Command H'58 (1 byte): Block erasure
- Size (1 byte): The number of characters in the block number field (fixed to 1)
- Block number (1 byte): H'FF (erasure terminating code)
- SUM (1 byte): Checksum

Response	H'06

- Response H'06 (1 byte): Response to the block erasure command for terminating erasure processing; ACK code is returned upon termination of the erasure process.

To perform erasure again after issuing the command with H'FF as the block number, start the process by sending an erasure selection command.

(e) Memory Read

In response to a memory read command, the boot program returns the data stored in the specified address.

Command	H'52	Size	Area	Address for reading	
	Reading size				SUM

- Command H'52 (1 byte): Memory read
- Size (1 byte): The total size of the area, address-for-reading, and reading-size fields (fixed to 9)
- Area (1 byte):
  H'01: User ROM area
  Specifying an incorrect area causes an address error.
- Address for reading (4 bytes): Address where reading starts
- Reading size (4 bytes): The amount of data to be read
- SUM (1 byte): Checksum

(3) Programming

A programming command is used to program data in the flash memory in 4-byte units.

Command or data size can be set depending on the FMWUS bit in FLMCR1. Setting the FMWUS bit to 0 enables using byte instructions. When H'41 is written in the first command cycle and data is written to the programming address in the second through fifth command cycles, programming and verifying are automatically started*.

Setting the FMWUS bit to 1 enables using word instructions. When H'4141 is written in the first command cycle and data is written to the programming address in the second and third command cycles, programming and verifying are started*.

Completion of programming is indicated by the FMRDY bit in FLMSTR. The FMRDY bit is read as 0 during programming, and read as 1 after programming completion.

After programming completion, the programming result can be checked by reading the FMPRSF bit in FLMSTR. (See the description in (9) below, Full Status Checking.)

Figure 7.16 shows the programming flowchart.

Do not additionally program the already-programmed addresses.

Note that if the lock bit is 0 (locked) in the specified block and the FMLBD bit is 0 (lock bit enabled), a programming command is not accepted for the specified block.

In EW1 mode, do not execute this command for the block in which the reprogramming-control program is located.

The FMRDY bit in FLMSTR changes to 0 when programming is started, and changes to 1 when completed.

Note: * The lower two bits of the programming addresses are ignored.

10.3 Port 3

Figure 10.3 shows the pin configuration of port 3.

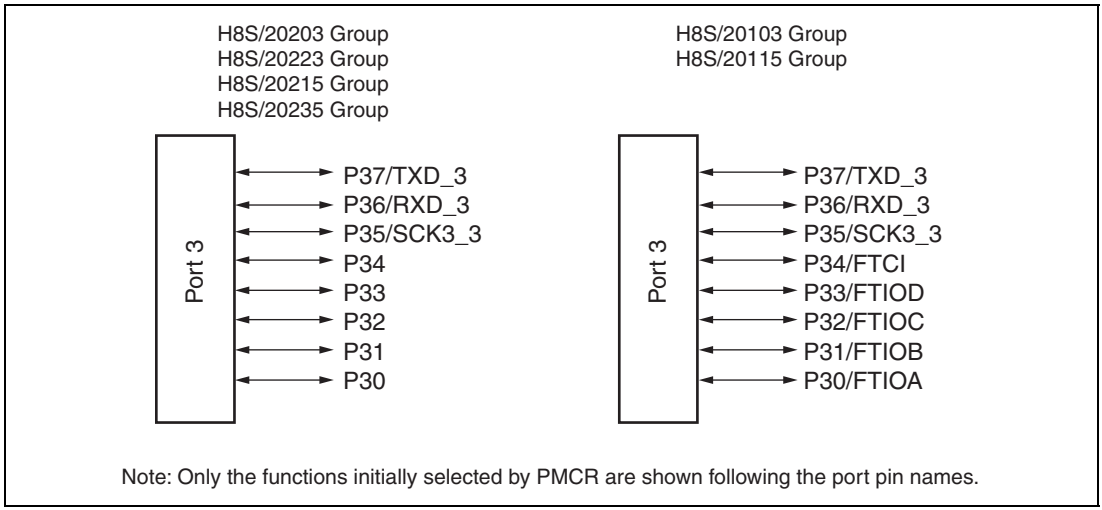


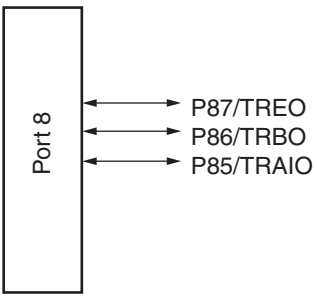
Figure 10.3 Port 3 Pin Configuration

Port 3 has the following registers.

- Port mode register 3 (PMR3)
- Port control register 3 (PCR3)
- Port data register 3 (PDR3)
- Port pull-up control register 3 (PUCR3)
- Port drive control register 3 (PDVR3)

10.6 Port 8

Figure 10.6 shows the pin configuration of port 8.



Note: Only the functions initially selected by PMCR are shown following the port pin names.

Figure 10.6 Port 8 Pin Configuration

Port 8 has the following registers.

- Port mode register 8 (PMR8)
- Port control register 8 (PCR8)
- Port data register 8 (PDR8)
- Port pull-up control register 8 (PUCR8)
- Port drive control register 8 (PDVR8)

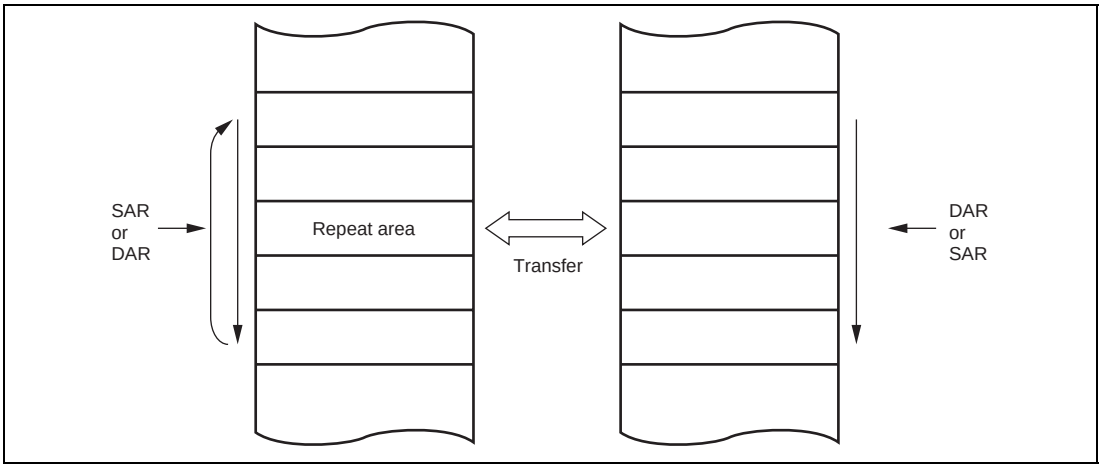


Figure 11.7 Memory Mapping in Repeat Mode

11.5.3 Block Transfer Mode

In block transfer mode, one operation transfers one block of data. Either the transfer source or the transfer destination is designated as a block area. Table 11.7 lists the register function in block transfer mode. The block size is 1 to 256. When the transfer of one block ends, the initial state of the block size counter and the address register specified as the block area is restored. The other address register is then incremented, decremented, or left fixed according to the register information. From 1 to 65,536 transfers can be specified. Once the specified number of transfers has ended, a CPU interrupt is requested.

Table 11.7 Register Function in Block Transfer Mode

Name	Abbreviation	Function
DTC source address register	SAR	Designates source address
DTC destination address register	DAR	Designates destination address
DTC transfer count register AH	CRAH	Holds block size
DTC transfer count register AL	CRAL	Designates block size count
DTC transfer count register B	CRB	Designates transfer count

12.2.12 Event-Generation Timer Interval Setting Register B (ELTMSB)

Address: H'FF06BA

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	C3CLS[3:0]				C2CLS[3:0]			
Value after reset:	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7 to 4	C3CLS[3:0]*	Channel 3 event-generation interval select	0000: Clock source φELC/1	R/W
			0001: Clock source φELC/2	
			0010: Clock source φELC/4	
			0011: Clock source φELC/8	
			0100: Clock source φELC/16	
			0101: Clock source φELC/32	
			0110: Clock source φELC/64	
			0111: Clock source φELC/128	
			1000: Clock source φELC/256 (initial value)	
			1001: Clock source φELC/512	
			1010: Clock source φELC/1024	
			1011: Clock source φELC/2048	
			1100: Clock source φELC/4096	
			1101: Clock source φELC/8192	
			1110: Clock source φELC/16384	
			1111: Clock source φELC/32768	

- High-speed access by the internal 16-bit bus
  16-bit TRDCNT and GR registers can be accessed in high speed by a 16-bit bus interface
- Any initial timer output value can be set
- Output of the timer is disabled by external trigger
- Eleven interrupt sources
  Four compare match/input capture interrupts and an overflow interrupt are available for each channel. An underflow interrupt can be set for channel 1.

16.2.17 Interface with CPU

(1) 16-Bit Register

TRDCNT and GR are 16-bit registers. Reading/writing in a 16-bit unit is enabled but disabled in an 8-bit unit since the data bus with the CPU is 16-bit width. These registers must always be accessed in a 16-bit unit. Figure 16.5 shows an example of accessing the 16-bit registers.

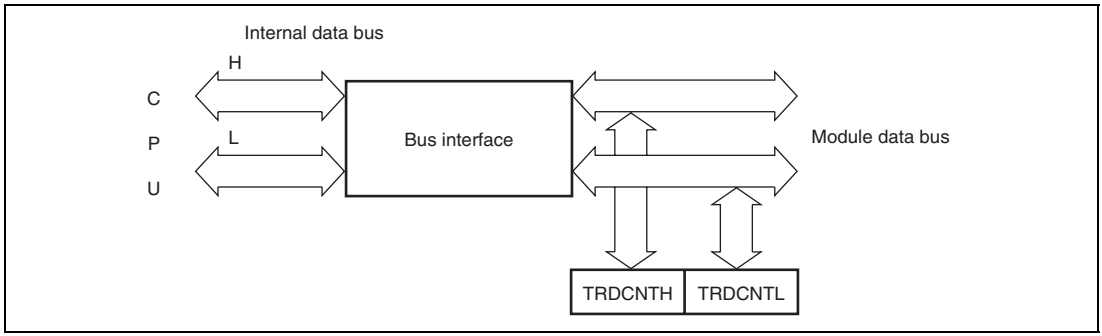


Figure 16.5 Accessing Operation of 16-Bit Register (between CPU and TRDCNT (16 bits))

(2) 8-Bit Register

Registers other than TRDCNT and GR are 8-bit registers that are connected internally with the CPU in an 8-bit width. Figure 16.6 shows an example of accessing the 8-bit registers.

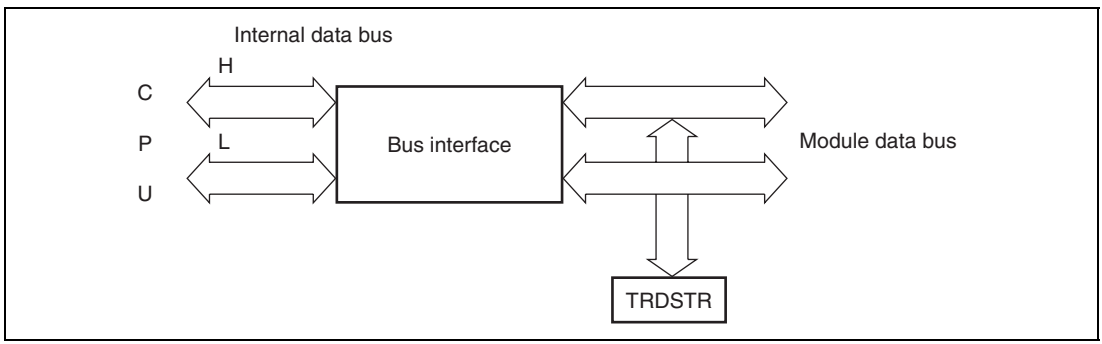


Figure 16.6 Accessing Operation of 8-Bit Register (between CPU and TRDSTR (8 bits))

(c) Output compare output timing

A compare match signal is generated in the final state in which TRGCNT and GR match (the point at which the count value matched by TRGCNT is updated). When a compare match signal is generated, the output value set in TRGIOR is output at the output compare output pin (TGIOA, TGIOB). After a match between TRGCNT and GR, the compare match signal is not generated until the TRGCNT input clock is generated.

Figure 18.5 shows output compare output timing.

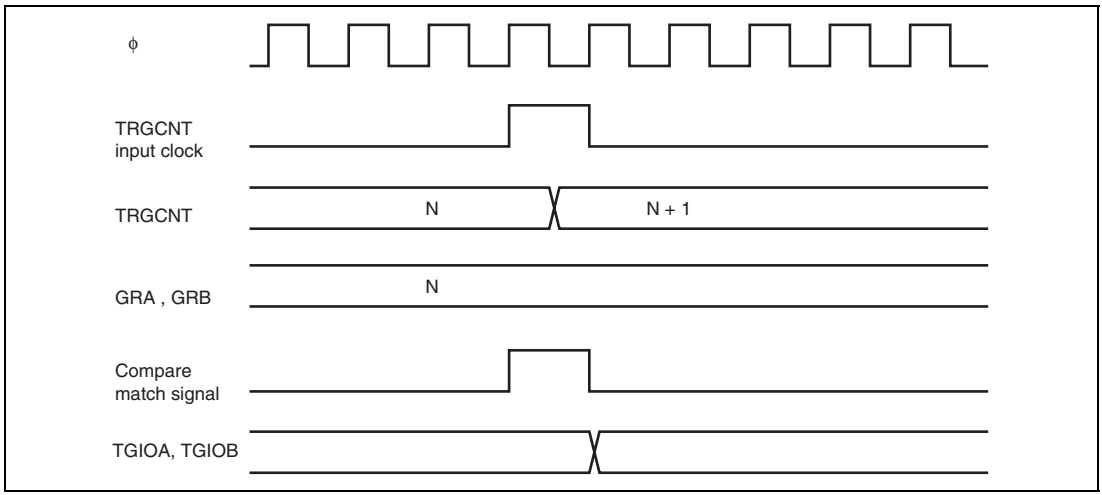


Figure 18.5 Output Compare Output Timing

19.2 Register Descriptions

The watchdog timer has the following registers.

- Timer control/status register WD (TCSRWD)
- Timer counter WD (TCWD)
- Timer mode register WD (TMWD)
- Timer interrupt control register WD (TICRWD)
- Timer interrupt flag register WD (TIFRWD)

19.2.1 Timer Control/Status Register WD (TCSRWD)

Address: H'FFFF9A

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	B6WI	TCWE	B4WI	TCSRWE	TMWLOCK	TMWI	—	—
Value after reset:	1	0	1	0	0	1	1	1

Bit	Symbol	Bit Name	Description	R/W
7	B6WI	Bit 6 write inhibit	0: Writing to the TCWE bit (bit 6 in this register) is enabled. 1: Writing to the TCWE bit (bit 6 in this register) is disabled. This bit is always read as 1.	R/W
6	TCWE	Timer counter WD write enable	0: Writing to the TCWD register is disabled. 1: Writing to the TCWD register is enabled. Before writing data to this bit, the B6WI bit must be cleared to 0.	R/W
5	B4WI	Bit 4 write inhibit	0: Writing to the TCSRWE bit (bit 4) is enabled. 1: Writing to the TCSRWE bit (bit 4) is disabled. This bit is always read as 1.	R/W
4	TCSRWE	Timer control/status register WD write enable	0: Writing to TMWLOCK and TMWI (bits 3 and 2 in this register) is disabled. 1: 0: Writing to TMWLOCK and TMWI (bits 3 and 2 in this register) is enabled. Before writing data to this bit, the B4WI bit must be cleared to 0.	R/W

21.3 Operation

The I²C bus interface 2 can communicate either in I²C bus mode or clock synchronous serial mode by setting FS in SAR.

21.3.1 I²C Bus Format

Figure 21.3 shows the I²C bus formats. Figure 21.4 shows the I²C bus timing. The first frame following a start condition always consists of 8 bits.

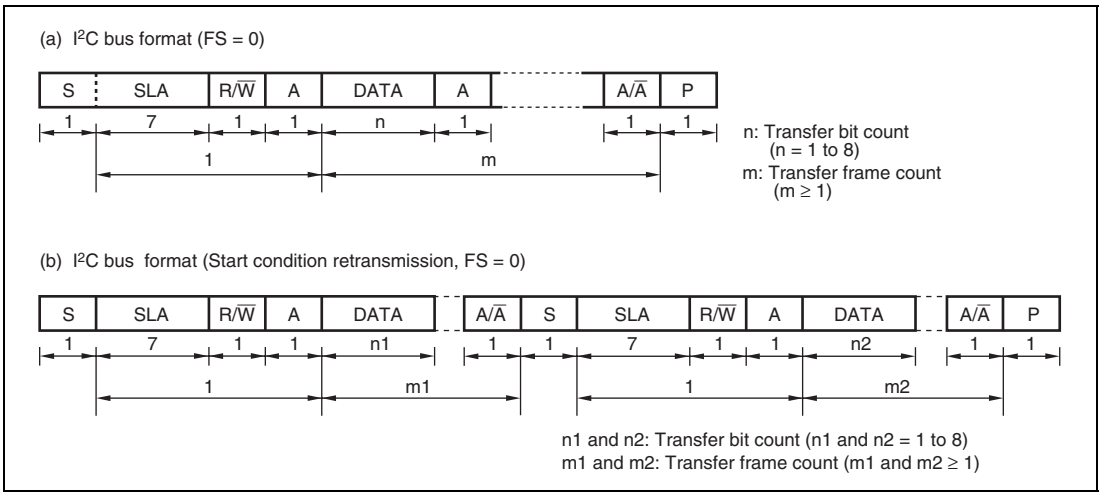


Figure 21.3 I²C Bus Formats

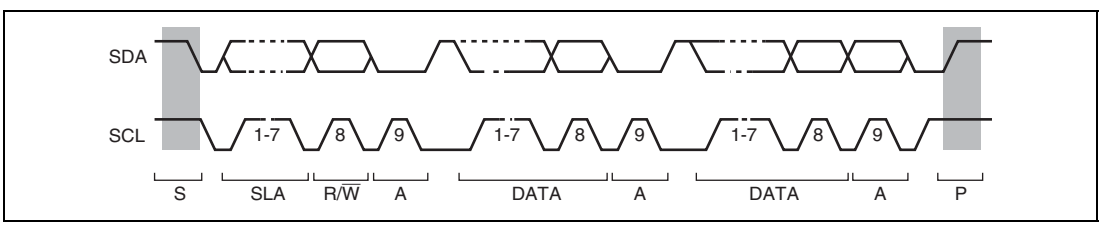


Figure 21.4 I²C Bus Timing

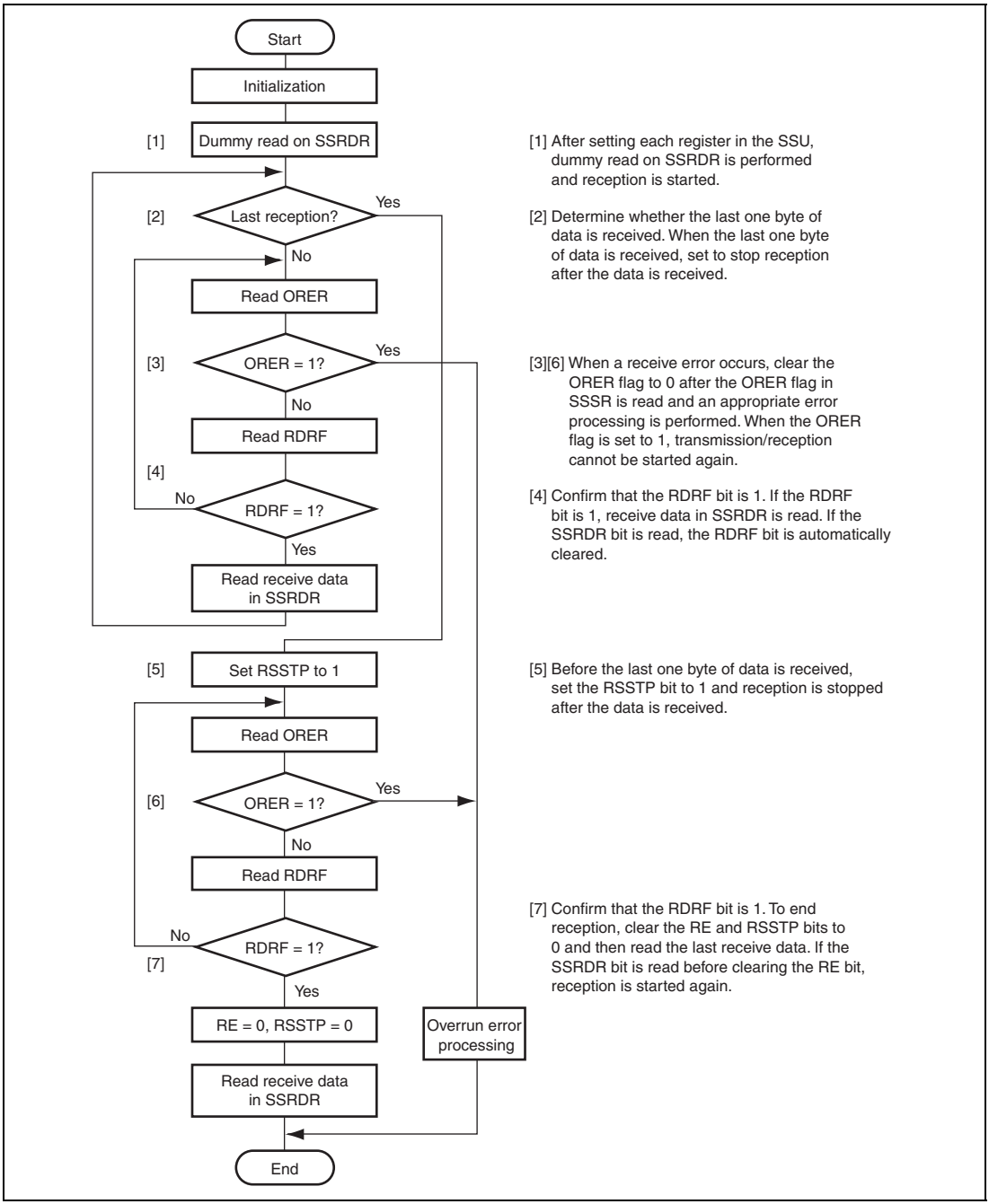


Figure 22.8 Sample Serial Reception Flowchart (MSS = 1)

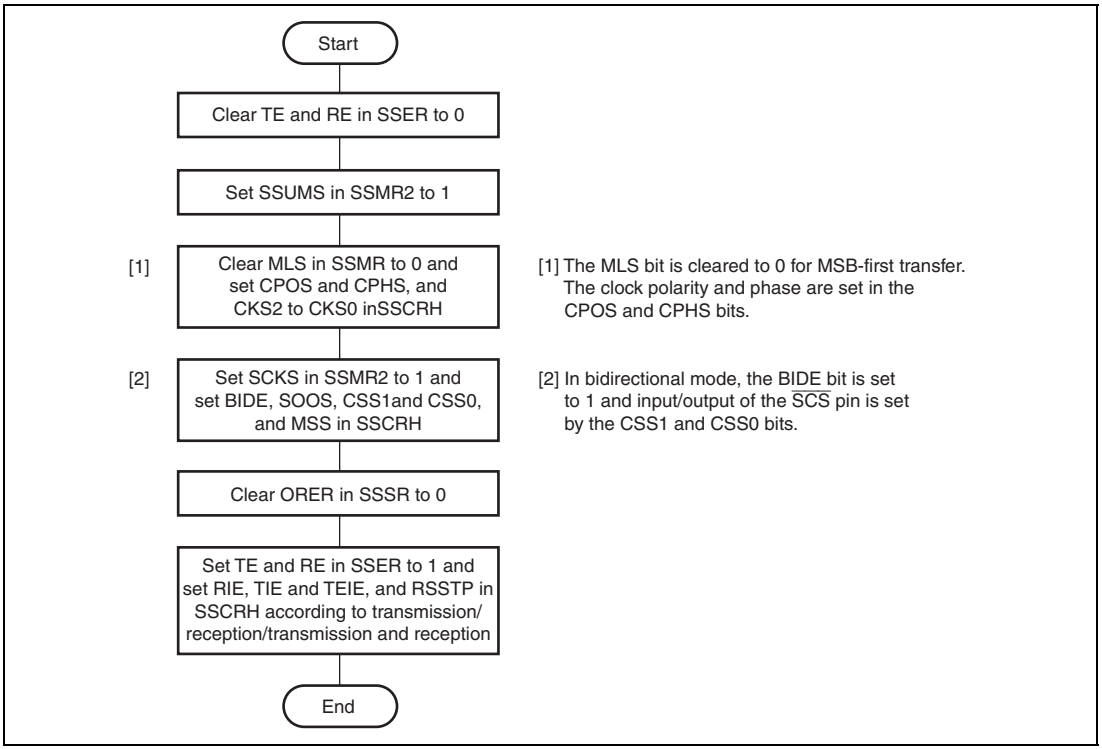


Figure 22.10 Initialization in Four-Line Bus Communication Mode

Section 26 Low-Voltage Detection Circuits

This microcontroller includes a low-voltage detection module consisting of three circuits, LVD0, LVD1, and LVD2.

The circuits are used to prevent abnormal operation (runaway execution) from occurring due to the power supply voltage falling and to recreate the state of the microcontroller before the power supply voltage fell when the power supply voltage rises again.

If the power supply voltage falls below a threshold voltage set by the users application, a warning can be given to the application so the application can shutdown in a controlled manner. If the power supply voltage continues to fall below a second programmable threshold voltage, the device can be safely placed in the reset state. This avoids the situation where the power supply voltage falls below the guaranteed operating voltage and the microcontroller enters an unstable state. Thus, system stability can be improved. If the power supply voltage rises again, active mode is automatically entered.

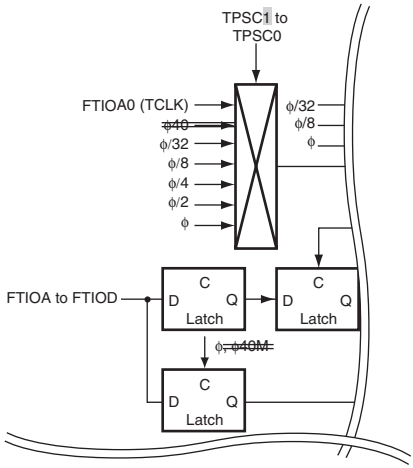
The circuits monitor the power-supply voltage, and generate a reset or an interrupt when the voltage falls below or rises above a specified value.

Figure 26.1 is a block diagram of the low-voltage detection circuits. Figures 26.2, 26.3, and 26.4 are block diagrams of the LVD2, LVD1 and LVD0 interrupt/reset generation circuits, respectively.

Register Name	Abbreviation	Number of Bits	Address	Module	Data Bus Width	Number of Access States
Event link setting register 19	ELSR19	8	H'FF0693	ELC	8	2
Event link setting register 21	ELSR21	8	H'FF0695	ELC	8	2
Event link setting register 22	ELSR22	8	H'FF0696	ELC	8	2
Event link setting register 23	ELSR23	8	H'FF0697	ELC	8	2
Event link setting register 24	ELSR24	8	H'FF0698	ELC	8	2
Event link setting register 29	ELSR29	8	H'FF069D	ELC	8	2
Event link setting register 30	ELSR30	8	H'FF069E	ELC	8	2
Event link setting register 31	ELSR31	8	H'FF069F	ELC	8	2
Event link setting register 32	ELSR32	8	H'FF06A0	ELC	8	2
Port-group setting register 1	PGR1	8	H'FF06A2	ELC	8	2
Port-group setting register 2	PGR2	8	H'FF06A3	ELC	8	2
Port-group control register 1	PGC1	8	H'FF06A6	ELC	8	2
Port-group control register 2	PGC2	8	H'FF06A7	ELC	8	2
Port buffer register 1	PDBF1	8	H'FF06AA	ELC	8	2
Port buffer register 2	PDBF2	8	H'FF06AB	ELC	8	2
Event link port setting register 0	PEL0	8	H'FF06AD	ELC	8	2
Event link port setting register 1	PEL1	8	H'FF06AE	ELC	8	2
Event link port setting register 2	PEL2	8	H'FF06AF	ELC	8	2
Event link port setting register 3	PEL3	8	H'FF06B0	ELC	8	2
Event link option setting register A	ELOPA	8	H'FF06B5	ELC	8	2
Event link option setting register B	ELOPB	8	H'FF06B6	ELC	8	2
Event link option setting register C	ELOPC	8	H'FF06B7	ELC	8	2
Event-generation timer control register	ELTMCR	8	H'FF06B8	ELC	8	2
Event-generation timer interval setting register A	ELTMSA	8	H'FF06B9	ELC	8	2
Event-generation timer interval setting register B	ELTMSB	8	H'FF06BA	ELC	8	2
Even-generation delay time selection register	ELTMDR	8	H'FF06BB	ELC	8	2
Event link control register	ELCR	8	H'FF06BC	ELC	8	2
ELC timer counter	ELTMCNT	16	H'FF06C0	ELC	16*[3]	2

Register Name	Abbreviation	Number of Bits	Address	Module	Data Bus Width	Number of Access States
Timer RD output master enable register 1_01	TRDOER1_01	8	H'FFFFD6	Timer RD unit 0 (channels 0 and 1 in common)	8	2
Time RD output master enable register 2_01	TRDOER2_01	8	H'FFFFD7		8	2
Timer RD output control register_01	TRDOCR_01	8	H'FFFFD8		8	2
Timer RC A/D conversion start trigger control register_01	TRDADCR_01	8	H'FFFFD9		8	2
Module standby control register 1	MSTCR1	8	H'FFFFDC	SYSTEM	8	2
Module standby control register 2	MSTCR2	8	H'FFFFDD	SYSTEM	8	2
Module standby control register 3	MSTCR3	8	H'FFFFDE	SYSTEM	8	2
Port data register 1	PDR1	8	H'FFFFE0	I/O Port	8	2
Port data register 2	PDR2	8	H'FFFFE1	I/O Port	8	2
Port data register 3	PDR3	8	H'FFFFE2	I/O Port	8	2
Port data register 5	PDR5	8	H'FFFFE4	I/O Port	8	2
Port data register 6	PDR6	8	H'FFFFE5	I/O Port	8	2
Port data register 8	PDR8	8	H'FFFFE7	I/O Port	8	2
Port data register 9*[1]	PDR9	8	H'FFFFE8	I/O Port	8	2
Port data register A	PDRA	8	H'FFFFE9	I/O Port	8	2
Port data register B	PDRB	8	H'FFFFEA	I/O Port	8	2
Port data register J	PDRJ	8	H'FFFFEC	I/O Port	8	2
Port control register 1	PCR1	8	H'FFFFF0	I/O Port	8	2
Port control register 2	PCR2	8	H'FFFFF1	I/O Port	8	2
Port control register 3	PCR3	8	H'FFFFF2	I/O Port	8	2
Port control register 5	PCR5	8	H'FFFFF4	I/O Port	8	2
Port control register 6	PCR6	8	H'FFFFF5	I/O Port	8	2
Port control register 8	PCR8	8	H'FFFFF7	I/O Port	8	2
Port control register 9*[1]	PCR9	8	H'FFFFF8	I/O Port	8	2
Port control register A	PCRA	8	H'FFFFF9	I/O Port	8	2
Port control register B	PCRB	8	H'FFFFFA	I/O Port	8	2
Port control register J	PCRJ	8	H'FFFFFC	I/O Port	8	2

Notes: 1. Not provided for the H8S/20103 and H8S/20115 Groups. These addresses are reserved.

Item	Page	Revision (See Manual for Details)
16.3.11 Digital Filtering Function for Input Capture Inputs Figure 16.54 Block Diagram of Digital Filter	588	Deleted 
16.3.14 Operation by Event Clear (2) Counting Event	593	Amended The counting of events by timer RD can be selected by ELOPA and ELOPB of the ELC. When the event specified in ELSR3 and ELSR4 occurs, event counter operation proceeds with that event as the source to drive counting, regardless of the setting of the TPSC[2:0] bits in TRDCR~~1~~ and the STR1 and STR0 bits in TRDSTR. When the value of the counter is read, the value read out is the actual number of input events.
Section 17 Timer RE 17.3 Operation of Realtime Clock Mode 17.3.4 Operation in Realtime Clock Mode Figure 17.5 Example of Realtime Clock Mode Operation	622	Amended