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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IrDA, LINbus, SCI, SSU, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f20114nfa-u0

Classification	Module/ Function	Description
Serial interfaces	I^2C bus interface 2 (IIC2)	• One channel (SSU and selection format) • Continuous transmission and reception possible • Two transmission/reception formats — I^2C bus format: generates start and stop conditions in master mode automatically, acknowledge bit, master or slave operation — Clock-synchronous serial format: no acknowledge bit, master operation only
	Hardware LIN interface	One channel (timer RA and SCI3 used)
Event link controller (ELC)		Events (interrupts) generated by peripheral modules can be interconnected between modules, enabling cooperation between the modules without CPU intervention.
I/O ports		• I/O pins — 55 (H8S/20103 and H8S/20115 Groups) — 69 (H8S/20203, H8S/20223, H8S/20215, and H8S/20235 Groups) • Pull-up resistors settable for all ports • LED driving capability

2.2 CPU Operating Modes

The H8S/2000 CPU has two operating modes: normal and advanced. Note that this LSI supports only advanced mode. Advanced mode supports a maximum 16-Mbyte address space.

2.2.1 Advanced Mode

- Address space

  Linear access to a maximum address space of 16 Mbytes is possible.
- Extended registers (En)

  The extended registers (E0 to E7) can be used as 16-bit registers. They can also be used as the upper 16-bit segments of 32-bit registers or address registers.
- Instruction set

  All instructions and addressing modes can be used.
- Exception vector table and memory indirect branch addresses

  In advanced mode, the top area starting at H'00000000 is allocated to the exception vector table in 32-bit units. In each 32 bits, the upper 8 bits are ignored and a branch address is stored in the lower 24 bits (see figure 2.1). For details of the exception vector table, see section 3, Exception Handling.

2.4.1 General Registers

The H8S/2000 CPU has eight 32-bit general registers. These general registers are all functionally alike and can be used as both address registers and data registers. When a general register is used as a data register, it can be accessed as a 32-bit, 16-bit, or 8-bit register. Figure 2.5 illustrates the usage of the general registers. When the general registers are used as 32-bit registers or address registers, they are designated by the letters ER (ER0 to ER7).

When the general registers are used as 16-bit registers, the ER registers are divided into 16-bit general registers designated by the letters E (E0 to E7) and R (R0 to R7). These registers are functionally equivalent, providing a maximum sixteen 16-bit registers. The E registers (E0 to E7) are also referred to as extended registers.

When the general registers are used as 8-bit registers, the R registers are divided into 8-bit general registers designated by the letters RH (R0H to R7H) and RL (R0L to R7L). These registers are functionally equivalent, providing a maximum sixteen 8-bit registers.

The usage of each register can be selected independently.

General register ER7 has the function of the stack pointer (SP) in addition to its general-register function, and is used implicitly in exception handling and subroutine calls. Figure 2.6 shows the stack.

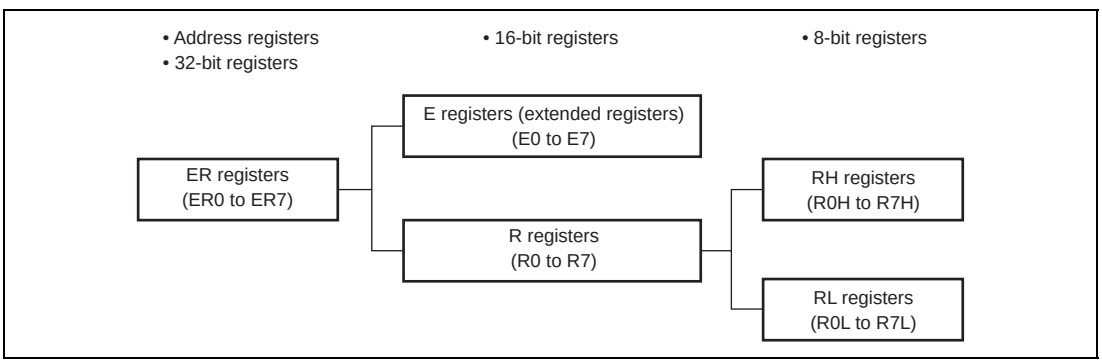


Figure 2.5 Usage of General Registers

Table 2.5 Logic Operations Instructions

Instruction	Size*	Function
AND	B/W/L	Rd ∧ Rs → Rd, Rd ∧ #IMM → Rd Performs a logical AND operation on a general register and another general register or immediate data.
OR	B/W/L	Rd ∨ Rs → Rd, Rd ∨ #IMM → Rd Performs a logical OR operation on a general register and another general register or immediate data.
XOR	B/W/L	Rd ⊕ Rs → Rd, Rd ⊕ #IMM → Rd Performs a logical exclusive OR operation on a general register and another general register or immediate data.
NOT	B/W/L	~ Rd → Rd Takes the one's complement (logical complement) of data in a general register.

Note: * Size refers to the operand size.
B: Byte
W: Word
L: Longword

2.9 Usage Notes

2.9.1 TAS Instruction

Only register ER0, ER1, ER4, or ER5 should be used when using the TAS instruction. The H8S and H8/300 Series C/C++ Compiler of Renesas Electronics Corp. does not generate a TAS instruction. Accordingly, when a TAS instruction is used as a user-defined embedded function, register ER0, ER1, ER4, or ER5 should be used.

2.9.2 STM and LDM Instructions

The ER7 register is used as a stack pointer in an STM and LDM instructions. Accordingly, ER7 cannot be stored by STM or loaded by LDM. Two, three, or four registers can be stored or loaded by a single STM or LDM instruction. The combination of registers that can be stored or loaded are as follows.

- Two registers: ER0 and ER1, ER2 and ER3, or ER4 and ER5
- Three registers: ER0 to ER2 or ER4 to ER6
- Four registers: ER0 to ER3

The H8S and H8/300 Series C/C++ Compiler of Renesas Electronics Corp. does not generate an STM or LDM instruction that uses ER7.

2.9.3 Note on Bit Manipulation Instructions

Bit manipulation instructions such as BSET, BCLR, BNOT, BST, and BIST read data in byte units, perform bit manipulation, and write data in byte units. Thus, care must be taken when these bit manipulation instructions are executed for a register or port including write-only bits.

In addition, the BCLR instruction can be used to clear the flag of an internal I/O register. In this case, if the flag to be cleared has been set by an interrupt processing routine, the flag need not be read before executing the BCLR instruction.

(5) Port 6

(a) Port 6 Peripheral Function Mapping Register 1 (PMCR61)

Address: H'FF0054

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	—	P61MD[2:0]			—	P60MD[2:0]		
Value after reset:	0	1	0	1	0	1	0	1

Bit	Symbol	Bit Name	Description	R/W
7	—	Reserved	This bit is always read as 0. The write value should always be 0.	—
6 to 4	P61MD[2:0]	P61 function select	000: Setting prohibited 001: $\overline{\text{IRQ1}}$ input 010: RXD input (SCI3_1) 011: FTIOB input/output (timer RC)* 100: TCLKB input (timer RG) 101: FTIOB0 input/output (timer RD_0) (initial value) 110: TRGB input (timer RB) 111: Setting prohibited	R/W
3	—	Reserved	This bit is always read as 0. The write value should always be 0.	—
2 to 0	P60MD[2:0]	P60 function select	000: Setting prohibited 001: $\overline{\text{IRQ0}}$ input 010: SCK3 input/output (SCI3_1) 011: FTIOA input/output (timer RC)* 100: TCLKA input (timer RG) 101: FTIOA0 input/output (timer RD_0) (initial value) 110: TREO output (timer RE) 111: Setting prohibited	R/W

Note: * The timer RC is not available on the H8S/20203, H8S/20223, H8S/20215, and H8S/20235 Groups. These bits are reserved and the function cannot be selected for these groups.

(b) Port 6 Peripheral Function Mapping Register 2 (PMCR62)

Address: H'FF0055

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	—	P63MD[2:0]			—	P62MD[2:0]		
Value after reset:	0	1	0	1	0	1	0	1

Bit	Symbol	Bit Name	Description	R/W
7	—	Reserved	This bit is always read as 0. The write value should always be 0.	—
6 to 4	P63MD[2:0]	P63 function select	000: Setting prohibited 001: $\overline{\text{IRQ3}}$ input 010: $\overline{\text{TRCOI}}$ input (timer RC)* 011: FTIOD input/output (timer RC)* 100: TGIOB input/output (timer RG) 101: FTIOD0 input/output (timer RD_0) (initial value) 110: TRAO output (timer RA) 111: Setting prohibited	R/W
3	—	Reserved	This bit is always read as 0. The write value should always be 0.	—
2 to 0	P62MD[2:0]	P62 function select	000: Setting prohibited 001: $\overline{\text{IRQ2}}$ input 010: TXD output (SCI3_1) 011: FTIOC input/output (timer RC)* 100: TGIOA input/output (timer RG) 101: FTIOC0 input/output (timer RD_0) (initial value) 110: TRBO output (timer RB) 111: Setting prohibited	R/W

Note: * The timer RC is not available on the H8S/20203, H8S/20223, H8S/20215, and H8S/20235 Groups. These bits are reserved and the function cannot be selected for these groups.

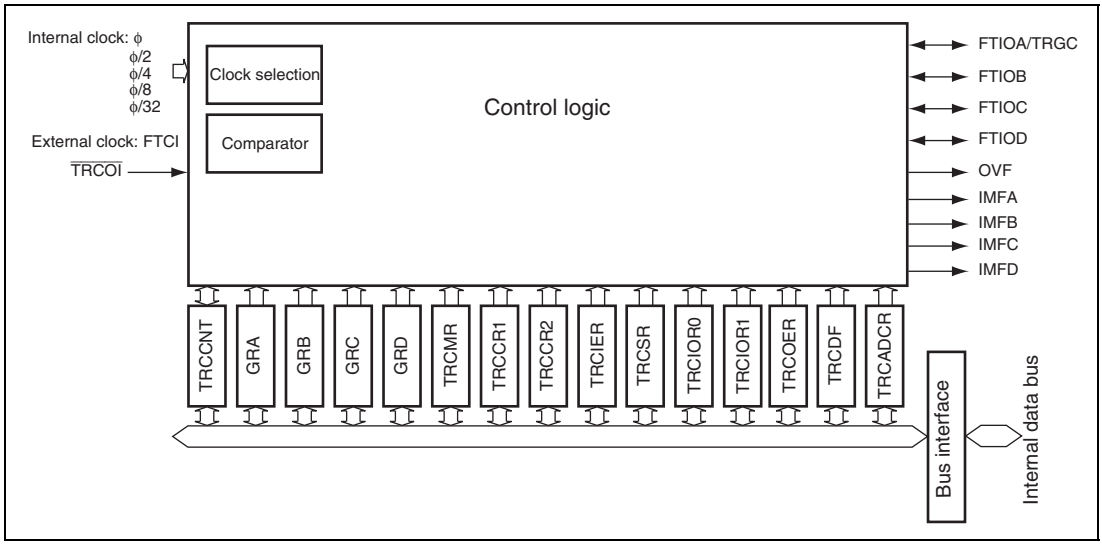


Figure 15.1 Timer RC Block Diagram

Table 15.2 summarizes the timer RC pins.

Table 15.2 Pin Configuration

Pin Name	Input/ Output	Function
FTCI	Input	External clock input pin
FTIOA/TRGC	I/O	Output pin for GRA output compare/input pin for GRA input capture/ external trigger input pin (TRGC)
FTIOB	I/O	Output pin for GRB output compare/input pin for GRB input capture/ PWM output pin in PWM mode
FTIOC	I/O	Output pin for GRC output compare/input pin for GRC input capture/ PWM output pin in PWM mode
FTIOD	I/O	Output pin for GRD output compare/input pin for GRD input capture/ PWM output pin in PWM mode
$\overline{\text{TRCOI}}$	Input	Input pin for timer output disabling signal

Figure 16.9 illustrates periodic counter operation.

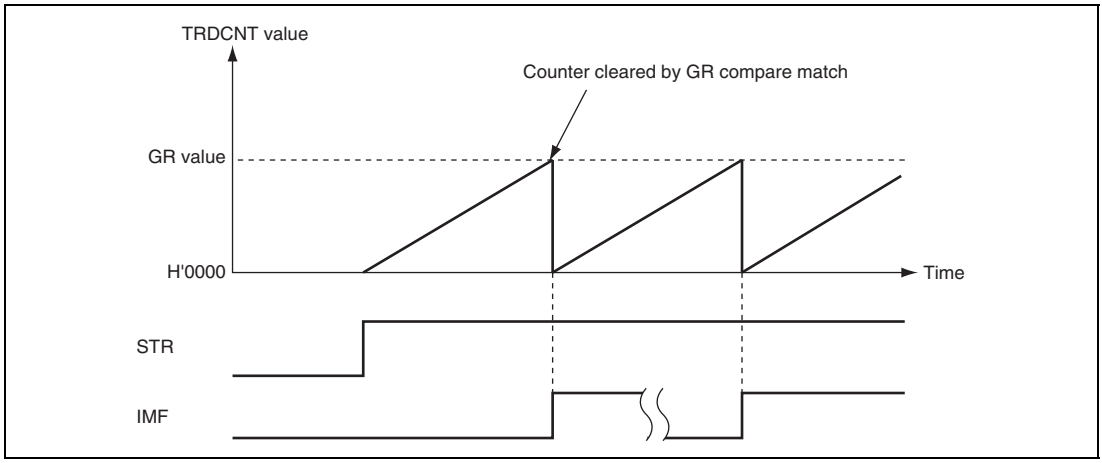


Figure 16.9 Periodic Counter Operation

(2) TRDCNT Count Timing

- Internal clock operation

  A system clock (ϕ), or four types of clocks (ϕ/2, ϕ/4, ϕ/8, or ϕ/32) that are generated by dividing the system clock can be selected by bits TPSC2 to TPSC0 in TRDCR.

  Figure 16.10 illustrates this timing.

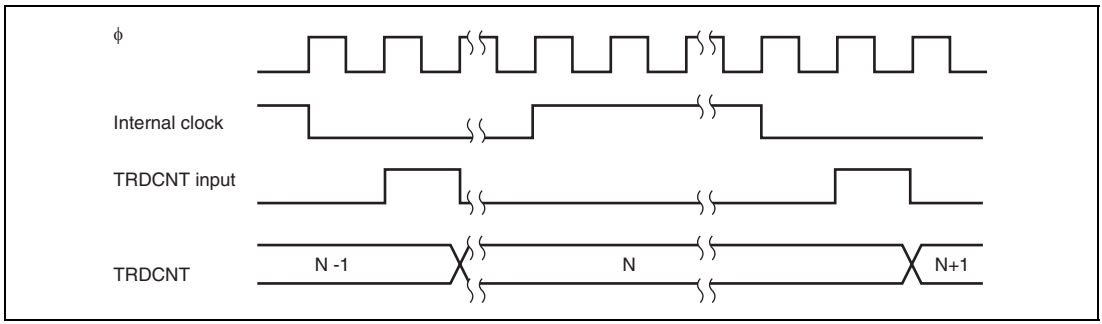


Figure 16.10 Count Timing in Internal Clock Operation

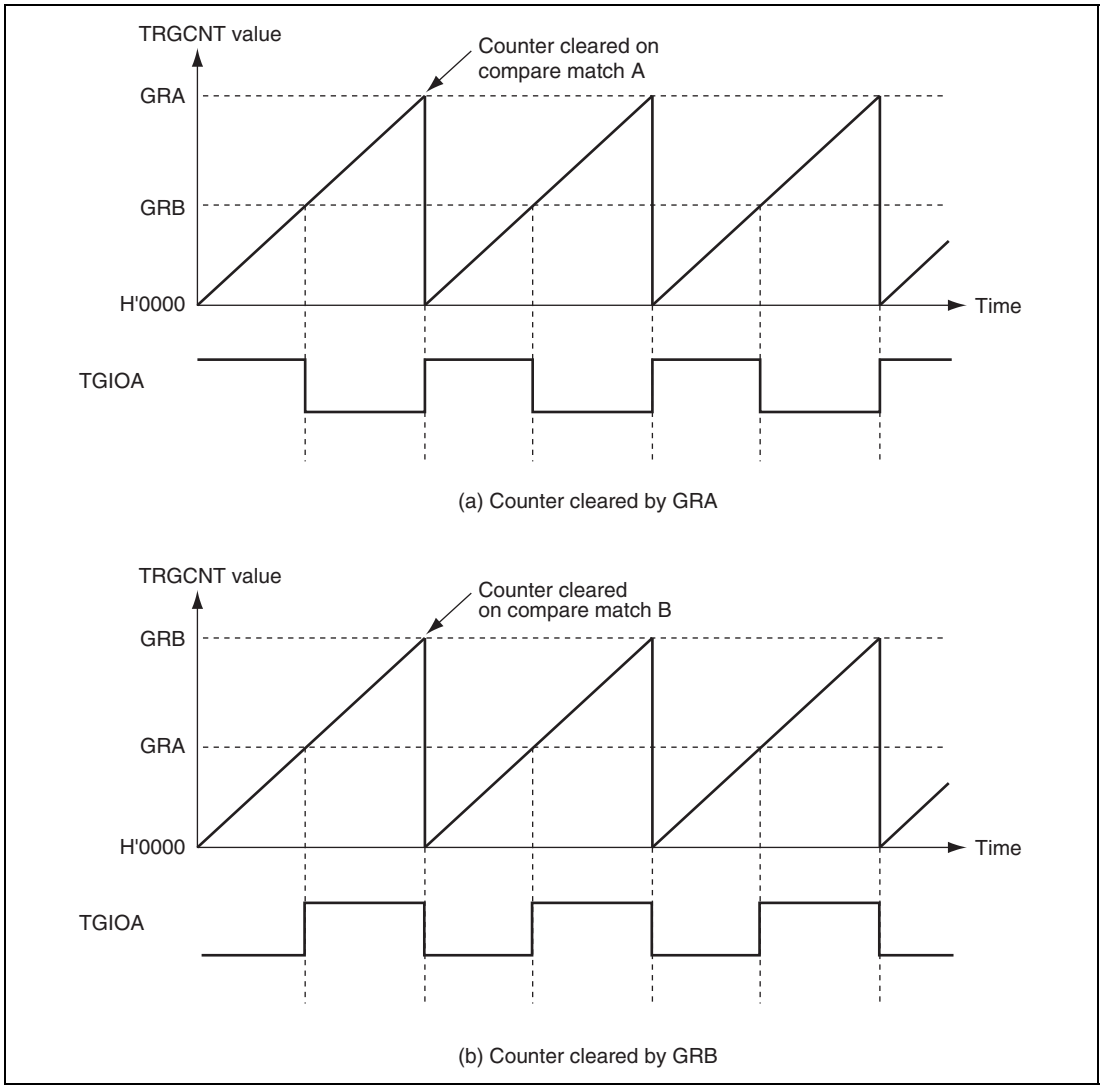


Figure 18.10 Example of PWM Mode Operation (1)

Figure 18.11 shows examples of PWM waveform output with 0% duty cycle and 100% duty cycle in PWM mode. When GRB compare match is set as the counter clearing source and the set value in GRA is greater than the value in GRB, the duty cycle of the PWM waveform is 0%. When GRA compare match is set as the counter clearing source and the set value in GRB is greater than the value in GRA, the duty cycle is 100%.

Bit	Symbol	Bit Name	Description	R/W
4	PM	Parity mode	(Enabled only when the PE bit is 1 in asynchronous mode) 0: Selects even parity. 1: Selects odd parity.	R/W
3	STOP	Stop bit length	(Enabled only in asynchronous mode) 0: 1 stop bit 1: 2 stop bits	R/W
2	MP	Multiprocessor mode	0: The multiprocessor communication function is disabled. 1: The multiprocessor communication function is enabled*2	R/W
1, 0	CKS[1:0]	Clock select 0 and 1	00: ϕ clock (n = 0) 01: ϕ/4 clock (n = 1) 10: ϕ/14 clock (n = 2) 11: ϕ/64 clock (n = 3)	R/W

Notes: 1. The SMR value is retained when (module) standby mode is entered.
2. In clocked synchronous mode, clear this bit to 0.

- STOP bit (stop bit length)

  Selects the stop bit length in transmission. For reception, only the first stop bit is checked, regardless of the value in the bit. If the second stop bit is 0, it is treated as the start bit of the next transmit character.

- MP bit (multiprocessor mode)

  When this bit is set to 1, the multiprocessor communication function is enabled. The PE bit and PM bit settings are invalid in multiprocessor mode.

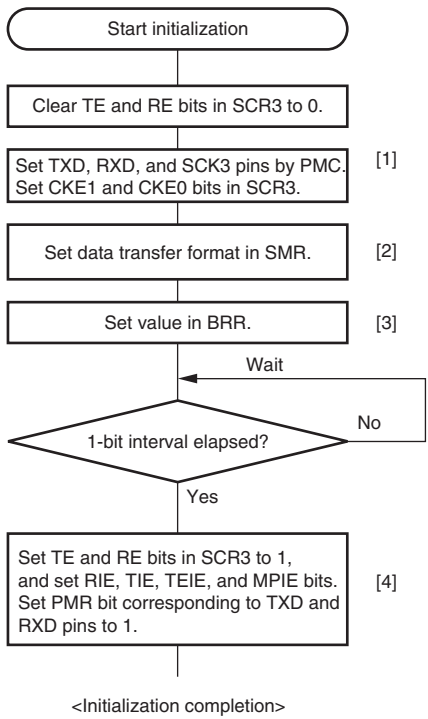
- CKS[1:0] bits (clock select 1, 0)

  These bits select the clock source for the baud rate generator.

  For the relationship between the bit rate register setting and the baud rate, see section 20.2.8, Bit Rate Register (BRR). n is the decimal representation of the value of n in BRR (see section 20.2.8, Bit Rate Register (BRR)).

20.3.2 SCI3 Initialization

Figure 20.4 shows a sample flowchart to initialize the SCI3. When the TE bit is cleared to 0, the TDRE flag is set to 1. Note that clearing the RE bit to 0 does not initialize the contents of the RDRF, PER, FER, and OER flags, or the contents of RDR. When the external clock is used in asynchronous mode, the clock must be supplied even during initialization.



[1] With the PMC, select which of the TXD, RXD, and SCK3 pins are to be used. Set the clock selection in SCR3. Be sure to clear the other bits in SCR3 to 0. When clock output is selected in asynchronous mode, after the CKE1 and CKE0 settings have been made, output of the clock signal begins immediately upon setting of the PMR bits that correspond to pins selected by SCK3. When clock output is selected with reception in clock-synchronous mode, and CKE1, CKE0, and RE are set to 1, output of the clock signal begins immediately upon setting of the PMR bits that correspond to pins selected by SCK3.

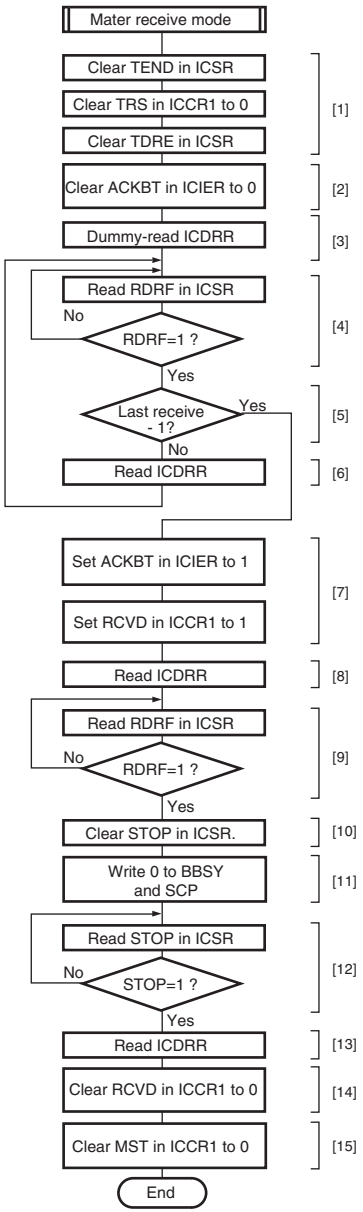
[2] Set the data transfer format in SMR.

[3] Write the value corresponding to the bit rate to BRR. Not necessary if an external clock is used.

[4] Wait at least one bit interval, then set the TE bit or RE bit in SCR3 to 1. For transmission, enable use of the TXD output pin by setting the PMR bit for the pin selected as TXD by the PMC to 1. For reception, enable use of the RXD input pin by setting the PMR bit for the pin selected as RXD by the PMC to 1.

Also set the RIE, TIE, TEIE, and MPIE bits, according to the required interrupts. In asynchronous mode, SCI3 is in the mark state (active) for transmission and in the space state (idle) while waiting for the start bit during reception. After the TE bit has been set to 1 in the case of transmission, transmission is enabled after the output of a frame with all bits 1.

Figure 20.4 Sample Flowchart for Initializing SCI3



[1] Clear TEND, select master receive mode, and then clear TDRE.*

[2] Set acknowledge to the transmit device.*

[3] Dummy-read ICDRR.*

[4] Wait for 1 byte to be received

[5] Check whether it is the (last receive - 1).

[6] Read the receive data.

[7] Set acknowledge of the last byte. Disable continuous reception (RCVD = 1).

[8] Read the (last byte - 1) of receive data.

[9] Wait for the last byte to be receive.

[10] Clear the STOP flag.

[11] Issue the stop condition.

[12] Wait for the generation of stop condition.

[13] Read the last byte of receive data.

[14] Clear RCVD.

[15] Set slave receive mode.

Note: Do not activate an interrupt during the execution of steps [1] to [3].

Supplementary explanation: When one byte is received, steps [2] to [6] are skipped after step [1] before jumping to step [7]. The step [8] is dummy-read in ICDRR.

Figure 21.18 Sample Flowchart for Master Receive Mode

- SOOS bit (SSO/SSI pins open-drain output select)

  Selects whether the serial data output pin is CMOS output or NMOS open-drain output. However, when the SSI output function is allocated to P57, this bit selects between NMOS push-pull output and NMOS open-drain output. The serial data output pin is changed according to the register setting value. For details, see section 22.3.3, Relationship between Data Input/Output Pin and Shift Register.

- CSOS bit ($\overline{\text{SCS}}$ pin open-drain output select)

  Selects whether the serial data output pin is CMOS output or NMOS open-drain output. However, when the $\overline{\text{SCS}}$ output function is allocated to P56, this bit selects between NMOS push-pull output and NMOS open-drain output.

- SSUMS bit (SSU mode select)

  Selects which combination of the serial data input pin and serial data output pin is used.

  For details, see section 22.3.3, Relationship between Data Input/Output Pin and Shift Register.

Bit	Symbol	Bit Name	Description	R/W
4, 3	—	Reserved	These bits are read as 0. The write value should be 0.	—
2	ORER	Overrun error flag	[Setting condition] • When the next serial reception is completed while RDRF = 1 [Clearing condition] • When 0 is written to this bit after reading 1	R/W
1	—	Reserved	These bits are read as 0. The write value should be 0.	—
0	CE	Conflict error flag	[Setting conditions] • When serial communication is started while SSUMS = 1 in SSMR2 and MSS = 1 in SSCRH, the $\overline{SCS}$ pin input is low • When the $\overline{SCS}$ pin level changes from low to high during transfer while SSUMS = 1 in SSMR2 and MSS = 0 in SSCRH [Clearing condition] • When 0 is written to this bit after reading 1	R/W

Notes: In standby mode, SSSR is reset.

* The DTC clears the peripheral module flags when all of the following three conditions are satisfied.

1. When the DISEL bit is 0.
2. When the transfer counter (DTC transfer count register A (CRA) in normal mode and repeat mode, or DTC transfer count register B (CRB) in block mode) is not 0.
3. When chain transfer is not used.

- ORER bit (overrun error flag)

  Indicates that the RDRF bit is abnormally terminated in reception because an overrun error has occurred. SSRDR retains received data before the overrun error occurs and the received data after the overrun error occurs is lost. When this bit is set to 1, subsequent serial reception cannot be continued. When the MSS bit in SSCRH is 1, this is also applied to serial transmission.

(2) Low Voltage Detect Interrupt 2 (LVDI2)

LVDI2 is an interrupt generated by the LVD2 circuit. Figure 26.8 shows the operation timing of LVDI2.

The LVD2 enters the module-standby state after release from a power-on reset. To operate the LVDI2, set the VD2E bit in LD2CRL to 1, wait for 50 µs ($t_{d(E-A)}$) until the detection voltage and the low-voltage detection circuit 2 operation have stabilized using a software timer, etc., then clear the VD2MS bit to 0 and set the VD2RE bit to 1 in LD2CRH. After that, the output settings of I/O ports must be made. To cancel the LVDI2, first the VD2RE bit in LD2CRH should be cleared to 0 and then the VD2E bit in LD2CRL should be cleared to 0. Figure 26.9 shows the procedure to set the LVDI2.

When the power-supply voltage falls below Vdet2, the LVDI2 clears the $\overline{\text{LVDINT2}}$ signal to 0 and the VD2DFS bit in LD2CRH is set to 1. If the VD2DFS or VD2IRCS bit in LD2CRH is 1 at this time, an LVD2 interrupt request is simultaneously generated. In this case, the necessary data must be saved in the on-chip flash memory area or external EEPROM, etc, and a transition must be made to standby mode or sleep mode. Until this processing is completed, the power supply voltage must be higher than the lower limit of the guaranteed operating voltage.

When the power-supply voltage does not fall below Vdet0 but rises above Vdet2, the LVDI2 sets the $\overline{\text{LVDINT2}}$ signal to 1 and set the VD2UF bit in LD2CRH to 1. If the VD2DFS bit in LD2CRH is 1 or the VD2IRCS bit in LD2CRH is 0 at this time, an LVD2 interrupt request is simultaneously generated.

If the power supply voltage falls below Vdet0, a power-on reset occurs.

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
TRDOER2_23*5	PTO	—	—	—	—	—	—	—	Timer RD Unit 1 (channels 2 and 3 in common)
TRDOCR_23*5	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0	
TRDADCR_23*5	ADTRGD1E	ADTRGC1E	ADTRGB1E	ADTRGA1E	ADTRGD0E	ADTRGC0E	ADTRGB0E	ADTRGA0E	
ICCR1	ICE	RCVD	MST	TRS	CKS[3:0]				IIC2/SSU
SSCRH	—	RSSTP	MSS	—	—	CKS[2:0]			
ICCR2	BBSY	SCP	SDAO	SDAOP	SCLO	—	IICRST	—	
SSCRL	—	—	SOL	SOLP	—	—	SRES	—	
ICMR	MLS	WAIT	—	—	BCWP	BC[2:0]			
SSMR	MLS	CPOS	CPHS	—	—	BC[2:0]			
ICIER	TIE	TEIE	RIE	NAKIE	STIE	ACKE	ACKBR	ACKBT	
SSER	TIE	TEIE	RIE	TE	RE	—	—	CEIE	
ICSR	TDRE	TEND	RDRF	NACKF	STOP	AL_OVE	AAS	ADZ	
SSSR	TDRE	TEND	RDRF	—	—	ORER	—	CE	
SAR	SVA[6:0]							FS	
SSMR2	BIDE	SCKS	CSS[1:0]		SCKOS	SOOS	CSOS	SSUMS	
ICDRT									
SSTDR									
ICDRR									
SSRDR									
DADR0									D/A converter
DADR1									
DACR	DAOE1	DAOE0	—	—	—	—	—	—	
IrCR	IrE		IrCK[2:0]		IrTXINV	IrRXINV	—	—	SCI3_2 (IrDA)
ADDR0									A/D converter (unit 1)
			—	—	—	—	—	—	
CMPR	CMP7	CMP6	CMP5	CMP4	CMP3	CMP2	CMP1	CMP0	
ADDR1									
			—	—	—	—	—	—	

Section 28 Electrical Characteristics

28.1 Absolute Maximum Ratings

Table 28.1 Absolute Maximum Ratings

Item		Symbol	Value	Unit	Notes
Power supply voltage		V_{CC}	–0.3 to +6.5	V	*1
Analog power supply voltage		AV_{CC}	–0.3 to +6.5	V	
Input voltage	All pins (other than AN pin, DA pin, OSC1, and X1)	V_{IN}	–0.3 to V_{CC} +0.3	V	
	AN pin, DA pin	AV_{IN}	–0.3 to AV_{CC} +0.3	V	
	OSC1, X1	V_{IN}	–0.3 to +1.65	V	*2
	OSC1	V_{IN}	–0.3 to V_{CC} +0.3	V	*3
Operating temperature		T_{opr}	N version: –20 to +85	°C	*4
			D version: –40 to +85	°C	
Storage temperature		T_{stg}	–55 to +125	°C	

Notes: 1. Permanent damage may result if maximum ratings are exceeded. Normal operation should be under the conditions specified in Electrical Characteristics. Exceeding these values can result in incorrect operation and reduced reliability.

2. The OSC1 pin is used when the external oscillator function is selected. (PMRJ1 = 1, PMRJ0 = 1)

3. When the external clock input function is selected. (PMRJ1 = 0, PMRJ0 = 1)

4. N-version products are used for customer products. D-version products are used for customer products and industrial equipment.

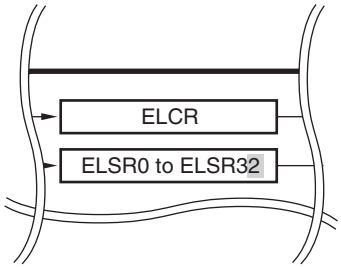
Item	Page	Revision (See Manual for Details)
Section 9 Peripheral I/O Mapping Controller Table 9.1 Multiplexed Pin Functions (Ports 1, 2, 3, 5, and 6)	237	Amended

Group 1	Pin Name	Function 4
Port 1 Port 2 Port 3 Port 5 Port 6	Pm7	~~SCL/~~SSI input/output
	Pm6	~~SDA/~~$\overline{\text{SCS}}$ input/output

Notes: 1. The timer RC is not available on the H8S/20203, H8S/20223, H8S/20215, and H8S/20235 Groups; therefore, the function cannot be selected for these groups.

2. The SCL and SDA functions for the IIC2 module are not allocatable to pins other than P56 and P57.

9.1 Register Description 9.1.2 Port Group 1 Peripheral Function Mapping Registers 1 to 4 (PMCRn1 to PMCRn4 (n = 1, 2, 3, 5, and 6)) (c) Port 1 Peripheral Function Mapping Register 3 (PMCR13)	243	Added Notes: 1. For the H8S/20103 and H8S/20115 Groups, P14 is not provided and P14MD[2:0] are reserved. The initial value is B'001. The write value should be B'001.

Item	Page	Revision (See Manual for Details)
11.8 Usage Notes 11.8.4 Limitation on Usage of the Interrupt Vector Offset Register (VOFR)	368	Added
Section 12 Event Link Controller 12.1 Overview Figure 12.1 Block Diagram of Event Link Controller	370	Amended 
12.2 Register Descriptions 12.2.2 Event Link Setting Registers 0 to 32 (ELSR0 to ELSR32)	372	Amended … Table 12.1 shows the correspondence between ELSR0 to ELSR32 and the peripheral modules. …
12.2.7 Port-Group Control Registers 1 and 2 (PGC1 and PGC2)	379	Amended … The correspondence between PGC and ports is shown in table 12.3.
12.2.8 Port Buffer Registers 1 and 2 (PDBF1 and PDBF2)	380	Amended PDBF is an 8-bit readable/writable register used in combination with PGR. For PDBF operations, see section 12.3, Operation. The correspondence of PDBF and PDR is shown in table 12.3.
12.3 Operation 12.3.5 Port Operation upon Event Input and Event Generation	392	Amended (1) Single-Ports and Port-Groups … A port-group can be set by specifying any two or more bits in the port* to which an event can be connected using the PGC register. …