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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IrDA, LINbus, SCI, SSU, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f20115nfa-u0

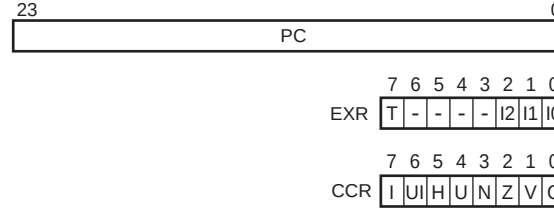
2.4 Register Configuration

The H8S/2000 CPU has the internal registers shown in figure 2.4. There are two types of registers: general registers and control registers. Control registers are a 24-bit program counter (PC), an 8-bit extended control register (EXR), and an 8-bit condition code register (CCR).

General Registers (Rn) and Extended Registers (En)

	15 0	7 0	7 0
ER0	E0	R0H	R0L
ER1	E1	R1H	R1L
ER2	E2	R2H	R2L
ER3	E3	R3H	R3L
ER4	E4	R4H	R4L
ER5	E5	R5H	R5L
ER6	E6	R6H	R6L
ER7 (SP)	E7	R7H	R7L

Control Registers



Legend:

SP	: Stack pointer	H	: Half-carry flag
PC	: Program counter	U	: User bit
EXR	: Extended control register	N	: Negative flag
T	: Trace bit	Z	: Zero flag
I2 to I0	: Interrupt mask bits	V	: Overflow flag
CCR	: Condition-code register	C	: Carry flag
I	: Interrupt mask bit		
UI	: User bit or interrupt mask bit*		

Note: * For this LSI, the interrupt mask bit is not available.

Figure 2.4 CPU Internal Registers

4.6.2 Instructions that Disable Interrupts

Instructions that disable interrupts are LDC, ANDC, ORC, and XORC. After any of these instructions is executed, all interrupts including NMI are disabled and the next instruction is always executed. When the I bit is set by one of these instructions, the new value becomes valid after two states that execution of the instruction ends.

4.6.3 Time when Interrupts are Disabled

There are time when interrupt acceptance is disabled by the interrupt controller. The interrupt controller disables interrupt acceptance for a 3-state period after the CPU has updated the mask level with an LDC, ANDC, ORC, or XORC instruction.

4.6.4 Interrupts during Execution of EEPMOV Instruction

Interrupt operation differs between the EEPMOV.B instruction and the EEPMOV.W instruction.

With the EEPMOV.B instruction, an interrupt request (including NMI) issued during the transfer is not accepted until the transfer is completed.

With the EEPMOV.W instruction, if an interrupt request is issued during the transfer, interrupt exception handling starts at a break in the transfer cycle. The PC value saved on the stack in this case is the address of the next instruction. Therefore, if an interrupt is generated during execution of an EEPMOV.W instruction, the following coding should be used.

```
L1:   EEPMOV.W
      MOV.W     R4,R4
      BNE       L1
```

5.3 Operation of Selection of System Reference Clock

After a reset, this LSI enters active mode operating in low-speed clocks. The user, by means of software, can change the system reference clock from a low-speed OCO clock to the main oscillator clock or a sub-oscillator clock.

Figure 5.2 shows a transition diagram between system reference clock states. Table 5.3 shows conditions under which clock sources can be switched.

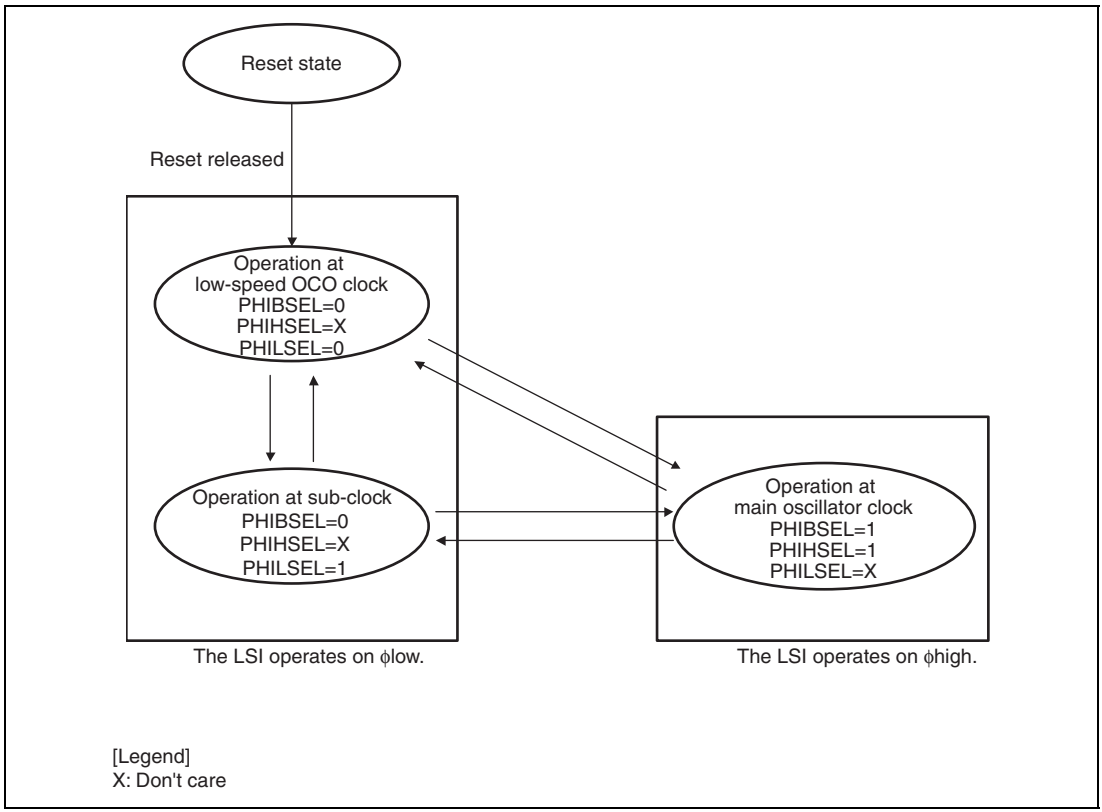


Figure 5.2 Transition Diagram between LSI System Reference Clock States

Section 7 ROM

The features of the on-chip flash memory are described below.

7.1 Overview

- Programming/erasing method

  Four bytes are programmed simultaneously. A single block is erased at a time; only one block should be erased at a time even when the entire ROM area is to be erased.
- Programming/erasing time

  Programmable ROM programming time: 150 µs (typ.) for 4-byte simultaneous programming, i.e., 38 µs (typ.) per byte

  Data flash programming time: 300 µs (typ.) for 4-byte simultaneous programming, i.e., 75 µs (typ.) per byte

  Erasing time: 200 ms (typ.) per block for the programmable ROM and data flash areas.
- Reprogramming capability: The programmable ROM area can be reprogrammed up to 1000 times and the data flash area can be reprogrammed up to 10000 times.
- Two on-board programming modes

  Boot mode: The on-chip SCI can be used for programming/erasing the user ROM area. In this mode, the communication bit rate between the host and this LSI can be automatically adjusted.

  User mode: Any interface can be used for programming/erasing the user ROM area.
- Programmer mode

  A PROM programmer is used for programming/erasing.
- Protection function

  Flash memory can be protected against erroneous programming and erasure.

  Lock-bit protection function can be set through software.
- PROM-programmer protection/Boot-mode protection

  By writing specified data to a specified address range in user ROM, protection of the user-ROM area in boot mode and PROM-programmer mode can be established.
- Access cycle

  Programmable ROM: One state

  Data flash: Two states

Table 7.9 Error Codes

Code	Description
H'00	No error
H'11	Checksum error
H'12	Programming size error
H'21	Device-code disagreement error
H'22	Clock-mode disagreement error
H'24	Bit-rate selection disable error
H'25	Input frequency error
H'26	Frequency division ratio error
H'27	Operating frequency error
H'29	Block number error
H'2A	Address error
H'2B	Data size error
H'51	Erasure error
H'52	Non-erased error
H'53	Programming error
H'54	Selection processing error
H'61	ID code mismatch error
H'63	Erasure error when ID code mismatch occurs
H'80	Command error
H'FF	Bit-rate-adjustment acknowledge error

7.5.3 Programming/Erasing in User Mode

On-board programming/erasing of individual flash memory blocks is also possible in user mode by branching to the user programming/erasure-control program. The user must set the branching conditions and provide the on-board means of supplying the programming data. The flash memory must contain the user programming/ erasure-control program or a program that allows the user programming/erasure-control program to be supplied externally. As the flash memory itself cannot be read during programming/erasing, transfer the user programming/erasure-control program to the on-chip RAM to execute, as in boot mode. Figure 7.12 shows a sample procedure for programming/erasing in user mode. Prepare user programming/erasure-control program in accordance with the description in section 7.6, Programming/Erasing.

(3) Programming

A programming command is used to program data in the flash memory in 4-byte units.

Command or data size can be set depending on the FMWUS bit in FLMCR1. Setting the FMWUS bit to 0 enables using byte instructions. When H'41 is written in the first command cycle and data is written to the programming address in the second through fifth command cycles, programming and verifying are automatically started*.

Setting the FMWUS bit to 1 enables using word instructions. When H'4141 is written in the first command cycle and data is written to the programming address in the second and third command cycles, programming and verifying are started*.

Completion of programming is indicated by the FMRDY bit in FLMSTR. The FMRDY bit is read as 0 during programming, and read as 1 after programming completion.

After programming completion, the programming result can be checked by reading the FMPRSF bit in FLMSTR. (See the description in (9) below, Full Status Checking.)

Figure 7.16 shows the programming flowchart.

Do not additionally program the already-programmed addresses.

Note that if the lock bit is 0 (locked) in the specified block and the FMLBD bit is 0 (lock bit enabled), a programming command is not accepted for the specified block.

In EW1 mode, do not execute this command for the block in which the reprogramming-control program is located.

The FMRDY bit in FLMSTR changes to 0 when programming is started, and changes to 1 when completed.

Note: * The lower two bits of the programming addresses are ignored.

(5) Lock-Bit Program

When H'77 is written in the first command cycle and H'D0 is written to any address in the block in the second command cycle, lock-bit programming of the specified block is started.

Completion of lock-bit programming is indicated by the FMRDY bit in FLMSTR. The FMRDY bit is read as 0 during lock-bit programming, and read as 1 after lock-bit programming completion.

After lock-bit programming completion, the lock-bit programming result can be checked by reading the FMPRSF bit in FLMSTR. (See the description in (9) below, Full Status Checking.)

Figure 7.18 shows the lock-bit programming flowchart.

The FMRDY bit in FLMSTR changes to 0 when lock-bit programming is started, and changes to 1 when completed.

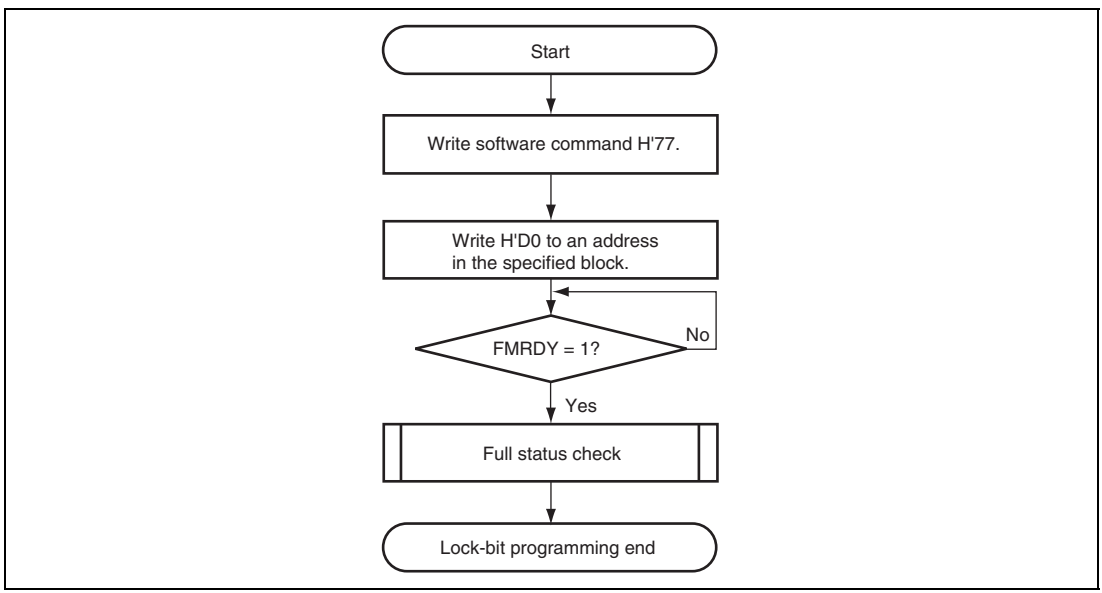


Figure 7.18 Lock-Bit Programming Flowchart

(b) Port 6 Peripheral Function Mapping Register 2 (PMCR62)

Address: H'FF0055

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	—	P63MD[2:0]			—	P62MD[2:0]		
Value after reset:	0	1	0	1	0	1	0	1

Bit	Symbol	Bit Name	Description	R/W
7	—	Reserved	This bit is always read as 0. The write value should always be 0.	—
6 to 4	P63MD[2:0]	P63 function select	000: Setting prohibited 001: $\overline{\text{IRQ3}}$ input 010: $\overline{\text{TRCOI}}$ input (timer RC)* 011: FTIOD input/output (timer RC)* 100: TGIOB input/output (timer RG) 101: FTIOD0 input/output (timer RD_0) (initial value) 110: TRAO output (timer RA) 111: Setting prohibited	R/W
3	—	Reserved	This bit is always read as 0. The write value should always be 0.	—
2 to 0	P62MD[2:0]	P62 function select	000: Setting prohibited 001: $\overline{\text{IRQ2}}$ input 010: TXD output (SCI3_1) 011: FTIOC input/output (timer RC)* 100: TGIOA input/output (timer RG) 101: FTIOC0 input/output (timer RD_0) (initial value) 110: TRBO output (timer RB) 111: Setting prohibited	R/W

Note: * The timer RC is not available on the H8S/20203, H8S/20223, H8S/20215, and H8S/20235 Groups. These bits are reserved and the function cannot be selected for these groups.

(d) Port 9 Peripheral Function Mapping Register 4 (PMCR94)

Address: H'FF0063

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	—	P97MD[2:0]			—	P96MD[2:0]		
Value after reset:	0	1	0	1	0	1	0	1

Bit	Symbol	Bit Name	Description	R/W
7	—	Reserved	This bit is always read as 0. The write value should always be 0.	—
6 to 4	P97MD[2:0]	P97 function select	000: Setting prohibited 001: $\overline{\text{IRQ7}}$ input 010: Setting prohibited 011: TXD output (SCI3_1) 100: TREO output (timer RE) 101: FTIOD3 input/output (timer RD_1) (initial value) 110: TXD_3 output (SCI3_3) 111: Setting prohibited	R/W
3	—	Reserved	This bit is always read as 0. The write value should always be 0.	—
2 to 0	P96MD[2:0]	P96 function select	000: Setting prohibited 001: $\overline{\text{IRQ6}}$ input 010: Setting prohibited 011: RXD input (SCI3_1) 100: TRBO output (timer RB) 101: FTIOC3 input/output (timer RD_1) (initial value) 110: RXD_3 input (SCI3_3) 111: Setting prohibited	R/W

Note: PMCR94 is not available on the H8S/20103 and H8S/20115 Groups.

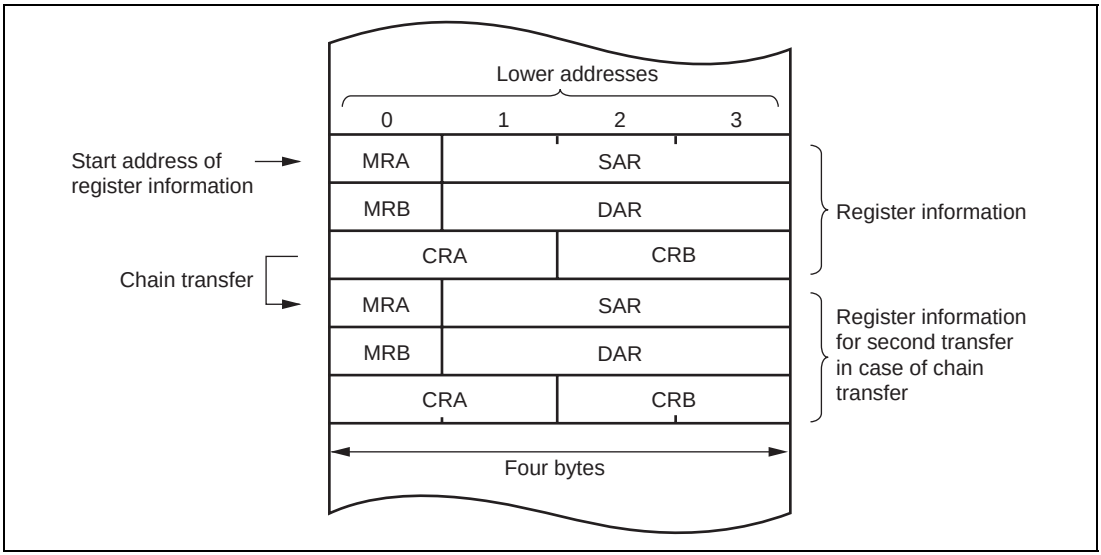


Figure 11.3 Locating DTC Register Information in Address Space

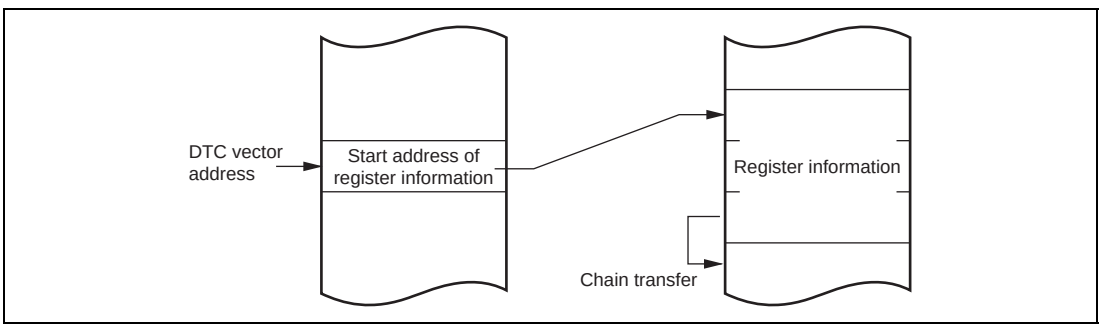


Figure 11.4 Correspondence between DTC Vector Address and Register Information

Table 14.1 shows the timer RB input/output pins.

Table 14.1 Pin Configuration

Name	I/O	Function
TRGB	Input	External trigger input
TRBO	Output	Successive pulse output or one-shot pulse output

14.2 Register Descriptions

The timer RB has the following registers:

- Timer RB control register (TRBCR)
- Timer RB one-shot control register (TRBOCR)
- Timer RB I/O control register (TRBIOC)
- Timer RB mode register (TRBMR)
- Timer RB interrupt request status register (TRBIR)
- Timer RB prescaler register (TRBPRE)
- Timer RB secondary register (TRBSC)
- Timer RB primary register (TRBPR)

15.2.10 Timer RC A/D Conversion Start Trigger Control Register (TRCADCR)

Address: H'FFFF93

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	ADTRGAE	ADTRGBE	ADTRGCE	ADTRGDE
Value after reset:	1	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7 to 4	—	Reserved	These bits are read as 1. The write value should be 1.	—
3	ADTRGAE	A/D conversion start trigger A enable	0: A/D conversion start trigger is not generated by compare match of GRA 1: A/D conversion start trigger is generated by compare match of GRA	R/W
2	ADTRGBE	A/D conversion start trigger B enable	0: A/D conversion start trigger is not generated by compare match of GRB 1: A/D conversion start trigger is generated by compare match of GRB	R/W
1	ADTRGCE	A/D conversion start trigger C enable	0: A/D conversion start trigger is not generated by compare match of GRC 1: A/D conversion start trigger is generated by compare match of GRC	R/W
0	ADTRGDE	A/D conversion start trigger D enable	0: A/D conversion start trigger is not generated by compare match of GRD 1: A/D conversion start trigger is generated by compare match of GRD	R/W

TRCADCR selects the trigger source to start A/D conversion. A/D conversion start trigger is generated by a corresponding compare match.

Figures 16.38 and 16.39 show examples of stopping operation of the counter in PWM3 mode, when the CCLR2 to CCLR0 bits in TRDCR are set to clear TRDCNT_0 on GRA_0 compare match. For details on PWM3 mode, see section 16.3.8, PWM3 Mode Operation.

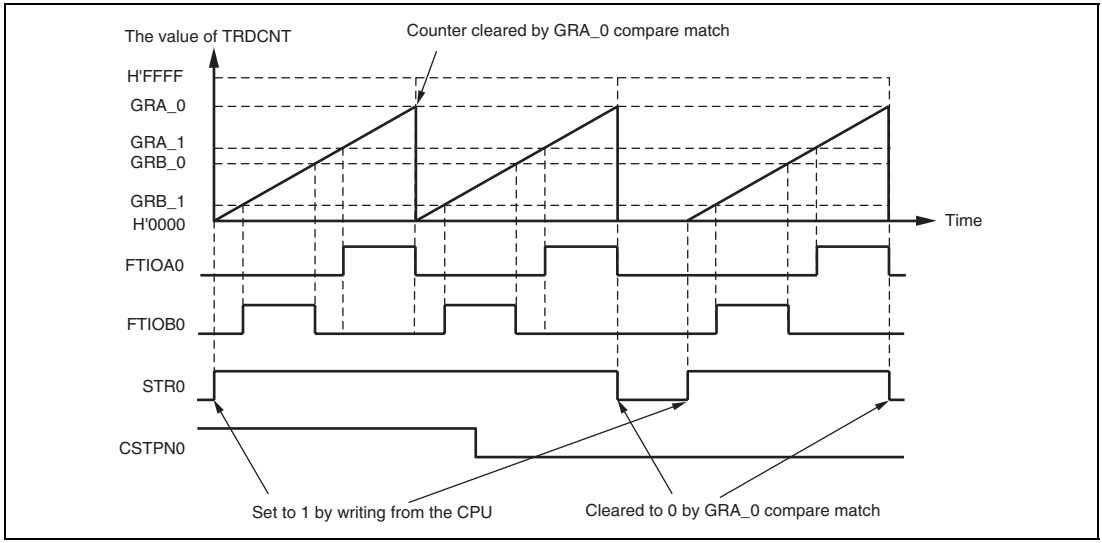


Figure 16.38 Example (1) of Stopping Operation of the Counter (in PWM3 Mode)

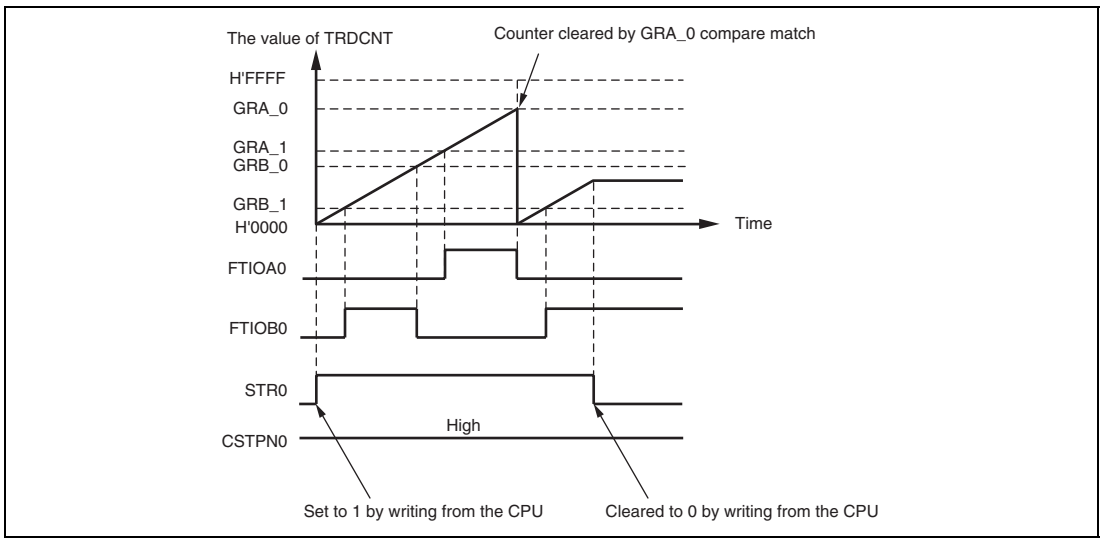


Figure 16.39 Example (2) of Stopping Operation of the Counter (in PWM3 Mode)

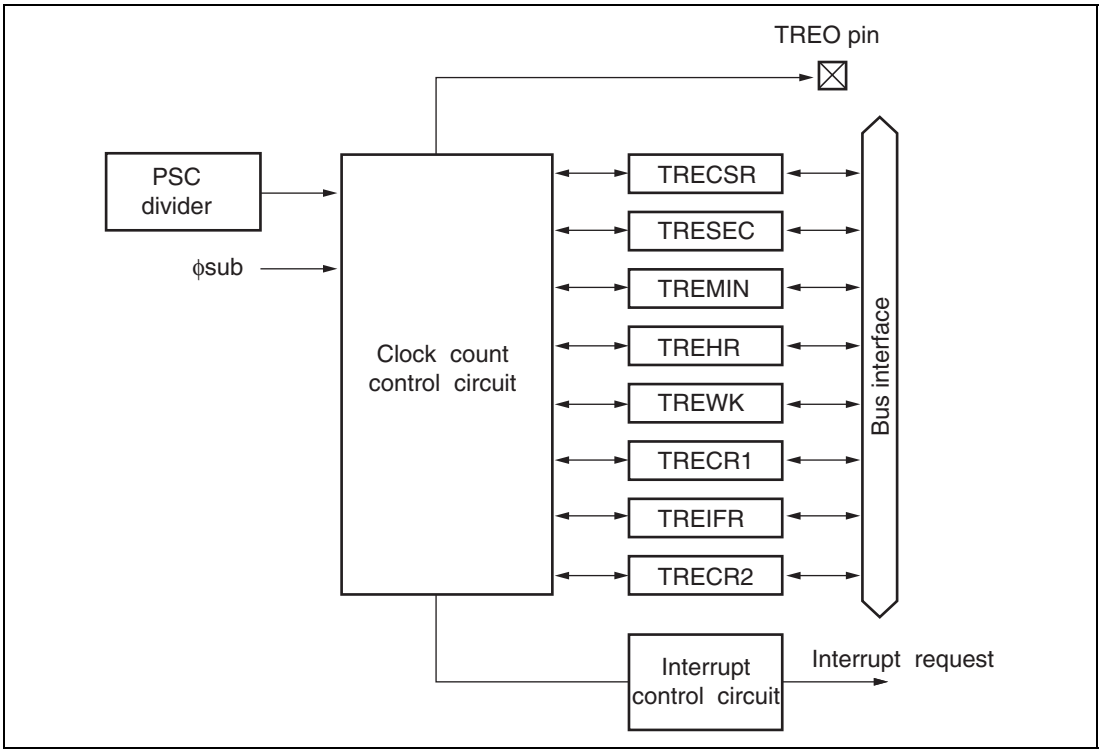


Figure 17.1 Block Diagram of Timer RE

Table 17.1 shows the timer RE input/output pin.

Table 17.1 Pin Configuration

Pin Name	I/O	Function
TREO	Output	Clock or compare-match output

Section 18 Timer RG

Timer RG is a 16-bit timer with output compare and input capture functions. Timer RG can count using a number of internal or external clocks and output pulses with a desired duty cycle using the compare match function between the timer counter and two general registers. Timer RG is also able to decode the phase difference between two external clocks and increment. Timer RG therefore provides an ideal solution for many systems with a requirement to decide position based on a rotary encoder or tachometer as well as a wide range of other applications.

18.1 Features

- Selection of six counter clock sources
  Internal clocks: ϕ, $\phi/2$, $\phi/4$, $\phi/8$, and $\phi/32$
  External clocks: TCLKA, TCLKB
- Timer mode
  Waveform output by compare match (Selection of 0 output, 1 output, or toggle output)
  Input capture function (Rising edge, falling edge, or both edges)
- PWM mode
  Generates pulses with a desired period and duty cycle.
- Phase counting mode
  Detects phase difference between two external clock inputs and increments/decrements the TCNT.
- Fast access via internal 16-bit bus
  Performs high-speed accesses to the timer counter and general registers using the 16-bit bus interface.
- Four interrupt sources
  TRGCNT overflow, TRGCNT underflow, compare match, and input capture

18.3.6 Digital Filtering Function for Input Capture Inputs

Input signals on the TGIOA and TGIOB pins can be input via the digital filters. The digital filter includes three latches connected in series and a matching detecting circuit. The input signals on the TGIOA and TGIOB pins are operated on the sampling clock specified by the DFCK1 and DFCK0 bits in TRGMDR. When outputs of the three latches match, the matching detecting circuit outputs the signal level of the input. Otherwise, the output remains unchanged. That is, when a pulse width is equal to or greater than three sampling clock cycles, the pulse is input as a signal. When a pulse width is less than three sampling clock cycles, the pulse is considered as a noise to be removed.

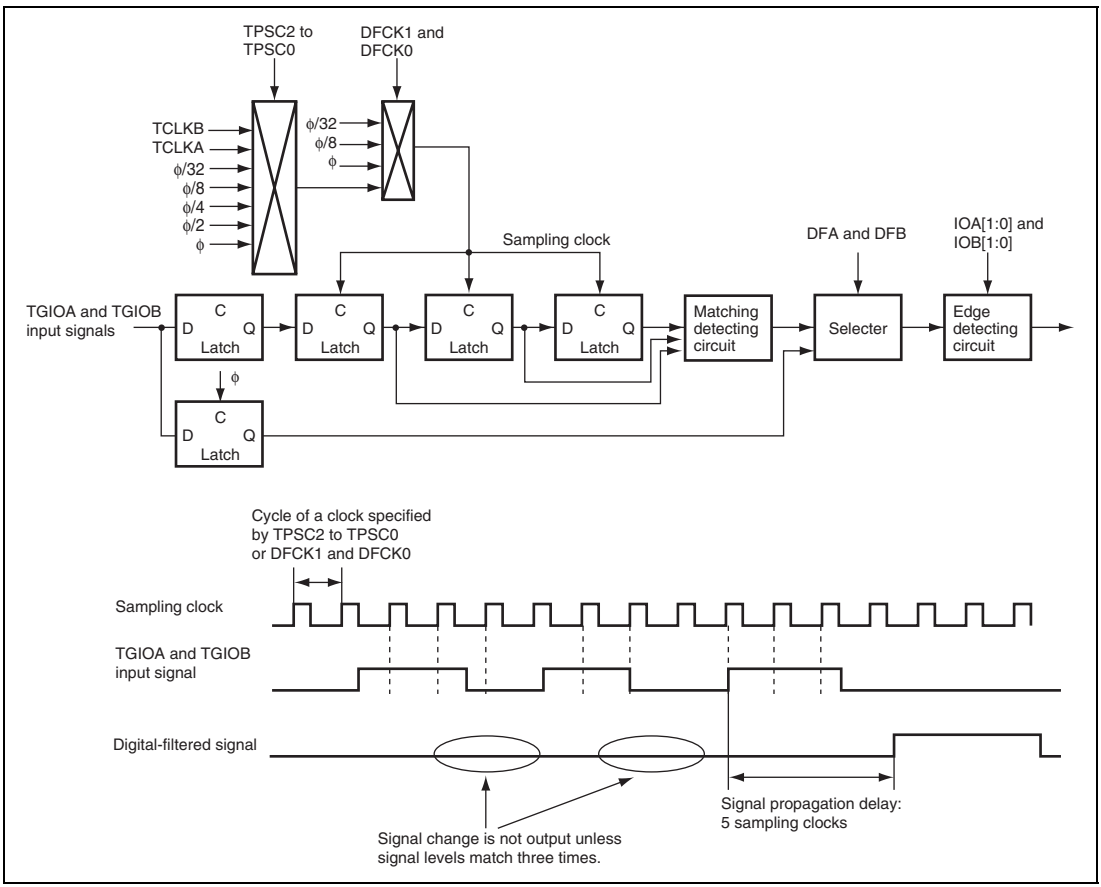


Figure 18.22 Block Diagram of Digital Filter

Section 23 Hardware LIN

The hardware LIN works in cooperation with timer RA and SCI3_1 to provide LIN communications.

23.1 Overview

- Master mode
  Generates Sync Break.
  Detects bus conflicts.
- Slave mode
  Detects Sync Break.
  Measures Sync Field.
  Controls Sync Break and Sync Field signal inputs to SCI3_1.
  Detects bus conflicts.

Figure 23.1 shows a block diagram of the hardware LIN interface.

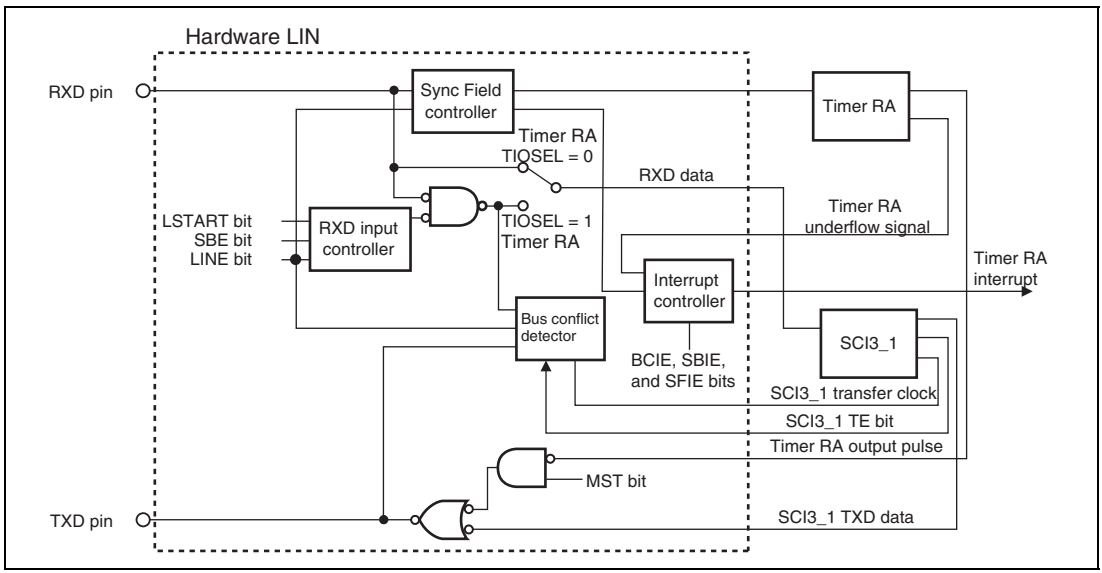
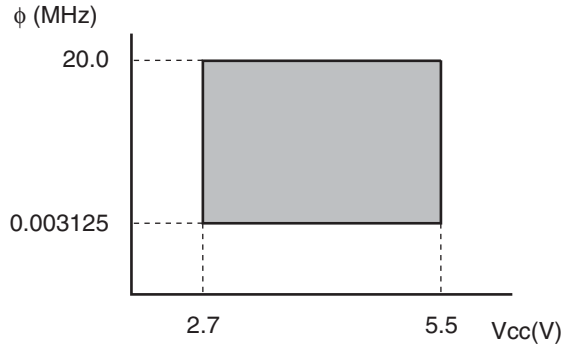
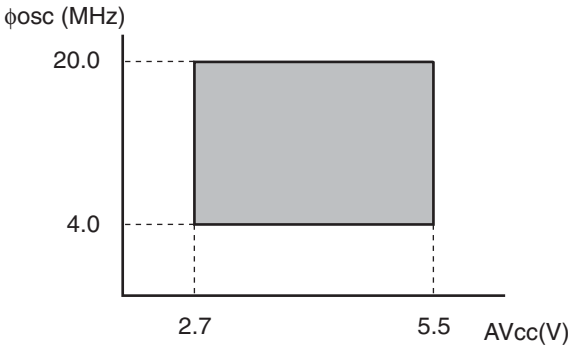


Figure 23.1 Block Diagram of Hardware LIN

(2) Power Supply Voltage and Operating Frequency Range



(3) Accuracy Guarantee Range of Analog Power Supply Voltage and A/D Converter



Mode	$\overline{RES}$ Pin	Internal State	PSCSTP	Other Pins	Oscillator Pins
Active mode 1	V_{CC}	Operating ($\phi = \phi_{OSC}$)	0	V_{CC}	Main clock oscillator: Ceramic resonator or crystal resonator Subclock oscillator: Pin X1 = V_{SS}
Active mode 2		Operating ($\phi = \phi_{OSC}/64$)	0		
Active mode 3		Operating ($\phi = \phi_{OSC}/128$)	0		
Sleep mode 1	V_{CC}	Only timers operating	0	V_{CC}	
Sleep mode 2		Only timers operating ($\phi = \phi_{OSC}/64$)	0		
Sleep mode 3		Only timers operating ($\phi = \phi_{OSC}/128$)	0		
Active mode 4	V_{CC}	Operating ($\phi = \phi_{sub}$)	1	V_{CC}	Main clock oscillator: Ceramic resonator or crystal resonator Subclock oscillator: Crystal resonator
Active mode 5		Operating ($\phi = \phi_{sub}/8$)	1		
Sleep mode 4	V_{CC}	Only timers operating ($\phi = \phi_{sub}$)	1	V_{CC}	
Sleep mode 5		Only timers operating ($\phi = \phi_{sub}/8$)	1		
Standby mode	V_{CC}	CPU and timers both stop.	—	V_{CC}	Main clock oscillator: Ceramic resonator or crystal resonator Subclock oscillator: Pin X1 = V_{SS}

Table 28.6 Timing of Serial Communication Interface (SCI)

V_{CC} = 2.7 to 5.5 V, V_{SS} = 0.0 V, Ta = –20 to +85 °C (N version)/ –40 to +85 °C (D version), unless otherwise indicated.

Item		Symbol	Applicable Pins	Test Conditions	Values				Reference Figure
					Min.	Typ.	Max.	Unit	
Input clock cycle	Asynchronous	t_{Scyc}	SCK3		4	—	—	t_{cyc}	Figure 28.6
	Clocked synchronous				6	—	—	t_{cyc}	
Input clock pulse width		t_{SCKW}	SCK3		0.4	—	0.6	t_{Scyc}	
Transmit data delay time (clocked synchronous)		t_{TXD}	TXD		—	—	1	t_{cyc}	Figure 28.7
Receive data setup time (clocked synchronous)		t_{RXS}	RXD		50.0	—	—	ns	
Receive data hold time (clocked synchronous)		t_{RXH}	RXD		50.0	—	—	ns	