Renesas Electronics America Inc - R4F20202DFD#U0 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IrDA, LINbus, SCI, SSU, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f20202dfd-u0

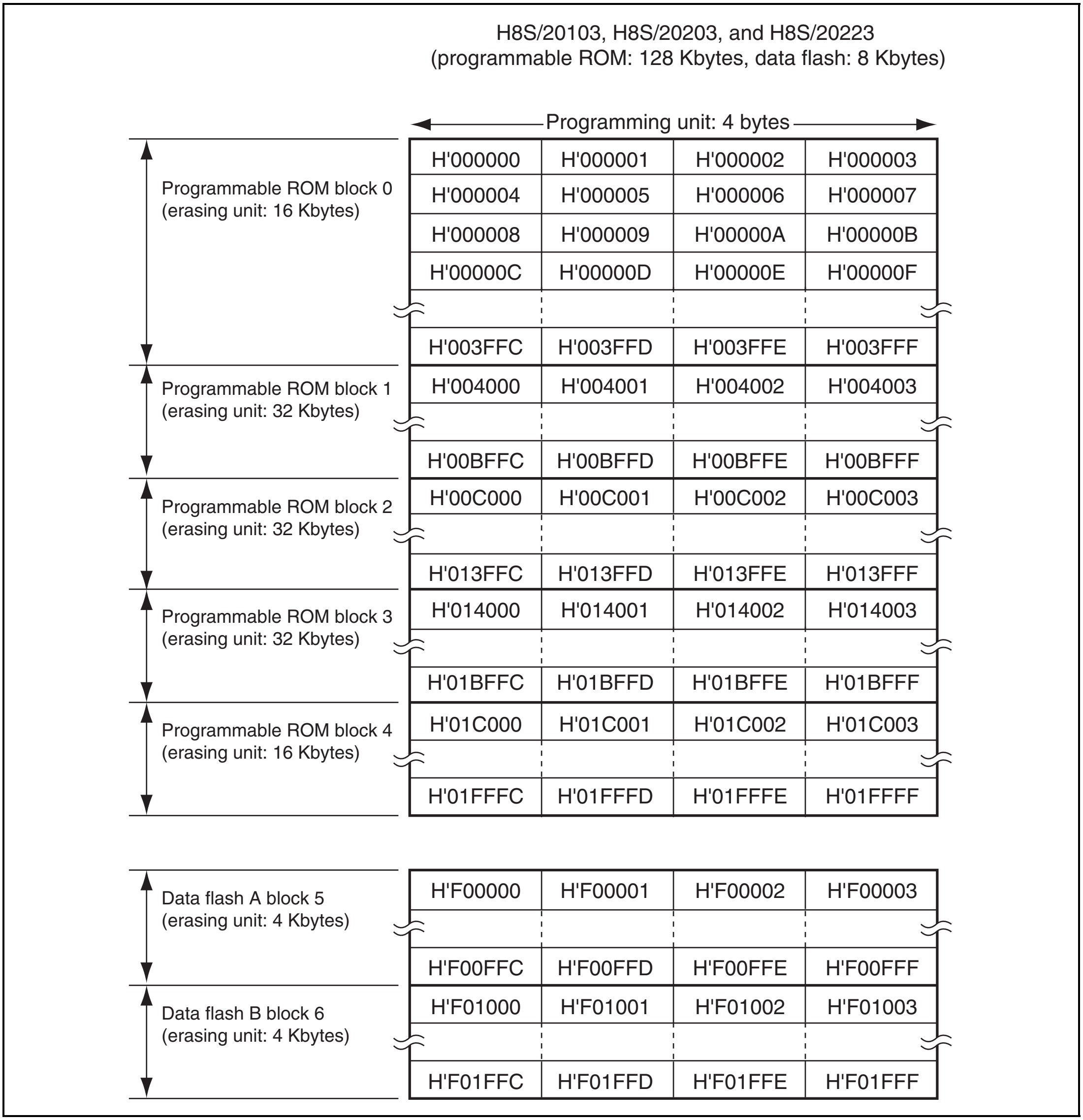


Figure 7.1 Block Configuration of Flash Memory (1)

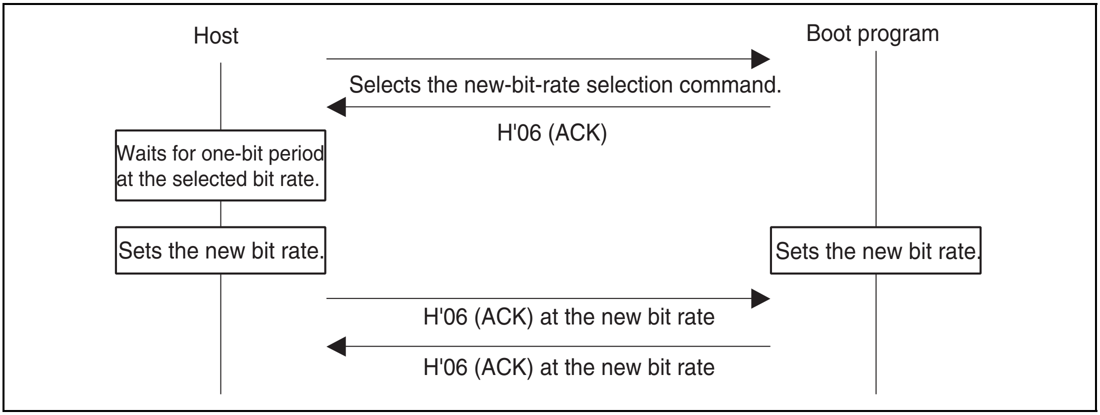


Figure 7.9 Sequence of New Bit-Rate Selection

(5) Programming/Erasure State Transition (Without ID Checking)

In response to a programming/erasure state transition command, the boot program transfers the erasure program to erase the data in the user ROM area. On completion of this erasure, the boot program returns the ACK code and enters the programming/erasure state.

Before transmitting the programming selection command and data for programming, the host should select the device, clock mode, and new bit rate for this LSI using the device selection, clock-mode selection, and new-bit-rate selection commands; and then transmit a programming/erasure state transition command to the boot program.

Command	H'40

- Command H'40 (1 byte): Programming/erasure state transition

Response	H'06

- Response H'06 (1 byte): Response to the programming/erasure state transition command (without ID checking)

  The ACK code is returned when the user ROM area have been successfully erased after transfer of the erasure program.

Error response

H'C0	H'51

(6) Read-Array Command

A read-array command is to cause a transition to a mode in which data can be read from flash memory.

When H'FF is written in the first command cycle, a transition to read array mode is caused. When the specified addresses are read out in the subsequent command cycles, data is read from the specified addresses.

Since read-array mode is retained until any other command is written, multiple addresses can be read successively.

(7) Lock-Bit Reading Command

This command is used to read the value of the lock bit in flash memory.

Writing H'71 in the first command cycle and reading from the specifying block address (BA) in the second command cycle returns the value of the lock bit. If a word instruction is used for reading, the value of the lock bit will be reflected in bits 6 and 14 of the read-out word. If a byte instruction is used, the value of the lock bit will be reflected in bit 6. Execute the lock-bit reading command in EW0 mode.

(8) Status Clearing Command

A clear-status command is used to clear the status flag to 0.

When H'50 is written in the first command cycle, the FMPRSF and FMEBSF bits in FLMSTR are cleared to 0.

(9) Full Status Checking

When any command (other than the read-array command, lock bit reading command and clear-status command) is issued, full-status checking is performed to confirm whether or not there was an error.

When an error occurs, the FMPRSF and FMEBSF bits in FLMSTR are set to 1, indicating the occurrence of the relevant errors.

Table 7.12 shows the bit values in FLMSTR and the corresponding errors. Figure 7.19 shows the full status checking flowchart and procedures of handling each error.

(c) Port 5 Peripheral Function Mapping Register 3 (PMCR53)

Address: H'FF0052

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	—	P55MD[2:0]			—	P54MD[2:0]		
Value after reset:	0	1	0	0	0	1	0	0

Bit	Symbol	Bit Name	Description	R/W
7	—	Reserved	This bit is always read as 0. The write value should always be 0.	—
6 to 4	P55MD[2:0]	P55 function select	000: Setting prohibited 001: $\overline{\text{IRQ5}}$ input 010: SCK3_2 input/output (SCI3_2) 011: SCK3_3 input/output (SCI3_3) 100: SSCK input/output*3 (SSU) (initial value) 101: FTIOB1 input/output (timer RD_0) 110: $\overline{\text{TRDOI\_1}}$ input/output (timer RD_1)*2 111: Setting prohibited	R/W
3	—	Reserved	This bit is always read as 0. The write value should always be 0.	—
2 to 0	P54MD[2:0]	P54 function select	000: Setting prohibited 001: $\overline{\text{IRQ4}}$ input 010: $\overline{\text{TRDOI\_0}}$ input (timer RD_0) 011: FTCI input (timer RC)*1 100: SSO input/output*3 (SSU) (initial value) 101: FTIOA1 input/output (timer RD_0) 110: TRAIO input/output (timer RA) 111: Setting prohibited	R/W

Notes: 1. The timer RC is not available on the H8S/20203, H8S/20223, H8S/20215, and H8S/20235 Groups. These bits are reserved and the function cannot be selected for these groups.

2. This function cannot be selected for the H8S/20103 and H8S/20115 Groups.

3. If the NMOS open-drain output is selected for the SSCK output pin or the SSO output pin, use the PMC to allocate that pin from port 5.

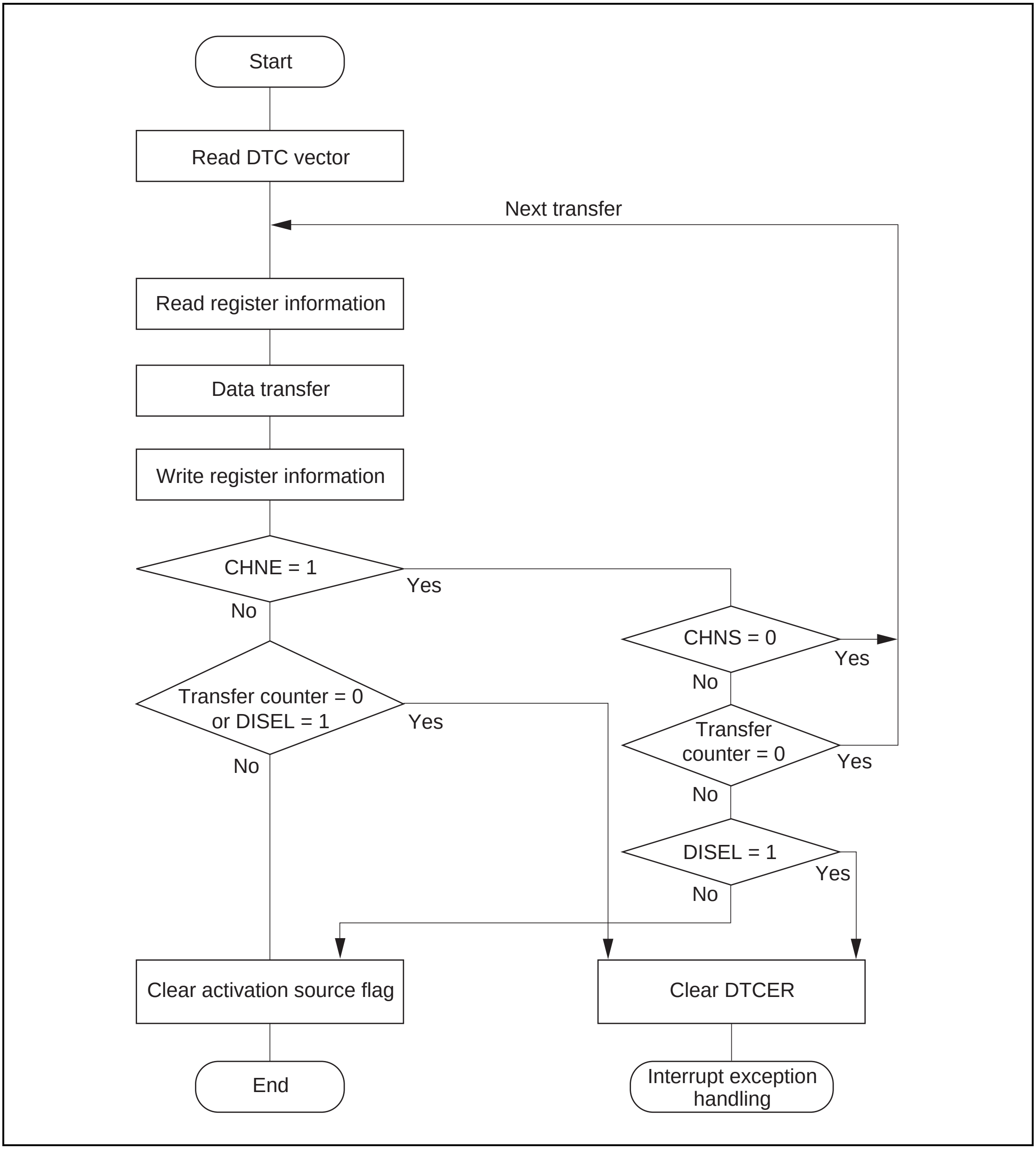


Figure 11.5 Flowchart of DTC Operation

15.2.10 Timer RC A/D Conversion Start Trigger Control Register (TRCADCR)

Address: H'FFFF93

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	ADTRGAE	ADTRGBE	ADTRGCE	ADTRGDE
Value after reset:	1	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7 to 4	—	Reserved	These bits are read as 1. The write value should be 1.	—
3	ADTRGAE	A/D conversion start trigger A enable	0: A/D conversion start trigger is not generated by compare match of GRA 1: A/D conversion start trigger is generated by compare match of GRA	R/W
2	ADTRGBE	A/D conversion start trigger B enable	0: A/D conversion start trigger is not generated by compare match of GRB 1: A/D conversion start trigger is generated by compare match of GRB	R/W
1	ADTRGCE	A/D conversion start trigger C enable	0: A/D conversion start trigger is not generated by compare match of GRC 1: A/D conversion start trigger is generated by compare match of GRC	R/W
0	ADTRGDE	A/D conversion start trigger D enable	0: A/D conversion start trigger is not generated by compare match of GRD 1: A/D conversion start trigger is generated by compare match of GRD	R/W

TRCADCR selects the trigger source to start A/D conversion. A/D conversion start trigger is generated by a corresponding compare match.

Table 15.9 A/D Conversion Start Trigger Generation in Each Operating Mode

		A/D Conversion Start Trigger Generation			
Operating Mode	**Buffer Operation**	**GRA**	**GRB**	**GRC**	**GRD**
Input capture	Enabled	×	×	×	×
	Disabled	×	×	×	×
Compare match	Enabled	O	O	×	×
	Disabled	O	O	O	O
PWM mode	Enabled	O	O	×	×
	Disabled	O	O	O	O
PWM2 mode	Enabled	O	O	O	×
	Disabled	O	O	O	O

[Legend]

O: The A/D conversion start trigger signal is generated.

×: The A/D conversion start trigger signal is not generated.

(2) Input Capture Signal Timing

Input capture on the rising edge, falling edge, or both edges can be selected through settings in TRDIOR. Figure 16.18 shows the timing when the rising edge is selected.

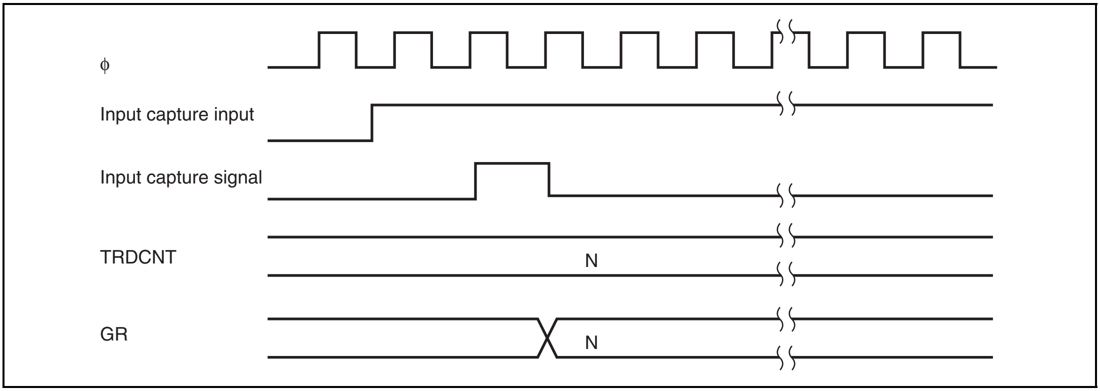


Figure 16.18 Input Capture Signal Timing

16.3.9 Buffer Operation

Buffer operation differs depending on whether GR has been designated for an input capture register or an output compare register, or in reset synchronous PWM mode or complementary PWM mode.

Table 16.10 shows the register combinations used in buffer operation.

Table 16.10 Register Combinations in Buffer Operation

General Register (GR)	Buffer Register
GRA	GRC
GRB	GRD

(1) When GR is an Output Compare Register

When a compare match occurs, the value in the buffer register of the corresponding channel is transferred to the general register.

This operation is illustrated in figure 16.41.

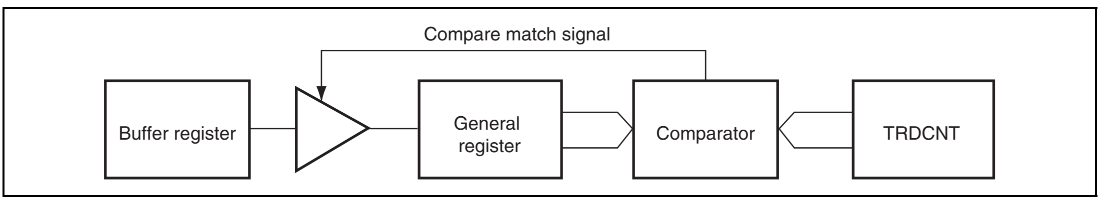


Figure 16.41 Compare Match Buffer Operation

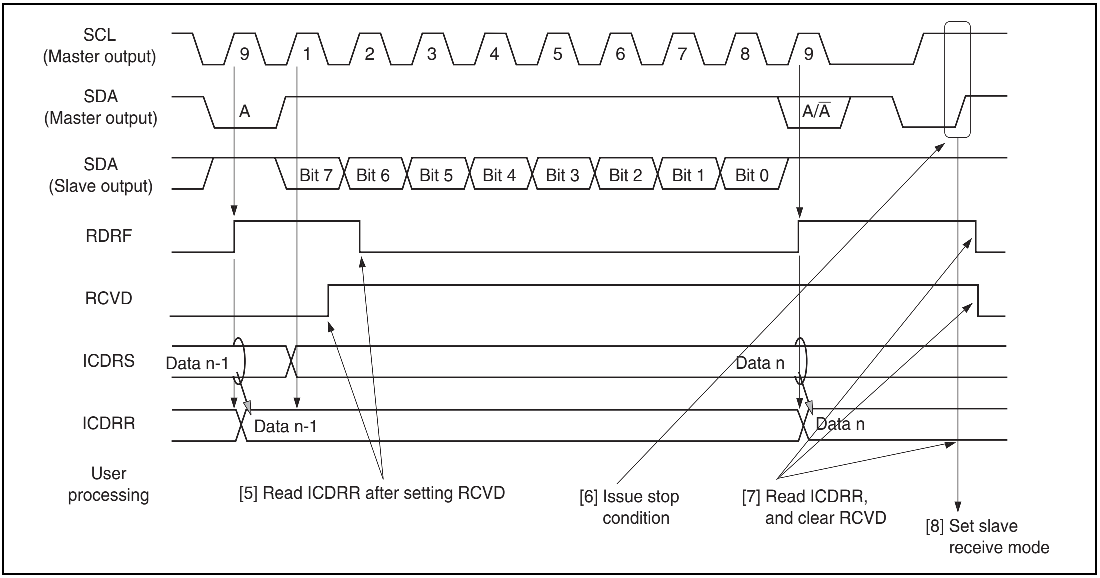


Figure 21.8 Master Receive Mode Operation Timing (2)

21.3.4 Slave Transmit Operation

In slave transmit mode, the slave device outputs the transmit data while the master device outputs the receive clock and returns an acknowledge signal. For slave transmit mode operation timing, see figures 21.9 and 21.10.

The transmission procedure and operations in slave transmit mode are described below.

1. Set the ICE bit in ICCR1 to 1. Set the MLS and WAIT bits in ICMR and the CKS3 to CKS0 bits in ICCR1 to 1 (Initial setting). Set the MST and TRS bits in ICCR1 to select slave receive mode, and wait until the slave address matches.
2. When the slave address matches in the first frame following detection of the start condition, the slave device outputs the level specified by ACKBT in ICIER to SDA at the rise of the 9th clock pulse. At this time, if the 8th bit data (R/$\overline{W}$) is 1, the TRS and ICSR bits in ICCR1 are set to 1, and the mode changes to slave transmit mode automatically. The continuous transmission is performed by writing transmit data to ICDRT every time TDRE is set.
3. If TDRE is set after writing last transmit data to ICDRT, wait until TEND in ICSR is set to 1, with TDRE = 1. When TEND is set, clear TEND.
4. Clear TRS for the end processing, and read ICDRR (dummy read). SCL is released.
5. Clear TDRE.

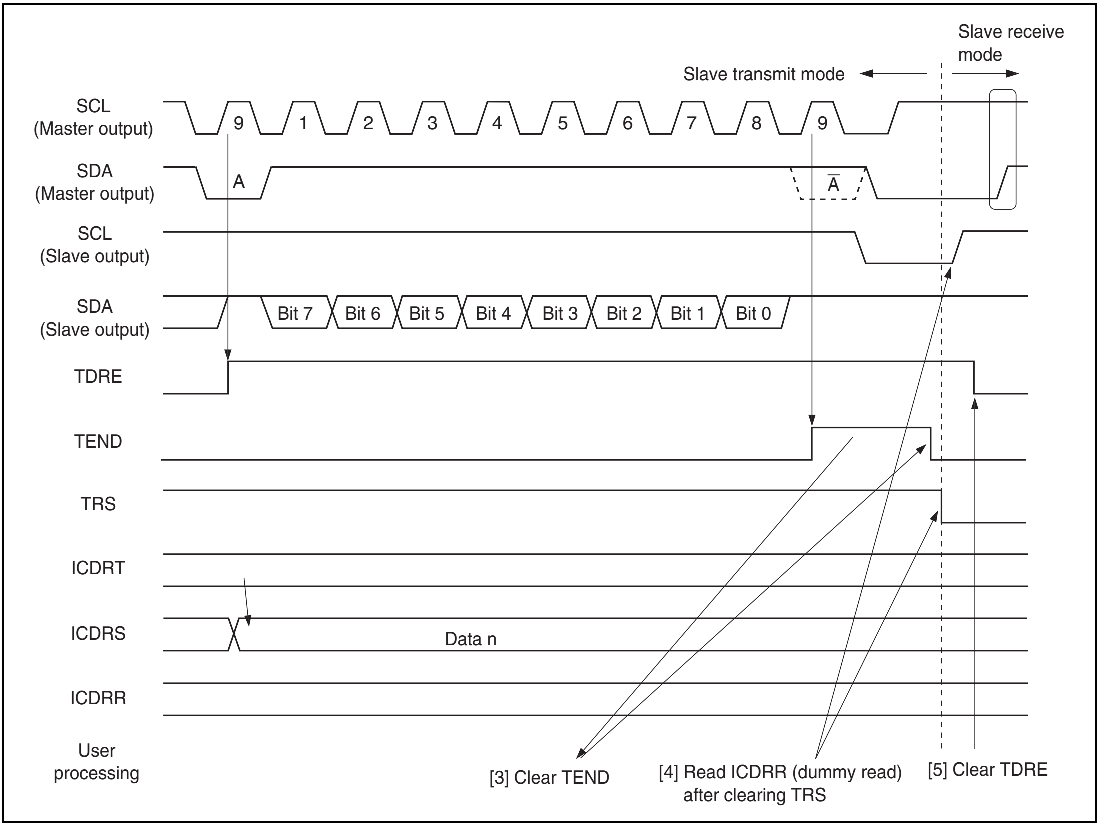


Figure 21.10 Slave Transmit Mode Operation Timing (2)

22.3.5 Operation in Clocked Synchronous Communication Mode

(1) Initialization in Clocked Synchronous Communication Mode

Figure 22.4 shows the initialization in clocked synchronous communication mode. Before transmitting and receiving data, the TE and RE bits in SSER should be cleared to 0, then the SSU should be initialized.

Note: When the operating mode, or transfer format, is changed for example, the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, the TDRE flag is set to 1. Note that clearing the RE bit to 0 does not change the contents of the RDRF and ORER flags, or the contents of SSRDR.

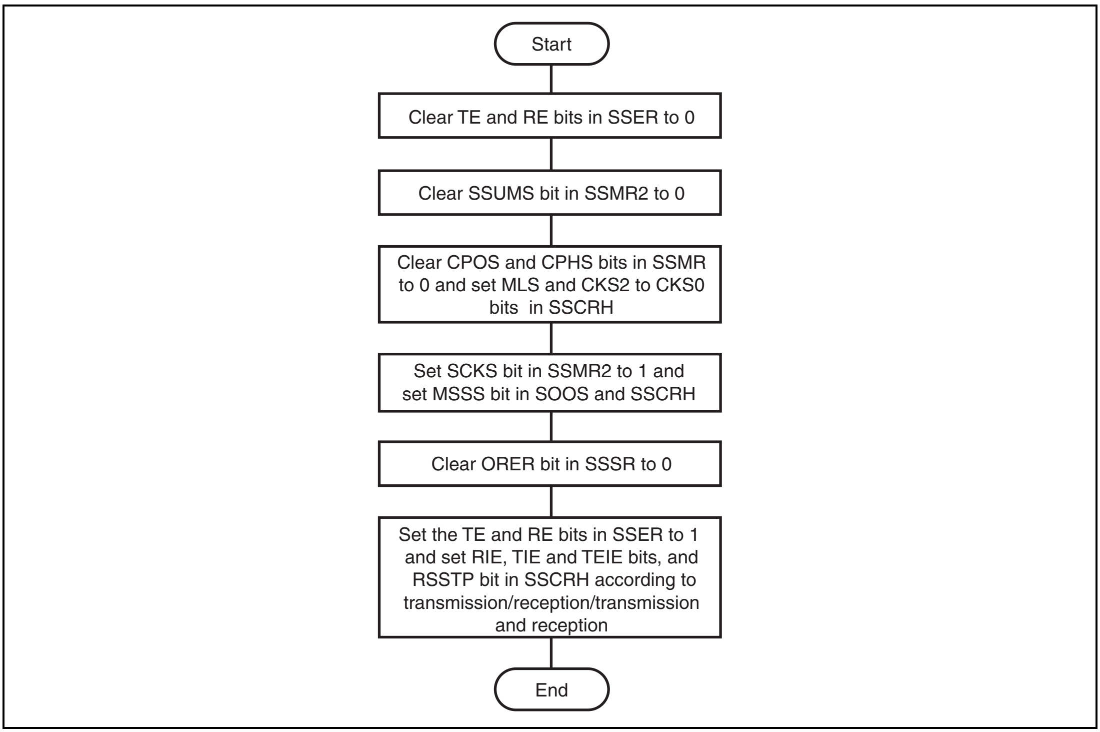


Figure 22.4 Initialization in Clocked Synchronous Communication Mode

Bit	Symbol	Bit Name	Description	R/W
1	ADSTCLR	ADST clear	If ADSTCLR is set to 1 in scan mode, the ADST bit is automatically cleared to 0 when A/D conversion of all the selected channels has been completed.	R/W
0	EXTRGS	External trigger select	EXTRGS combined with the TRGS1 and TRGS0 bits selects a trigger signal. For details, see the above description for the TRGS1 and TRGS0 bits.	R/W

[Legend]

x: Don't care.

Notes: 1. Selected only for the H8S/20223 and H8S/20235 Groups.
2. Selected only for the H8S/20103 and H8S/20115 Groups.
3. Not selected only for the H8S/20103 and H8S/20115 Groups.
4. Select these bits to fall the conversion time within the specified time.

- TRGS[1:0] bits (trigger select 1 and 0)

  These bits combined with the EXTRGS bit select enable or disable the A/D conversion start by a trigger signal.

- CKS[1:0] bits (clock select 1 to 0)

  These bits the A/D conversion time.

  The conversion time should be set while the A/D conversion is stopped (ADST = 0).

26.3.2 Low-Voltage Detection Circuit

(1) Low Voltage Detect Reset 2 (LVDR2)

LVDR2 is a reset generated by the LVD2 circuit. Figure 26.6 shows the operation timing of the LVDR2.

The LVD2 enters the module-standby state after release from a power-on reset. To operate the LVDR2, set the VD2E bit in LD2CRL to 1, wait for 50 µs ($t_{d(E-A)}$) until the detection voltage and the low-voltage detection circuit 2 operation have stabilized using a software timer, etc., then set the VD2MS and VD2RE bits in LD2CRH to 1. After that, the output settings of I/O ports must be made. To cancel the LVDR2, first the VD2RE bit in LD2CRH should be cleared to 0 and then the VD2E bit in LD2CRL should be cleared to 0. Figure 26.7 shows the procedure to set the LVDR2.

When the power-supply voltage falls below Vdet2, the LVDR2 clears the $\overline{\text{LVDRES2}}$ signal to 0, and resets the prescaler. The low-voltage detection reset state remains in place until a power-on reset is generated. When the power-supply voltage rises above the Vdet2 voltage again, the prescaler starts counting. It counts 32 φloco cycles, and then releases the internal reset signal.

Note that if the power supply voltage falls below $V_{LVD2min}$ = 2.7 V and then rises from that point, the LVDR2 may not occur. Such a case should be evaluated thoroughly.

If the power supply voltage falls below Vdet0, a power-on reset occurs.

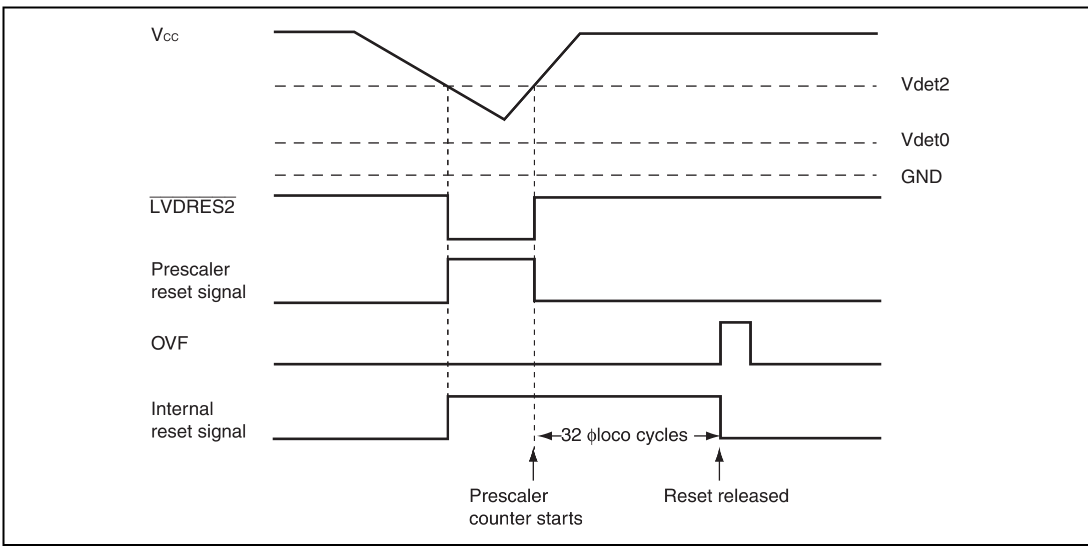
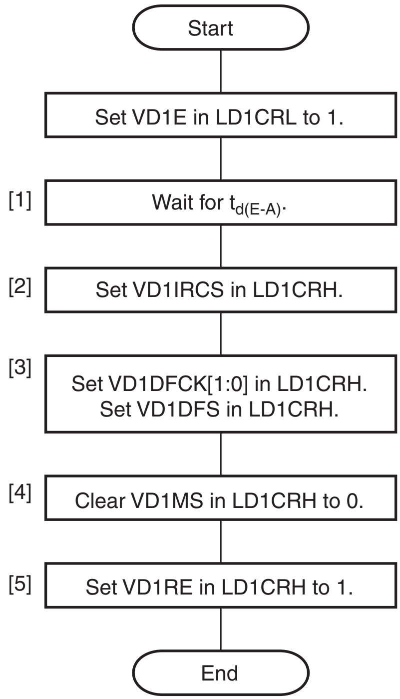


Figure 26.6 Operation Timing of LVDR2



[1] Set VD1E in LD1CRL to 1 to activate the LVD1 circuit and wait for the stabilization.

[2] Set interrupt request generation conditions when the digital filter is not used.

[3] Set the digital filter.

[4] Set the LVD1 circuit to generate interrupt requests.

[5] Enable the LVD1 circuit interrupt requests.

Figure 26.13 Procedure to Set LVDI1

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
CMPCSR	CMPF	CMPIE	CMPFC1	CMPFC0	—	—	—	—	A/D converter (unit 1)
ADDR2									
			—	—	—	—	—	—	
CMPVALH	—	—	—	—	—	—	VAL9	VAL8	
ADDR3									
			—	—	—	—	—	—	
CMPVALL	VAL7	VAL6	VAL5	VAL4	VAL3	VAL2	VAL1	VAL0	
ADDR4									
			—	—	—	—	—	—	
ADDR5									
			—	—	—	—	—	—	
ADDR6									
			—	—	—	—	—	—	
ADDR7									
			—	—	—	—	—	—	
ADCSR	ADF	ADIE	ADST	—	CH[3:0]				
ADCR	TRGS[1:0]		SCANE	SCANS	CKS[1:0]		ADSTCLR	EXTRGS	
ADMR	—	—	ADM1	—	—	—	—	—	
ADDR0_2*[6]									A/D converter (unit 2)*[6]
			—	—	—	—	—	—	
CMPR_2*[6]	—	—	—	—	CMP3	CMP2	CMP1	CMP0	
ADDR1_2*[6]									
			—	—	—	—	—	—	
CMPCSR_2*[6]	CMPF	CMPIE	CMPFC1	CMPFC0	—	—	—	—	
ADDR2_2*[6]									
			—	—	—	—	—	—	
CMPVALH_2*[6]	—	—	—	—	—	—	VAL9	VAL8	

Item	Page	Revision (See Manual for Details)
20.8 Interrupt Requests	724	Amended … When the RDRF flag in SSR is set to 1, a RXI interrupt request is generated. When any of the OER, PER and FER flags is set to 1, an ERI interrupt request is generated. The DTC can be activated to perform data transfers with the RXI interrupt request. The RDRF flag is automatically cleared to 0 by the DTC data transfer.
20.9 Usage Notes 20.9.6 Restrictions on Using DTC Figure 20.23 Example of DTC Transmission in Clock Synchronous Mode	727	Amended [Before amendment] SCK [After amendment] SCK3
Section 21 I^2C Bus Interface 2 (IIC2) 21.1 Features Table 21.1 Pin Configuration	731	Note added Note: When the IIC2 function is selected, use the PMC to allocate the SCL and SDA pin functions to P57 and P56, respectively.