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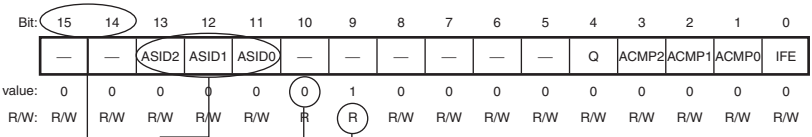
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IrDA, LINbus, SCI, SSU, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f20202nfd-u0

3. Description of Registers

Each register description includes a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meanings of the bit settings. The standard format and notation for bit charts and tables are described below.

[Bit Chart]



[Table of Bits]

(1) (2) (3) (4) (5)

Bit	Bit Name	Initial Value	R/W	Description
15	–	0	R	Reserved
14	–	0	R	These bits are always read as 0.
13 to 11	ASID2 to ASID0	All 0	R/W	Address Identifier These bits enable or disable the pin function.
10	–	0	R	Reserved This bit is always read as 0.
9	–	1	R	Reserved This bit is always read as 1.
	–	0		

Note: The bit names and sentences in the above figure are examples, and have nothing to do with the contents of this manual.

(1) Bit
Indicates the bit number or numbers.
In the case of a 32-bit register, the bits are arranged in order from 31 to 0. In the case of a 16-bit register, the bits are arranged in order from 15 to 0.

(2) Bit name
Indicates the name of the bit or bit field.
When the number of bits has to be clearly indicated in the field, appropriate notation is included (e.g., ASID[3:0]).
A reserved bit is indicated by "–".
Certain kinds of bits, such as those of timer counters, are not assigned bit names. In such cases, the entry under Bit Name is blank.

(3) Initial value
Indicates the value of each bit immediately after a power-on reset, i.e., the initial value.
0: The initial value is 0
1: The initial value is 1
–: The initial value is undefined

(4) R/W
For each bit and bit field, this entry indicates whether the bit or field is readable or writable, or both writing to and reading from the bit or field are impossible.
The notation is as follows:

R/W: The bit or field is readable and writable.
R/(W): The bit or field is readable and writable.
However, writing is only performed to flag clearing.
R: The bit or field is readable.
"R" is indicated for all reserved bits. When writing to the register, write the value under Initial Value in the bit chart to reserved bits or fields.
W: The bit or field is writable.

(5) Description
Describes the function of the bit or field and specifies the values for writing.

4. Description of Abbreviations

The abbreviations used in this manual are listed below.

- Abbreviations specific to this product

Abbreviation	Description
BSC	Bus controller
CPG	Clock pulse generator
INT	Interrupt controller
SCI3	Serial communications interface 3
PMC	Peripheral I/O mapping controller
WDT	Watchdog timer
DTC	Data transfer controller
ELC	Event link controller
IIC2	Inter IC bus interface 2
SSU	Synchronous serial communication unit
LVD	Low-voltage detection circuits

- Abbreviations other than those listed above

Abbreviation	Description
Bps	Bits per second
CRC	Cyclic redundancy check
DMA	Direct memory access
Hi-Z	High impedance
I/O	Input/output
IrDA	Infrared Data Association
LSB	Least significant bit
MSB	Most significant bit
NC	No connection
PLL	Phase-locked loop
PWM	Pulse width modulation
SFR	Special function register
UART	Universal asynchronous receiver/transmitter
VCO	Voltage-controlled oscillator

3.4 Trace Exception Handling

Traces are enabled in interrupt control mode 2. Trace mode is not activated in interrupt control mode 0, irrespective of the state of the T bit. For details on interrupt control modes, see section 4, Interrupt Controller.

If the T bit in EXR is set to 1, trace mode is activated. In trace mode, a trace exception occurs on completion of each instruction. Trace mode is not affected by the interrupt masking bit in CCR. Table 3.3 shows the state of CCR and EXR after execution of trace exception handling. Trace mode is canceled by clearing the T bit in EXR to 0. The T bit saved on the stack retains its value of 1, and trace mode resumes when control is returned from the trace exception handling routine by the RTE instruction. Trace exception handling is not carried out after execution of the RTE instruction.

Interrupts are accepted even within the trace exception handling routine.

Table 3.3 Status of CCR and EXR after Trace Exception Handling

	CCR			EXR
Interrupt Control Mode	**I**	**UI**	**I2 to I0**	**T**
0	Trace exception handling cannot be used.			
2	1	—	—	0

[Legend]

1: Set to 1

0: Cleared to 0

—: Retains value prior to execution.

4.4 Interrupt Exception Handling Vector Table

Table 4.3 shows interrupt exception handling sources, vector addresses, and interrupt priorities.

For default priorities, the lower the vector number, the higher the priority. When interrupt control mode 2 is set, priorities among modules can be changed by the IPR. Modules set at the same priority will conform to their default priorities. Priorities within a module are fixed.

5.5 Subclock Oscillator

Figure 5.16 shows a block diagram of the subclock oscillator.

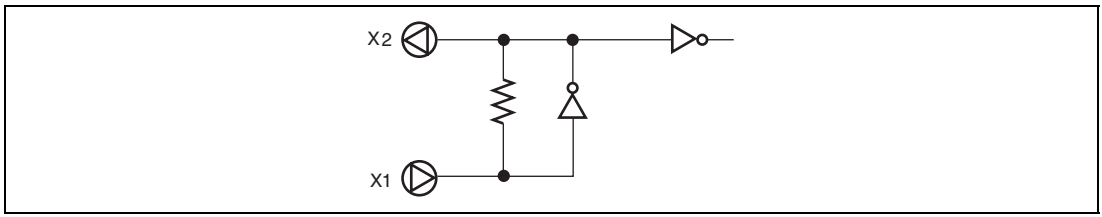


Figure 5.16 Block Diagram of Subclock Oscillator

5.5.1 Connecting 32.768-kHz Crystal Resonator

Clock pulses can be supplied to the subclock divider by connecting a 32.768-kHz crystal resonator, as shown in figure 5.17. A damping resistor Rd should be added, if necessary. Since the resistor values vary depending on the resonator, use values recommended by the resonator manufacturer.

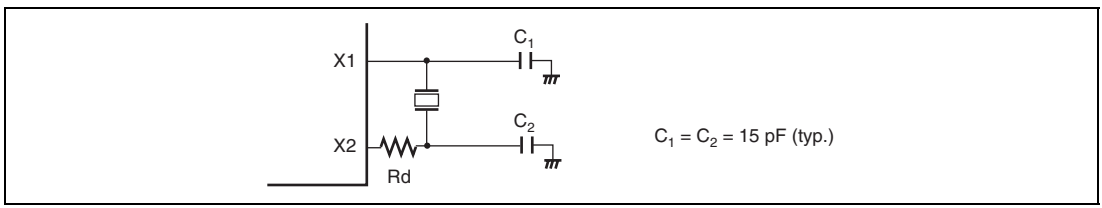


Figure 5.17 Typical Connection to 32.768-kHz Crystal Resonator

5.5.2 Pin Connection when not Using Subclock

When the subclock is not used, connect pin X1 to VSS and leave pin X2 open, as shown in figure 5.18.

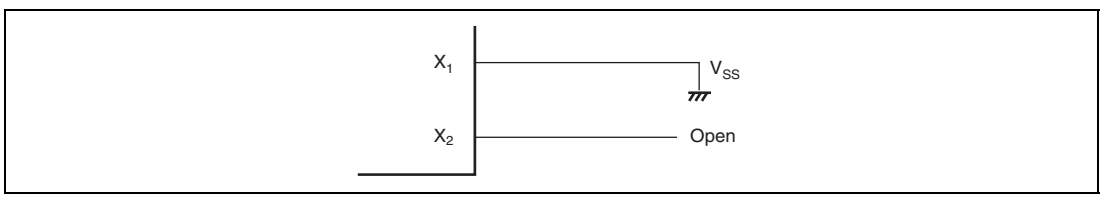


Figure 5.18 Pin Connection when not Using Subclock

10.3.1 Port Mode Register 3 (PMR3)

Address: H'FF0002

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	PMR37	PMR36	PMR35	PMR34	PMR33	PMR32	PMR31	PMR30
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7	PMR37	Port 37 mode	0: General I/O port 1: The function selected by the peripheral function mapping controller (PMC). PMR3 is a register that selects the function of the multiplexed pins: general I/O function or the function selected by the PMC.	R/W
6	PMR36	Port 36 mode		R/W
5	PMR35	Port 35 mode		R/W
4	PMR34	Port 34 mode		R/W
3	PMR33	Port 33 mode		R/W
2	PMR32	Port 32 mode		R/W
1	PMR31	Port 31 mode		R/W
0	PMR30	Port 30 mode		R/W

12.2.2 Event Link Setting Registers 0 to 32 (ELSR0 to ELSR32)

Address: H'FF0680 to H'FF0684, H'FF0688, H'FF068A to H'FF068C, H'FF068E, H'FF068F, H'FF0692, H'FF0693, H'FF0695 to H'FF0698, H'FF069D to H'FF06A0

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	ELSn7	ELSn6	ELSn5	ELSn4	ELSn3	ELSn2	ELSn1	ELSn0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7	ELSn7	Event link select n7	00000000: Linkage of the event is disabled. 0000001 to 01100001: Set the number specific to the event signal to be linked. Other than the above: Setting prohibited.	R/W
6	ELSn6	Event link select n6		R/W
5	ELSn5	Event link select n5		R/W
4	ELSn4	Event link select n4		R/W
3	ELSn3	Event link select n3		R/W
2	ELSn2	Event link select n2		R/W
1	ELSn1	Event link select n1		R/W
0	ELSn0	Event link select n0		R/W

[Legend]

n: 0 to 32 (except 5 to 7, 9, 13, 16, 17, 20, and 25 to 28)

Each of ELSR0 to ELSR32 specifies an event signal to be linked for the peripheral module. Table 12.1 shows the correspondence between ELSR0 to ELSR32 and the peripheral modules. Table 12.2 shows the correspondence between the event signal names and the numbers specific to the signals.

12.2.14 ELC Timer Counter (ELTMCNT)

Address: H'FF06C0

Bit:	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ELTMCNT is a 16-bit readable/writable up-counter. To select the input clock signal to be supplied to the counter, use the CLSRS[3:0] bits in ELTMCR. ELTMCNT cannot be accessed in 8-bit units; it must always be accessed in 16-bit units. The initial value of ELTMCNT is H'0000.

To set the event-generation interval to the time from starting of the timer to generation of the first event, set the counter to 0.

Figure 15.11 shows an example of buffer operation when the FTIOB pin is set to PWM mode and GRD is set as the buffer register for GRB. TRCCNT is cleared on compare match A, and the FTIOB pin outputs 1 on compare match B and 0 on compare match A.

Due to the buffer operation, the FTIOB output levels are changed and the value of buffer register GRD is transferred to GRB whenever compare match B occurs. This procedure is repeated every time compare match B occurs.

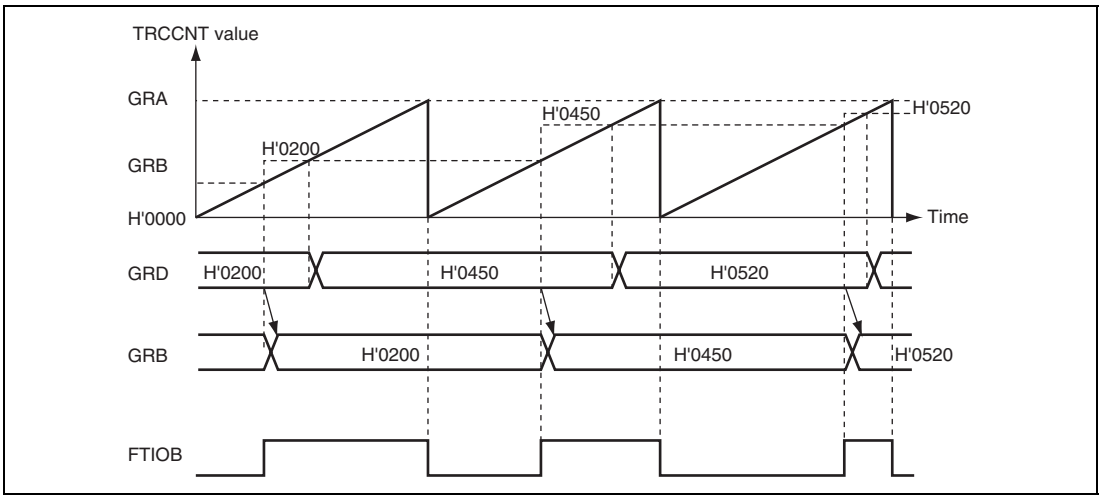
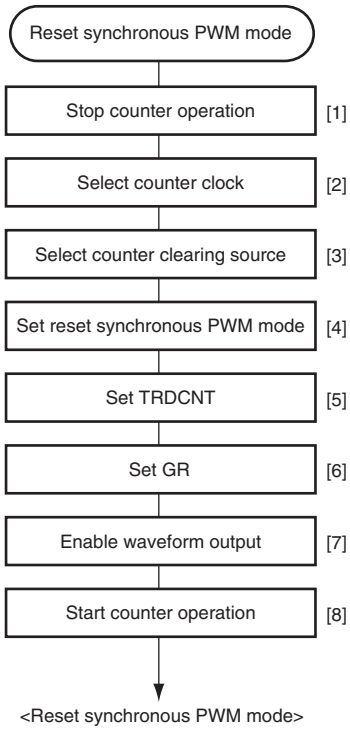


Figure 15.11 Buffer Operation Example (Output Compare)



[1] Clear bit STR0 in TRDSTR to 0 and stop the counter operation of TRDCNT_0. Set reset synchronous PWM mode after TRDCNT_0 stops.

[2] Select the counter clock with bits TPSC2 to TPSC0 in TRDCR. When an external clock is selected, select the external clock edge with bits CKEG1 and CKEG0 in TRDCR.

[3] Use bits CCLR2 to CCLR0 in TRDCR to select counter clearing source GRA_0.

[4] Select the reset synchronous PWM mode with bits CMD1 and CMD0 in TRDFCR. FTIOB0 to FTIOD0 and FTIOA1 to FTIOD1 become PWM output pins automatically.

[5] Set TRDCNT_0 as H'0000. TRDCNT_1 does not need to be set.

[6] GRA_0 is a cycle register. Set a cycle for GRA_0. Set the changing point timing of the PWM output waveform for GRB_0, GRA_1, and GRB_1.

[7] Enable or disable the timer output by TRDOER1.

[8] Set the STR bit in TRDSTR to 1 and start the counter operation.

Figure 16.26 Example of Reset Synchronous PWM Mode Setting Procedure

17.5 Interrupt Sources

There are six kinds of timer RE interrupts: week interrupts, day interrupts, hour interrupts, minute interrupts, and second interrupts in realtime clock mode, and compare-match interrupts in output compare mode. Table 17.2 shows the interrupt sources.

When using an interrupt, initiate the timer RE last after other registers are set. Independent vector addresses are allocated to each timer RE interrupt source.

Table 17.2 Interrupt Sources

Interrupt Name	Interrupt Source	Interrupt Enable Bit
Compare-match interrupt	Occurs when the count value matches the compare data.	COMIE
Week periodic interrupt	Occurs every week when the day-of-week data register value becomes 0.	WKIE
Day periodic interrupt	Occurs every day when the day-of-week data register value is incremented.	DYIE
Hour periodic interrupt	Occurs every hour when the hour date register value is incremented.	HRIE
Minute periodic interrupt	Occurs every minute when the minute data register value is incremented.	MNIE
Second periodic interrupt	Occurs every second when the second data register value is incremented.	SEIE

17.6 Usage Notes

(1) Starting and Stopping Counting Process

The timer RE includes a TSTART bit that directs the start or stop of the counting process, and a TCSTF bit that indicates that the counting process has started or stopped.

Setting the TSTART bit to 1 causes the timer RE to start counting and assigns 1 to the TCSTF bit. From the time the TSTART bit is set to 1 and to the time the TCSTF bit turns 1, a maximum of 2 cycles of count sources are required. During this time period, the timer RE related registers*, with the exception of the TCSTF bit, should not be accessed.

Similarly, clearing the TSTART bit to 0 causes the timer RE to stop counting, and assigns 0 to the TCSTF bit. From the time the TSTART bit is set to 0 and to the time the TCSTF bit turns 0, the timer RE related registers*, with the exception of the TCSTF bit, should not be accessed.

Note: Timer RE related registers: TRESEC, TREMIN, TREHR, TREWK, TRECR1, TRECR2, and TRECSR

(2) Register Settings of Timer RE

The following registers and bits should be written when the timer RE is stopped.

The condition "timer RE stopped" refers to the condition in which both the TSTART and TCSTF bits in TRECR1 are 0. Set TRECR2 at the end of setting the above registers and bits (before the timer RE counting process is started).

- Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2
- Bits H12_H24 bit, PM, and INT in TRECR1
- Bits RCS0 to RCS3 in TRECSR

(3) Sampling Circuit for Noise Canceler in ϕ Subclock Signal

When selecting the ϕsub as the clock source for the timer RE, always enable the sampling circuit with the SUBNC[1:0] bits in SYSCCR. For details of the SUBNC[1:0] bits, see section 5.2.2, System Clock Control Register (SYSCCR).

(4) Restrictions on Clock Selection in Output Compare Mode

In output compare mode, do not select the ϕsub clock as the clock source for the timer if the CPU is in ϕloco mode.

18.3.6 Digital Filtering Function for Input Capture Inputs

Input signals on the TGIOA and TGIOB pins can be input via the digital filters. The digital filter includes three latches connected in series and a matching detecting circuit. The input signals on the TGIOA and TGIOB pins are operated on the sampling clock specified by the DFCK1 and DFCK0 bits in TRGMDR. When outputs of the three latches match, the matching detecting circuit outputs the signal level of the input. Otherwise, the output remains unchanged. That is, when a pulse width is equal to or greater than three sampling clock cycles, the pulse is input as a signal. When a pulse width is less than three sampling clock cycles, the pulse is considered as a noise to be removed.

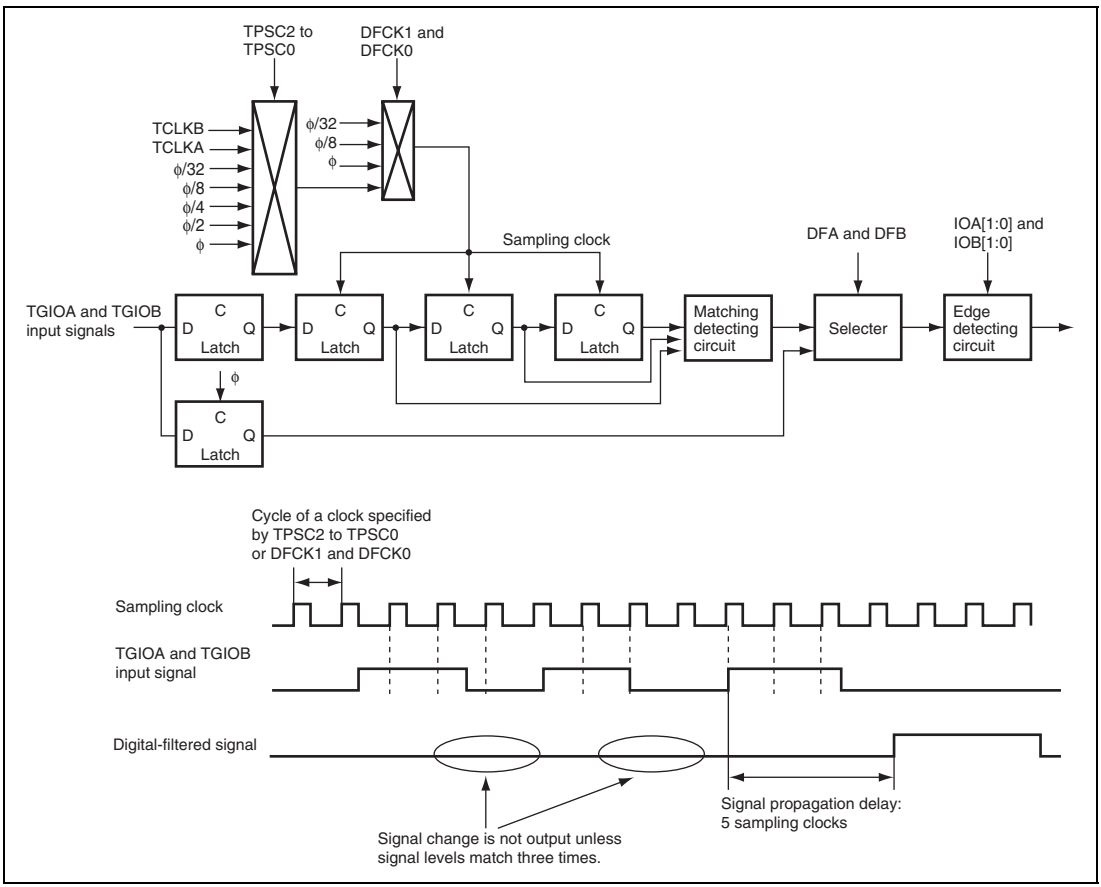


Figure 18.22 Block Diagram of Digital Filter

Section 20 Serial Communication Interface 3 (SCI3, IrDA)

This LSI includes a serial communication interface 3 (SCI3), which has three independent channels. The SCI3 can handle both asynchronous and clocked synchronous serial communication. In asynchronous mode, serial data communication can be carried out using standard asynchronous communication chips such as a Universal Asynchronous Receiver/Transmitter (UART) or an Asynchronous Communication Interface Adapter (ACIA). A function is also provided for serial communication between processors (multiprocessor communication function).

SCI3_2 provides IrDA (Infrared Data Association) communication waveform transmission/reception according IrDA standard version 1.0.

Table 20.1 shows the SCI3 channel configuration and figure 20.1 shows a block diagram of the SCI3. Since pin functions are identical for each of the three channels (SCI3, SCI3_2, and SCI3_3), separate explanations are not given in this section.

20.1 Features

- Choice of asynchronous or clocked synchronous serial communication mode
- Full-duplex communication capability

  The transmitter and receiver are mutually independent, enabling transmission and reception to be executed simultaneously.

  Double-buffering is used in both the transmitter and the receiver, enabling continuous transmission and continuous reception.
- On-chip baud rate generator allows any bit rate to be selected
- External clock or on-chip baud rate generator can be selected as a transfer clock source.
- Six interrupt sources

  Transmit-end, transmit-data-empty, receive-data-full, overrun error, framing error, and parity error. The DTC can be activated by the transmit-data-empty interrupt and receive-data-full interrupt sources.

Asynchronous mode

- Data length: 7 or 8 bits
- Stop bit length: 1 or 2 bits
- Parity: Even, odd, or none
- Receive error detection: Parity, overrun, and framing errors
- Break detection: Break can be detected by reading the RXD pin level directly in the case of a framing error

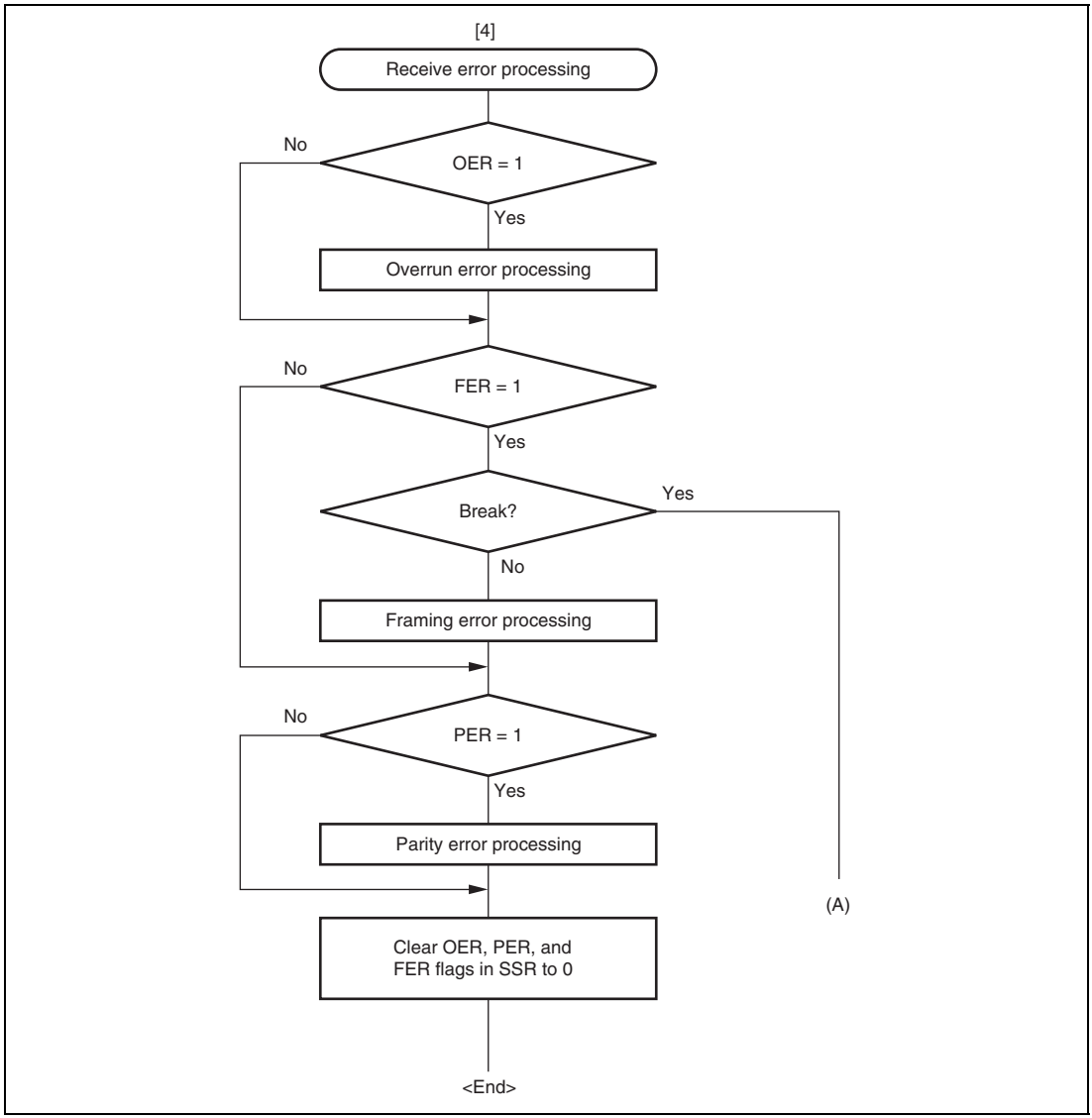


Figure 20.8 Sample Flowchart for Data Reception (Asynchronous Mode) (2)

(2) Serial Data Transmission

Figure 22.5 shows an example of the SSU operation for transmission. In serial transmission, the SSU operates as described below.

When the SSU is set as a master device, it outputs a synchronous clock and data. When the SSU is set as a slave device, it outputs data in synchronized with the input clock.

When the SSU writes transmit data in SSTDR after setting the TE bit to 1, the TDRE flag is automatically cleared to 0 and data is transferred from SSTDR to SSTRSR. Then the SSU sets the TDRE flag to 1 and starts transmission. If the TIE bit in SSER is set to 1 at this time, a TXI is generated.

When the TDRE flag is 0 and one frame of data has transferred, data is transferred from SSTDR to SSTRSR and serial transmission of the next frame is started. If the eighth bit is transmitted while the TDRE flag is 1, the TEND bit in SSSR is set to 1 and the state is retained. If the TEIE bit in SSER is set to 1 at this time, a TEI is generated. After transmission is ended, the SSCK pin is fixed high.

While the ORER bit in SSSR is set to 1, transmission cannot be performed. Therefore confirm that the ORER bit is cleared to 0 before transmission.

Figure 22.6 shows a sample flowchart for serial data transmission.

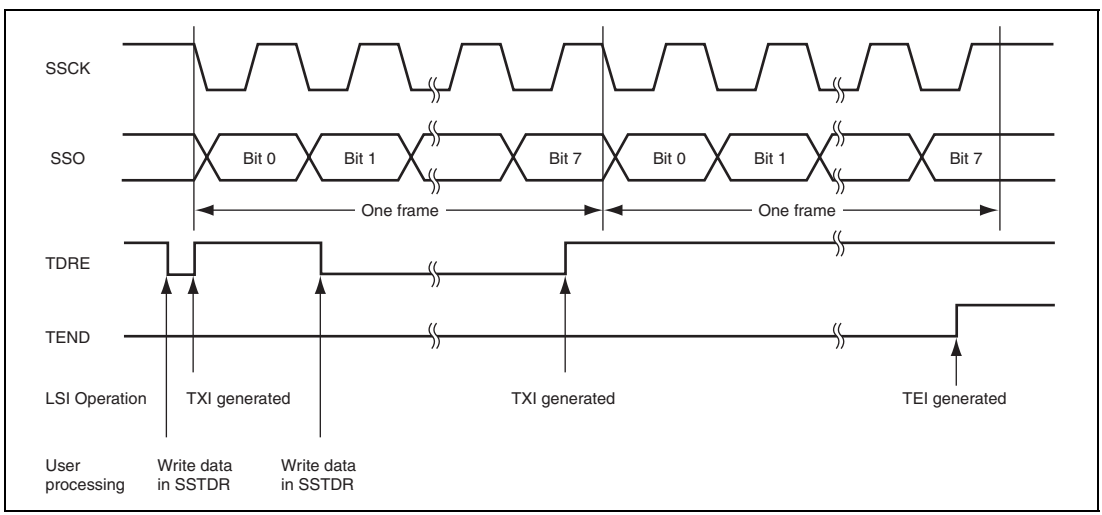


Figure 22.5 Example of Operation in Data Transmission

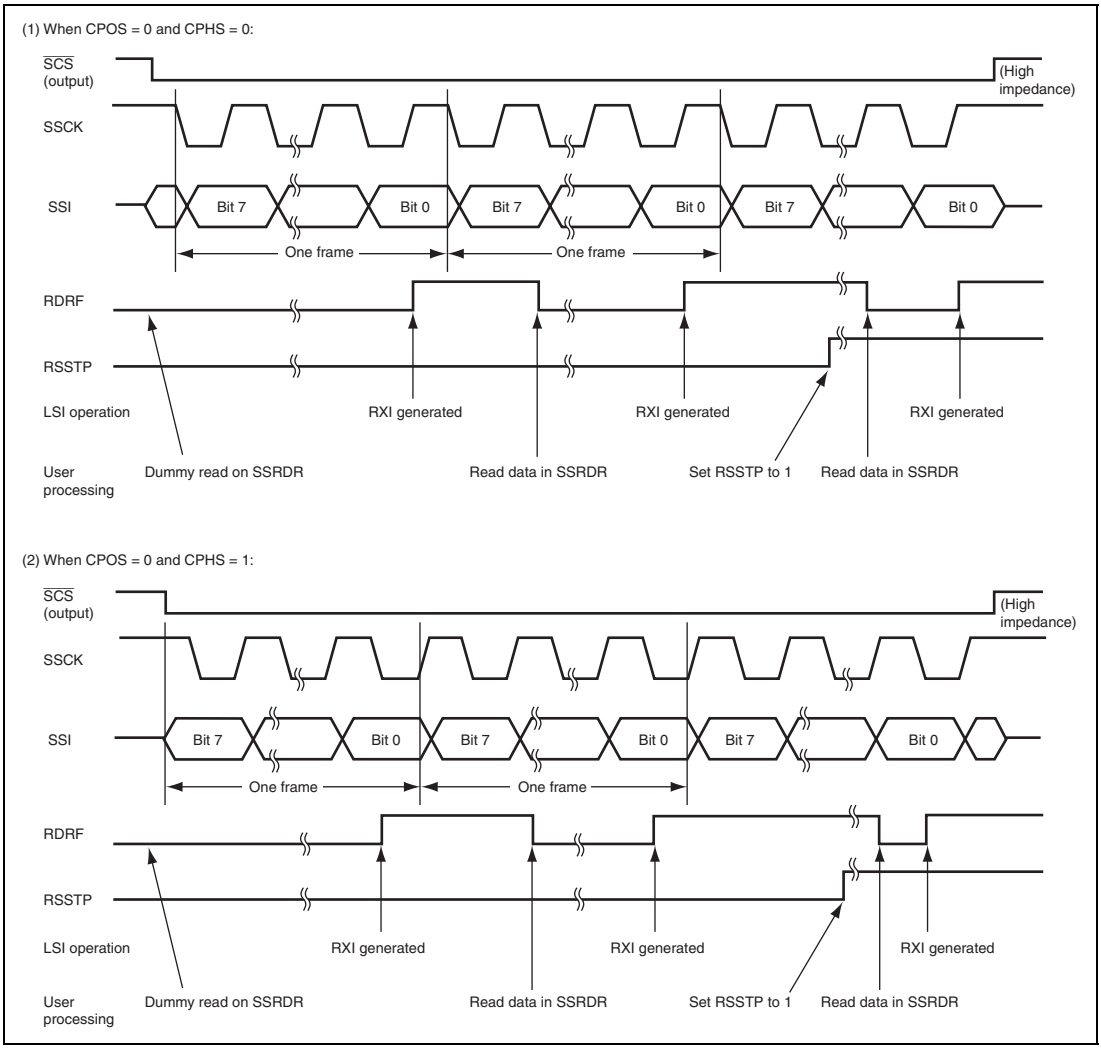


Figure 22.12 Example of Operation in Data Reception (MSS = 1)

24.2.7 Compare Voltage Registers H and L (CMPVALH and CMPVALL)

• CMPVALH

Address: H'FF05E4, H'FF0604

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	VAL9	VAL8
Value after reset:	0	0	0	0	0	0	0	0

• CMPVALL

Address: H'FF05E6, H'FF0606

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	VAL7	VAL6	VAL5	VAL4	VAL3	VAL2	VAL1	VAL0
Value after reset:	0	0	0	0	0	0	0	0

- CMPVALH

Bit	Symbol	Bit Name	Description	R/W
7 to 2	—	Reserved	This bit is read as 0. The write value should be 0.	—
1	VAL9	—	These bits set the compare voltage VAL[9:8].	R/W
0	VAL8	—		R/W

- CMPVALL

Bit	Symbol	Bit Name	Description	R/W
7	VAL7	—	These bits set the compare voltage VAL[7:0].	R/W
6	VAL6	—		R/W
5	VAL5	—		R/W
4	VAL4	—		R/W
3	VAL3	—		R/W
2	VAL2	—		R/W
1	VAL1	—		R/W
0	VAL0	—		R/W

26.2.6 Low-Voltage Detection Circuit 0 Control Register H (LD0CRH)

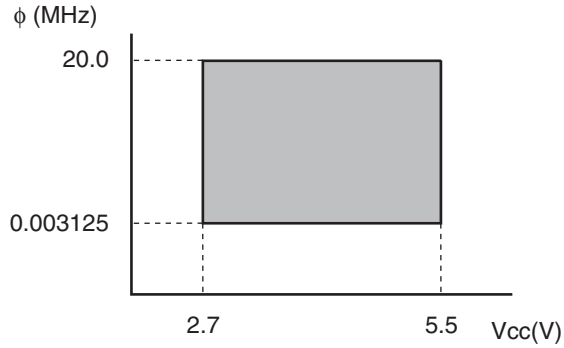
Address: H'FF0626

Bit:	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	VD0DFCK[1:0]		VD0DFS	—	—	—
Value after reset:	—	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
7	—	Reserved	This bit is read as undefined value. The write value should be 0.	—
6	—	Reserved	This bit is read as 0. The write value should be 0.	—
5, 4	VD0DFCK[1:0]	LVD0 digital filter sampling clock select	00: φloco/1 01: φloco/2 10: φloco/4 11: φloco/8	R/W
3	VD0DFS	LVD0 digital filter function select	0: Disables the digital filter function. 1: Enables the digital filter function.	R/W
2, 1	—	Reserved	These bits are read as 0. The write value should always be 0.	—
0	—	Reserved	This bit is read as 1. The write value should be 1.	—

Note: This register is not initialized by an LVD2 reset and LVD1 reset.

(2) Power Supply Voltage and Operating Frequency Range



(3) Accuracy Guarantee Range of Analog Power Supply Voltage and A/D Converter