Infineon Technologies - MB96F395RSAPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LCD, LVD, LVR, POR, PWM, WDT
Number of I/O	76
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f395rsapmc-gse2

■ PRODUCT LINEUP

Features		MB96V300B	MB9639x
Product type		Evaluation sample	Flash product: MB96F39x Mask ROM product: MB9639x
Product options			
YS		NA	LVD persistently on / Single clock devices
RS			LVD can be disabled / Single clock devices
YW			LVD persistently on / Dual clock devices
RW			LVD can be disabled / Dual clock devices
Flash/ROM	RAM		
160kB	5kB	ROM/Flash memory emulation by external RAM, 92kB internal RAM	MB96F395Y*1, MB96F395R*1,
Package		BGA416	FPT-100P-M20
DMA		16 channels	0 channels
USART		10 channels	3 channels
I2C		2 channels	1 channel
A/D Converter		40 channels	11 channels
A/D Converter Reference Voltage switch		yes	No
16-bit Reload Timer		6 channels + 1 channel (for PPG)	4 channels + 1 channel (for PPG)
16-bit Free-Running Timer		4 channels	2 channels
16-bit Output Compare		12 channels	4 channels
16-bit Input Capture		12 channels	4 channels
16-bit Programmable Pulse Generator		20 channels	4 channels
CAN Interface		5 channels	1 channels
Stepping Motor Controller		6 channels	4 channels
External Interrupts		16 channels	8 channels
Non-Maskable Interrupt		1 channel	
Sound generator		2 channels	1 channels
LCD Controller		4 COM x 72 SEG	4 COM x 49 SEG

■ PIN FUNCTION DESCRIPTION

Pin Function description (1 / 2)

Pin name	Feature	Description
ADTG	ADC	A/D converter trigger input
ALARMn	Alarm comparator	Alarm Comparator n input
ANn	ADC	A/D converter channel n input
AV_{CC}	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AV_{SS}	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTn_R	Clock output function	Relocated Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
CKOTXn_R	Clock output function	Relocated Clock Output function n inverted output
COMn	LCD	LCD COM pins
DV_{CC}	Supply	SMC pins power supply
FRCKn	Free Running Timer	Free Running Timer n input
FRCKn_R	Free Running Timer	Relocated Free Running Timer n input
INn	ICU	Input Capture Unit n input
INn_R	ICU	Relocated Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
MDn	Core	Input pins for specifying the operating mode.
NMI	External Interrupt	Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
OUTn_R	OCU	Relocated Output Compare Unit n waveform output
Pxx_n	GPIO	General purpose IO
PPGn	PPG	Programmable Pulse Generator n output
PPGn_R	PPG	Relocated Programmable Pulse Generator n output
PWMn	SMC	SMC PWM high current
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input

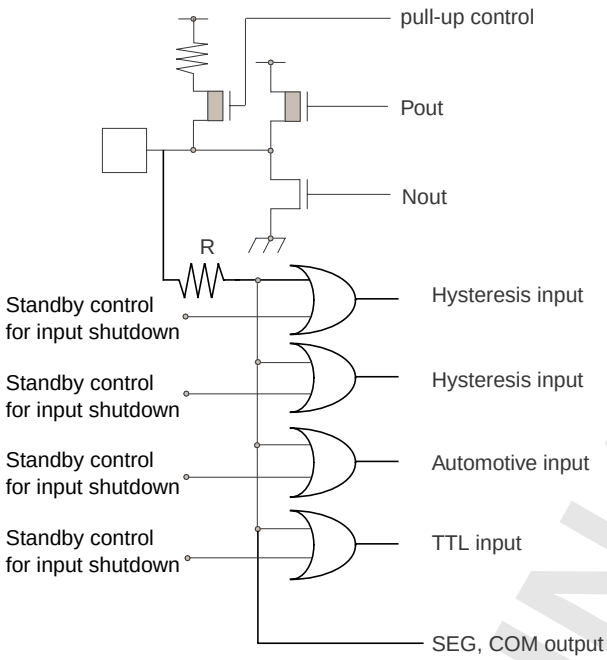
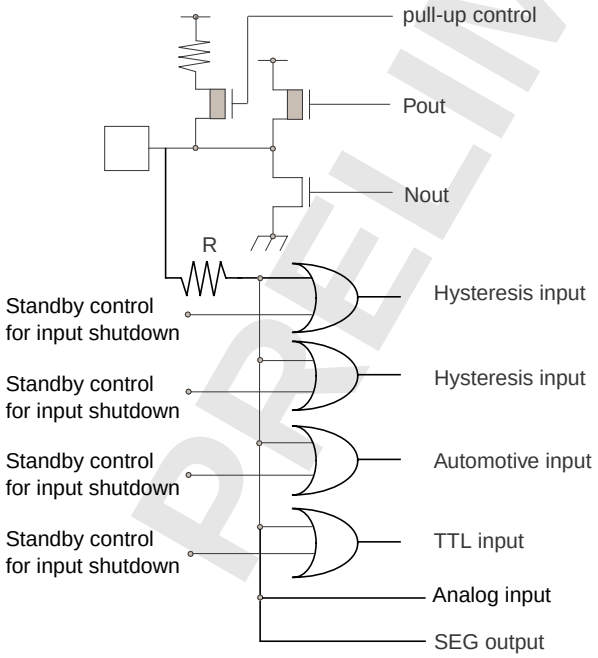
Pin Function description (2 / 2)

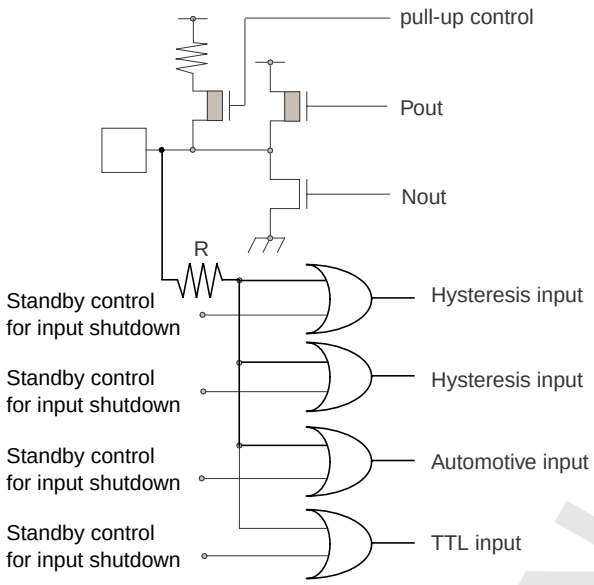
Pin name	Feature	Description
SCKn	USART	USART n serial clock input/output
SCLn	I2C	I2C interface n clock I/O input/output
SDAn	I2C	I2C interface n serial data I/O input/output
SEGn	LCD	LCD segment n
SGA	Sound Generator	SG amplitude output
SGO	Sound Generator	SG sound/tone output
SINn	USART	USART n serial data input
SOTn	USART	USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
Vn	LCD	LCD voltage references
V_{CC}	Supply	Power supply
V_{SS}	Supply	Power supply
WOT	RTC	Real Timer clock output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix "W")
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix "W")

■ PIN CIRCUIT TYPE

FPT-100P-M20	
Pin no.	Circuit type
1	Supply
2	F
3 to 10	J
11,12	N
13 to 17	K
18	Supply
19 to 20	G
21	Supply
22 to 24	K
25,26	Supply
27 to 29	K
30 to 34	M
35,36	Supply
37 to 43	M
44,45	Supply
46 to 49	M
50, 51	Supply
52 to 54	C
55, 56	A
57	Supply
58,59	B[1)]
58,59	H[2)]
60	E
61 to 74	J
75 to 76	Supply

[1)] Devices with suffix ”W”
[2)] Devices without suffix ”W”

Type	Circuit	Remarks
J		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx. • SEG or COM output
K		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function. • Programmable pull-up resistor: 50kΩ approx. • Analog input • SEG output

Type	Circuit	Remarks
N		• CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx.

■ SERIAL PROGRAMMING COMMUNICATION INTERFACE

USART pins for Flash serial programming (MD[2:0] = 010, Serial Communication mode)

MB96F39x		
Pin number	USART Number	Normal function
LQFP-100		
8	USART0	SIN0
9		SOT0
10		SCK0
3	USART1	SIN1
4		SOT1
5		SCK1
46	USART2	SIN2
47		SOT2
48		SCK2

Note: If a Flash programmer and its software needs to use a handshaking pin, Fujitsu suggests to the tool vendor to support at least port P00_1 on pin 88.
If handshaking is used by the tool but P00_1 is not available in customer's application, Fujitsu suggests to the customer to check the tool manual or to contact the tool vendor for alternative handshaking pins.

I/O map MB96F39x (18 / 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004C9H	I/O Port P13 - External Pin State Register	EPSR13		R
0004CAH-0004CFH	Reserved			-
0004D0H	ADC analog input enable register 0	ADER0		RW
0004D1H	ADC analog input enable register 1	ADER1		RW
0004D2H	ADC analog input enable register 2	ADER2		RW
0004D3H	ADC analog input enable register 3	ADER3		RW
0004D4H	ADC analog input enable register 4	ADER4		RW
0004D5H	Reserved			-
0004D6H	Peripheral Resource Relocation Register 0	PRRR0		RW
0004D7H	Peripheral Resource Relocation Register 1	PRRR1		RW
0004D8H	Peripheral Resource Relocation Register 2	PRRR2		RW
0004D9H	Peripheral Resource Relocation Register 3	PRRR3		RW
0004DAH	Peripheral Resource Relocation Register 4	PRRR4		RW
0004DBH	Peripheral Resource Relocation Register 5	PRRR5		RW
0004DCH	Peripheral Resource Relocation Register 6	PRRR6		RW
0004DDH	Peripheral Resource Relocation Register 7	PRRR7		RW
0004DEH	Peripheral Resource Relocation Register 8	PRRR8		RW
0004DFH	Peripheral Resource Relocation Register 9	PRRR9		RW
0004E0H	RTC - Sub Second Register L	WTBRL0	WTBR0	RW
0004E1H	RTC - Sub Second Register M	WTBRH0		RW
0004E2H	RTC - Sub-Second Register H	WTBR1		RW
0004E3H	RTC - Second Register	WTSR		RW
0004E4H	RTC - Minutes	WTMR		RW
0004E5H	RTC - Hour	WTHR		RW
0004E6H	RTC - Timer Control Extended Register	WTCER		RW
0004E7H	RTC - Clock select register	WTCKSR		RW
0004E8H	RTC - Timer Control Register Low	WTCRL	WTCR	RW
0004E9H	RTC - Timer Control Register High	WTCRH		RW
0004EAH	CAL - Calibration unit Control register	CUCR		RW

■ INTERRUPT VECTOR TABLE

Interrupt vector table MB96(F)39x (1 / 3)

Vector number	Offset in vector table	Vector name	Index in ICR to program	Description
0	3FC	CALLV0	-	
1	3F8	CALLV1	-	
2	3F4	CALLV2	-	
3	3F0	CALLV3	-	
4	3EC	CALLV4	-	
5	3E8	CALLV5	-	
6	3E4	CALLV6	-	
7	3E0	CALLV7	-	
8	3DC	RESET	-	
9	3D8	INT9	-	
10	3D4	EXCEPTION	-	
11	3D0	NMI	-	Non-Maskable Interrupt
12	3CC	DLY	12	Delayed Interrupt
13	3C8	RC_TIMER	13	RC Timer
14	3C4	MC_TIMER	14	Main Clock Timer
15	3C0	SC_TIMER	15	Sub Clock Timer
16	3BC			Reserved
17	3B8	EXTINT0	17	External Interrupt 0
18	3B4	EXTINT1	18	External Interrupt 1
19	3B0	EXTINT2	19	External Interrupt 2
20	3AC	EXTINT3	20	External Interrupt 3
21	3A8	EXTINT4	21	External Interrupt 4
22	3A4	EXTINT5	22	External Interrupt 5
23	3A0	EXTINT6	23	External Interrupt 6
24	39C	EXTINT7	24	External Interrupt 7
25	398	CAN0	25	CAN Controller 0
26	394			Reserved
27	390	PPG0	27	Programmable Pulse Generator 0
28	38C	PPG1	28	Programmable Pulse Generator 1
29	388	PPG2	29	Programmable Pulse Generator 2
30	384	PPG3	30	Programmable Pulse Generator 3
31	380			Reserved
32	37C			Reserved

■ HANDLING DEVICES

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- SMC power supply pins

1. Latch-up prevention

- CMOS IC chips may suffer latch-up under the following conditions:
  - A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
  - A voltage higher than the rated voltage is applied between V_{CC} and V_{SS}.
  - The AV_{CC} power supply is applied before the V_{CC} voltage.
- Latch-up may increase the power supply current dramatically, causing thermal damages to the device.
- For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

2. Unused pins handling

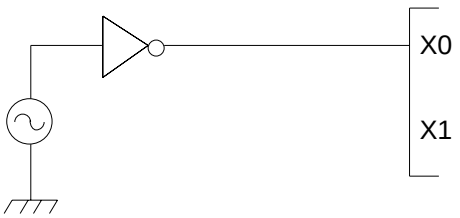
- Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).
- Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.
- Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

3. External clock usage

- The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

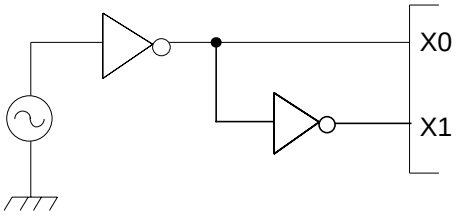
1. Single phase external clock

- When using a single phase external clock, X0 pin must be driven and X1 pin left open.



2. Opposite phase external clock

- When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



4. Unused sub clock signal

- If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

5. Notes on PLL clock mode operation

- If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

6. Power supply pins (V_{CC}/V_{SS})

- It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.
- V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.
- As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 µF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

7. Crystal oscillator circuit

- Noise at X0 or X1 pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.
- It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.
- It is highly recommended to evaluate the quartz/MCU system at the quartz manufacturer.

8. Turn on sequence of power supply to A/D converter and analog inputs

- It is required to turn the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.
- It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

9. Pin handling when not using the A/D converter

- It is required to connect the unused pins of the A/D converter as AV_{CC} = V_{CC}, AV_{SS} = AVRH = AVRL = V_{SS}.

10. Notes on energization

- To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2 V to 2.7 V.

11. Stabilization of power supply voltage

- If the power supply voltage varies acutely even within the operation safety range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

12. SMC power supply pins

- All DV_{SS} pins must be set to the same level as the V_{SS} pins.
- The DV_{CC} power supply level can be set independently of the V_{CC} power supply level. However note that the SMC I/O pin state is undefined if DV_{CC} is powered on and V_{CC} is below 3V. To avoid this, we recommend to always power V_{CC} before DV_{CC}.

2. Recommended Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, DV_{CC}	3.0	-	5.5	V	
Smoothing capacitor at C pin	C_S	4.7	-	10	µF	Use a low inductance capacitor (for example X7R ceramic capacitor)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the devices electrical characteristics are guaranteed when the device is operated within these ranges.

Semiconductor devices must always be operated within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

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(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output “H” voltage	V_{OH2}	Normal and High Current outputs	4.5V ≤ (D)V_{CC} ≤ 5.5V I_{OH} = -2mA 3.0V ≤ (D)V_{CC} < 4.5V I_{OH} = -1.6mA	(D)V_{CC} - 0.5	-	-	V	Driving strength set to 2mA
	V_{OH5}	Normal and High Current outputs	4.5V ≤ (D)V_{CC} ≤ 5.5V I_{OH} = -5mA 3.0V ≤ (D)V_{CC} < 4.5V I_{OH} = -3mA	(D)V_{CC} - 0.5	-	-	V	Driving strength set to 5mA
	V_{OH30}	High current outputs	4.5V ≤ DV_{CC} ≤ 5.5V I_{OH} = -30mA 3.0V ≤ DV_{CC} < 4.5V I_{OH} = -20mA	DV_{CC} - 0.5	-	-	V	Driving strength set to 30mA
	V_{OH3}	I^2C outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OH} = -3mA 3.0V ≤ V_{CC} < 4.5V I_{OH} = -2mA	V_{CC} - 0.5	-	-	V	
Output “L” voltage	V_{OL2}	Normal and High Current outputs	4.5V ≤ (D)V_{CC} ≤ 5.5V I_{OL} = +2mA 3.0V ≤ (D)V_{CC} < 4.5V I_{OL} = +1.6mA	-	-	0.4	V	Driving strength set to 2mA
	V_{OL5}	Normal and High Current outputs	4.5V ≤ (D)V_{CC} ≤ 5.5V I_{OL} = +5mA 3.0V ≤ (D)V_{CC} < 4.5V I_{OL} = +3mA	-	-	0.4	V	Driving strength set to 5mA
	V_{OL30}	High current outputs	4.5V ≤ DV_{CC} ≤ 5.5V I_{OL} = +30mA 3.0V ≤ DV_{CC} < 4.5V I_{OL} = +20mA	-	-	0.5	V	Driving strength set to 30mA
	V_{OL3}	I^2C outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = +3mA 3.0V ≤ V_{CC} < 4.5V I_{OL} = +2mA	-	-	0.4	V	
Input leak current	I_{IL}	Pnn_m	DV_{CC} = V_{CC} = 5.5V V_{SS} < V_I < V_{CC}	-1	-	+1	µA	

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Total LCD leakage current	ΣI_{ILCD}	all SEG/ COM pins	V_{CC} = 5.0V	-10	0.5	10	µA	Maximum leakage current of all LCD pins
Internal LCD divide resistance	R_{LCD}	Between V3 and V_{SS}		25	35	50	kΩ	
Pull-up resistance	R_{UP}	Pnn_m, RSTX	-	25	50	100	kΩ	

Note: Input/output voltages of high current ports depend on DV_{CC}, of other ports on V_{CC}.

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Run modes*	I_{CCPLL}	PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz	35	44	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V 0 Flash/ROM wait states
			36	47		125˚C	
		PLL Run mode with CLKS1/2 = 80MHz, CLKB = CLKP1 = 40MHz, CLKP2 = 20MHz	47	60	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V 1 Flash/ROM wait state
			48	63		125˚C	
	I_{CCMAIN}	Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz	4.5	5.5	mA	25˚C	CLKPLL, CLKSC and CLKRC stopped 1 Flash/ROM wait state
			5.1	8.5		125˚C	
	I_{CCRCH}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 2MHz	2.9	4	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped 1 Flash/ROM wait state
			3.5	6.5		125˚C	

To satisfy the A/D conversion precision standard, the relationship between the external impedance and minimum sampling time must be considered and then either the resistor value and operating frequency must be adjusted or the external impedance must be decreased so that the sampling time (T_{samp}) is longer than the minimum value. Usually, this value is set to 7τ, where $\tau = RC$. If the external input resistance (R_{ext}) connected to the analog input is included, the sampling time is expressed as follows:

T_{samp} [min] = $7 \times (R_{ext} + 2.6k\Omega) \times C$ for $4.5 \leq AV_{cc} \leq 5.5$

T_{samp} [min] = $7 \times (R_{ext} + 12.1k\Omega) \times C$ for $3.0 \leq AV_{cc} \leq 4.5$

If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- About the error

The accuracy gets worse as |AVRH - AVRL| becomes smaller.

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