Infineon Technologies - MB96F395RWAPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LCD, LVD, LVR, POR, PWM, WDT
Number of I/O	74
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f395rwapmc-gse2

■ FEATURES

Feature	Description
Technology	• 0.18µm CMOS
CPU	• F2MC-16FX CPU • Up to 40 MHz internal, 25 ns instruction cycle time • Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers) • 8-byte instruction execution queue • Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available
System clock	• On-chip PLL clock multiplier (x1..25, x1 when PLL stop) • 3-16 MHz external quartz clock • Up to 40 MHz external clock • 32-100 kHz subsystem quartz clock • 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog • Clock source selectable from main- and subclock oscillator (part number suffix “W”) and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals. • Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode) • Clock modulator
On-chip voltage regulator	• Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures
Low voltage reset	• Reset is generated when supply voltage is below minimum.
Code Security	• Protects ROM content from unintended read-out
Memory Patch Function	• Replaces ROM content • Can also be used to implement embedded debug support
Interrupts	• Fast Interrupt processing • 8 programmable priority levels • Non-Maskable Interrupt (NMI)
Timers	• Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer) • Watchdog Timer

Feature	Description
Non Maskable Interrupt	• Disabled after reset • Once enabled, can not be disabled other than by reset. • Level high or level low sensitive • Pin shared with external interrupt 0.
Alarm comparator	• Monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds • Threshold voltages defined externally or generated internally • Status is readable, interrupts can be masked separately
I/O Ports	• Virtually all external pins can be used as general purpose I/O • All push-pull outputs (except when used as I2C SDA/SCL line) • Bit-wise programmable as input/output or peripheral signal • Bit-wise programmable input enable • Bit-wise programmable input levels (Automotive / CMOS-Schmitt trigger / TTL) • Bit-wise programmable pull-up resistor • Bit-wise programmable output driving strength for EMI optimization
Packages	• 100-pin plastic LQFP
Flash Memory	• Supports automatic programming, Embedded Algorithm™*1 • Write/Erase/Erase-Suspend/Resume commands • A flag indicating completion of the algorithm • Number of erase cycles: 10,000 times • Data retention time: 20 years • Erase can be performed on each sector individually • Sector protection • Flash Security feature to protect the content of the Flash • Low voltage detection during Flash erase

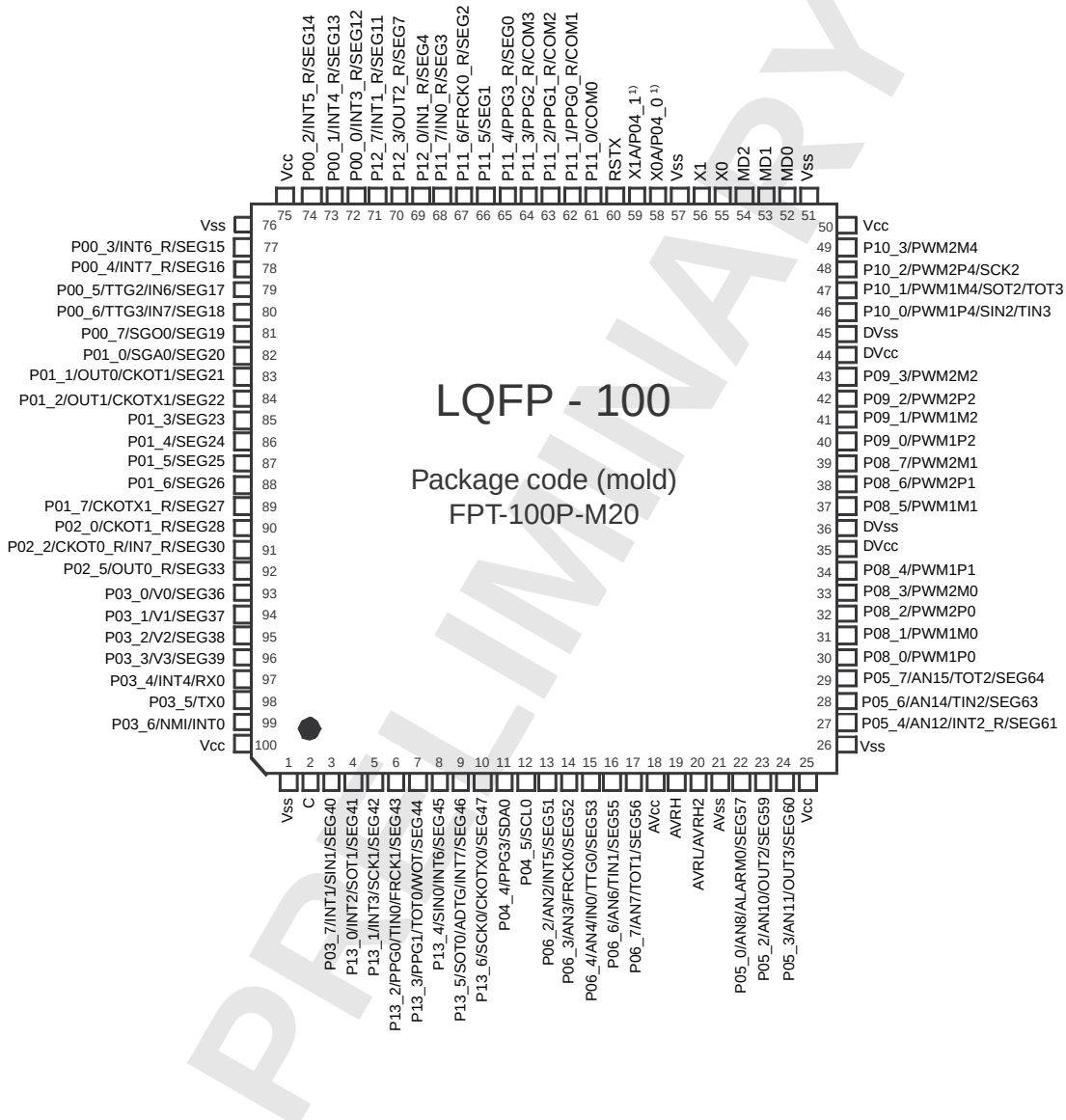
*1: Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

Features	MB96V300B	MB9639x
Real Time Clock	1	
I/O Ports	136	74 for part number with suffix "W", 76 for part number with suffix "S"
Alarm comparator	2 channels	1 channels
External bus interface	Yes	No
Clock output function	2 channels	
Low voltage reset	Yes	
On-chip RC-oscillator	Yes	

*1: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

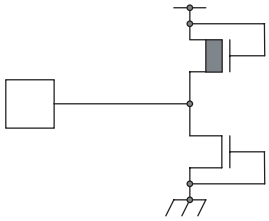
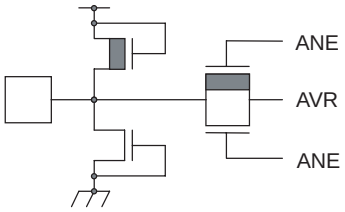
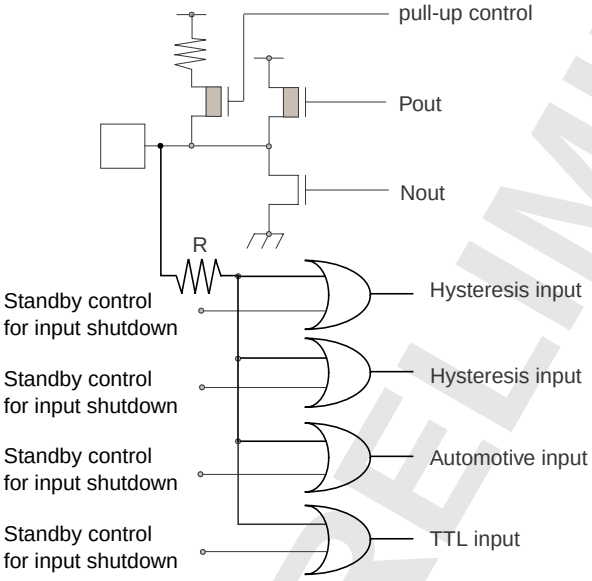
■ PIN ASSIGNMENTS

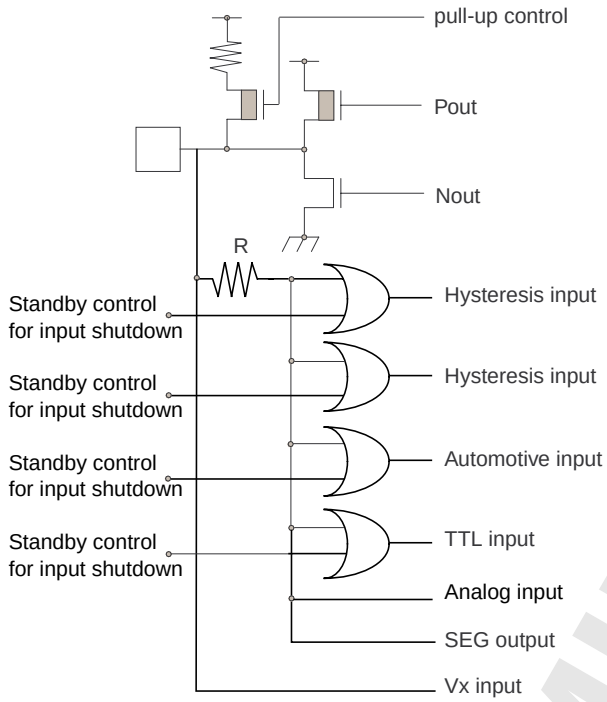
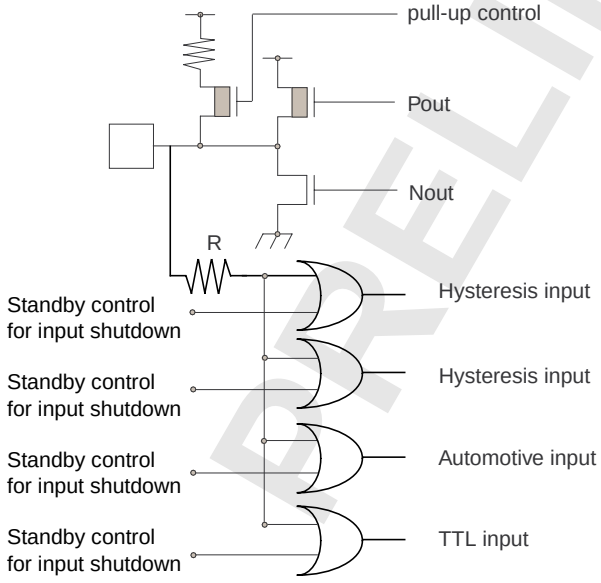
Pin assignment of MB96F39x



1) Devices with suffix W: X0A/X1A
Devices with suffix S: P04_0, P04_1

(FPT-100P-M20)

Type	Circuit	Remarks
F		• Power supply input protection circuit
G		• A/D converter ref+ (AVRH/AVRH2) power supply input pin with protection circuit • Flash devices do not have a protection circuit against VCC for pins AVRH/AVRH2 • Devices without AVRH reference switch do not have an analog switch for the AVRL pin
H		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx.

Type	Circuit	Remarks
L		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx. • Analog input • Vx input • SEG output
M		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, I_{OL} = 30mA, I_{OH} = -30mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx.

■ RAMSTART/END AND EXTERNAL BUS END ADDRESSES

Devices	Bank 0 RAM size	RAMSTART0
MB96F395	5kB	00:6E40$_H$

■ SERIAL PROGRAMMING COMMUNICATION INTERFACE

USART pins for Flash serial programming (MD[2:0] = 010, Serial Communication mode)

MB96F39x		
Pin number	USART Number	Normal function
LQFP-100		
8	USART0	SIN0
9		SOT0
10		SCK0
3	USART1	SIN1
4		SOT1
5		SCK1
46	USART2	SIN2
47		SOT2
48		SCK2

Note: If a Flash programmer and its software needs to use a handshaking pin, Fujitsu suggests to the tool vendor to support at least port P00_1 on pin 88.
If handshaking is used by the tool but P00_1 is not available in customer's application, Fujitsu suggests to the customer to check the tool manual or to contact the tool vendor for alternative handshaking pins.

I/O map MB96F39x (2 / 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000024H	FRT1 - Data register of free-running timer		TCDT1	RW
000025H	FRT1 - Data register of free-running timer			RW
000026H	FRT1 - Control status register of free-running timer Low	TCCSL1	TCCS1	RW
000027H	FRT1 - Control status register of free-running timer High	TCCSH1		RW
000028H	OCU0 - Output Compare Control Status	OCS0		RW
000029H	OCU1 - Output Compare Control Status	OCS1		RW
00002AH	OCU0 - Compare Register		OCCP0	RW
00002BH	OCU0 - Compare Register			RW
00002CH	OCU1 - Compare Register		OCCP1	RW
00002DH	OCU1 - Compare Register			RW
00002EH	OCU2 - Output Compare Control Status	OCS2		RW
00002FH	OCU3 - Output Compare Control Status	OCS3		RW
000030H	OCU2 - Compare Register		OCCP2	RW
000031H	OCU2 - Compare Register			RW
000032H	OCU3 - Compare Register		OCCP3	RW
000033H	OCU3 - Compare Register			RW
000034H-00003FH	Reserved			-
000040H	ICU0/ICU1 - Control Status Register	ICS01		RW
000041H	ICU0/ICU1 - Edge register	ICE01		RW
000042H	ICU0 - Capture Register Low	IPCPL0	IPCP0	R
000043H	ICU0 - Capture Register High	IPCPH0		R
000044H	ICU1 - Capture Register Low	IPCPL1	IPCP1	R
000045H	ICU1 - Capture Register High	IPCPH1		R
000046H	ICU2/ICU3 - Control Status Register	ICS23		RW
000047H	ICU2/ICU3 - Edge register	ICE23		RW
000048H	ICU2 - Capture Register Low	IPCPL2	IPCP2	R
000049H	ICU2 - Capture Register High	IPCPH2		R
00004AH	ICU3 - Capture Register Low	IPCPL3	IPCP3	R

I/O map MB96F39x (16 / 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000470H	I/O Port P04 - Extended Port Input Level Register	EPILR04		RW
000471H	I/O Port P05 - Extended Port Input Level Register	EPILR05		RW
000472H	I/O Port P06 - Extended Port Input Level Register	EPILR06		RW
000473H	Reserved			-
000474H	I/O Port P08 - Extended Port Input Level Register	EPILR08		RW
000475H	I/O Port P09 - Extended Port Input Level Register	EPILR09		RW
000476H	I/O Port P10 - Extended Port Input Level Register	EPILR10		RW
000477H	I/O Port P11 - Extended Port Input Level Register	EPILR11		RW
000478H	I/O Port P12 - Extended Port Input Level Register	EPILR12		RW
000479H	I/O Port P13 - Extended Port Input Level Register	EPILR13		RW
00047AH-00047FH	Reserved			-
000480H	I/O Port P00 - Port Output Drive Register	PODR00		RW
000481H	I/O Port P01 - Port Output Drive Register	PODR01		RW
000482H	I/O Port P02 - Port Output Drive Register	PODR02		RW
000483H	I/O Port P03 - Port Output Drive Register	PODR03		RW
000484H	I/O Port P04 - Port Output Drive Register	PODR04		RW
000485H	I/O Port P05 - Port Output Drive Register	PODR05		RW
000486H	I/O Port P06 - Port Output Drive Register	PODR06		RW
000487H	Reserved			-
000488H	I/O Port P08 - Port Output Drive Register	PODR08		RW
000489H	I/O Port P09 - Port Output Drive Register	PODR09		RW
00048AH	I/O Port P10 - Port Output Drive Register	PODR10		RW
00048BH	I/O Port P11 - Port Output Drive Register	PODR11		RW
00048CH	I/O Port P12 - Port Output Drive Register	PODR12		RW
00048DH	I/O Port P13 - Port Output Drive Register	PODR13		RW
00048EH-00049BH	Reserved			-
00049CH	I/O Port P08 - Port High Drive Register	PHDR08		RW
00049DH	I/O Port P09 - Port High Drive Register	PHDR09		RW
00049EH	I/O Port P10 - Port High Drive Register	PHDR10		RW

■ HANDLING DEVICES

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- SMC power supply pins

1. Latch-up prevention

- CMOS IC chips may suffer latch-up under the following conditions:
  - A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
  - A voltage higher than the rated voltage is applied between V_{CC} and V_{SS}.
  - The AV_{CC} power supply is applied before the V_{CC} voltage.
- Latch-up may increase the power supply current dramatically, causing thermal damages to the device.
- For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

2. Unused pins handling

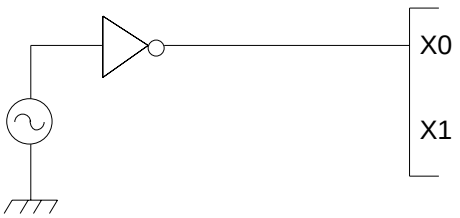
- Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).
- Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.
- Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

3. External clock usage

- The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

1. Single phase external clock

- When using a single phase external clock, X0 pin must be driven and X1 pin left open.



2. Opposite phase external clock

2. Recommended Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, DV_{CC}	3.0	-	5.5	V	
Smoothing capacitor at C pin	C_S	4.7	-	10	µF	Use a low inductance capacitor (for example X7R ceramic capacitor)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the devices electrical characteristics are guaranteed when the device is operated within these ranges.

Semiconductor devices must always be operated within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC characteristics

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input “H“ voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	0.8 V_{CC}	-	(D)V_{CC} + 0.3	V	
			CMOS Hysteresis 0.7/0.3 input selected	0.7 V_{CC}	-	(D)V_{CC} + 0.3	V	(D)V_{CC} ≥ 4.5V
				0.74 V_{CC}	-	(D)V_{CC} + 0.3	V	(D)V_{CC} < 4.5V
			AUTOMOTIVE Hysteresis input selected	0.8 V_{CC}	-	(D)V_{CC} + 0.3	V	
			TTL input selected	2.0	-	(D)V_{CC} + 0.3	V	
	V_{IHX0F}	X0	External clock in “Fast Clock Input mode”	0.8 V_{CC}	-	V_{CC} + 0.3	V	
	V_{IHX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	2.5	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	0.8 V_{CC}	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	
Input “L” voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	V_{SS} - 0.3	-	0.2 (D)V_{CC}	V	
			CMOS Hysteresis 0.7/0.3 input selected	V_{SS} - 0.3	-	0.3 (D)V_{CC}	V	
			AUTOMOTIVE Hysteresis input selected	V_{SS} - 0.3	-	0.5 (D)V_{CC}	V	(D)V_{CC} ≥ 4.5V
				V_{SS} - 0.3	-	0.46 (D)V_{CC}		(D)V_{CC} < 4.5V
			TTL input selected	V_{SS} - 0.3	-	0.8	V	
	V_{ILX0F}	X0	External clock in “Fast Clock Input mode”	V_{SS} - 0.3	-	0.2 V_{CC}	V	
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	V_{SS} - 0.3	-	0.4	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	0.2 V_{CC}	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Total LCD leakage current	ΣI_{ILCD}	all SEG/ COM pins	V_{CC} = 5.0V	-10	0.5	10	µA	Maximum leakage current of all LCD pins
Internal LCD divide resistance	R_{LCD}	Between V3 and V_{SS}		25	35	50	kΩ	
Pull-up resistance	R_{UP}	Pnn_m, RSTX	-	25	50	100	kΩ	

Note: Input/output voltages of high current ports depend on DV_{CC}, of other ports on V_{CC}.

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Run modes*	I_{CCPLL}	PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz	35	44	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V 0 Flash/ROM wait states
			36	47		125˚C	
		PLL Run mode with CLKS1/2 = 80MHz, CLKB = CLKP1 = 40MHz, CLKP2 = 20MHz	47	60	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V 1 Flash/ROM wait state
			48	63		125˚C	
	I_{CCMAIN}	Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz	4.5	5.5	mA	25˚C	CLKPLL, CLKSC and CLKRC stopped 1 Flash/ROM wait state
			5.1	8.5		125˚C	
	I_{CCRCH}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 2MHz	2.9	4	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped 1 Flash/ROM wait state
			3.5	6.5		125˚C	

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Sleep modes*	I_{CCSRCL}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 0	0.3	0.5	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode
			0.8	3.4		125˚C	
		RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 1	0.06	0.15	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode
			0.56	3		125˚C	
	I_{CCSUB}	Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz	0.04	0.12	mA	25˚C	CLKMC, CLKPLL and CLKRC stopped
			0.54	2.9		125˚C	

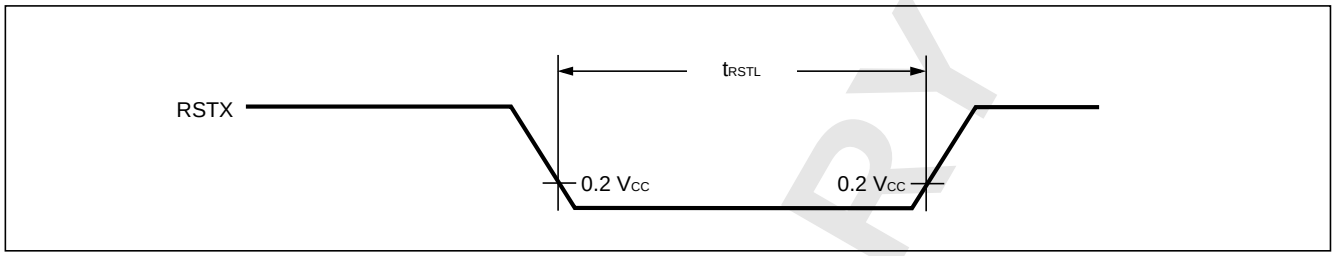
(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Timer modes*	I_{CCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz	1.6	2	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			2.1	4.8		125˚C	
	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0	0.35	0.5	mA	25˚C	CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode
			0.85	3.3		125˚C	
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1	0.1	0.15	mA	25˚C	CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode
			0.6	2.9		125˚C	
	I_{CCTRCH}	RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0	0.35	0.5	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode
			0.85	3.3		125˚C	
		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 1	0.1	0.15	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode
			0.6	2.9		125˚C	
	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0	0.3	0.45	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode
			0.8	3.2		125˚C	
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1	0.05	0.1	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode
			0.55	2.8		125˚C	

External Reset timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, DV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Reset input time	t_{RSTL}	RSTX	500	-	-	ns	



7. Low Voltage Detector characteristics

(T_A = -40 ˚C to +125 ˚C, V_{cc} = AV_{cc} = 3.0V - 5.5V, V_{ss} = AV_{ss} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Stabilization time	$T_{LVDSTAB}$	60	75	µs	
Level 0	V_{DL0}	2.7	2.9	V	CILCR:LVL[3:0]="0000"
Level 1	V_{DL1}	2.9	3.1	V	CILCR:LVL[3:0]="0001"
Level 2	V_{DL2}	3.1	3.3	V	CILCR:LVL[3:0]="0010"
Level 3	V_{DL3}	3.5	3.75	V	CILCR:LVL[3:0]="0011"
Level 4	V_{DL4}	3.6	3.85	V	CILCR:LVL[3:0]="0100"
Level 5	V_{DL5}	3.7	3.95	V	CILCR:LVL[3:0]="0101"
Level 6	V_{DL6}	3.8	4.05	V	CILCR:LVL[3:0]="0110"
Level 7	V_{DL7}	3.9	4.15	V	CILCR:LVL[3:0]="0111"
Level 8	V_{DL8}	4.0	4.25	V	CILCR:LVL[3:0]="1000"
Level 9	V_{DL9}	4.1	4.35	V	CILCR:LVL[3:0]="1001"
Level 10	V_{DL10}	not used			
Level 11	V_{DL11}	not used			
Level 12	V_{DL12}	not used			
Level 13	V_{DL13}	not used			
Level 14	V_{DL14}	not used			
Level 15	V_{DL15}	not used			

Levels 10 to 15 are not used in this device.

For correct detection, the slope of the voltage level must satisfy $\left|\frac{dV}{dt}\right| \leq 0.004\frac{V}{\mu s}$.
Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of Vcc = 2.7V. The electrical characteristics however are only valid in the specified range (usually down to 3.0V).