Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e300
Core Size	32-Bit Single-Core
Speed	400MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, USB OTG
Peripherals	DMA, WDT
Number of I/O	147
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc5121vy400b

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 7 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
$\overline{\text{PCI\_GNT0}}$	E25	PCI	V_{DD_IO}	—
$\overline{\text{PCI\_GNT1}}$	G22	PCI	V_{DD_IO}	—
$\overline{\text{PCI\_GNT2}}$	E24	PCI	V_{DD_IO}	—
PCI_CLK	C26	PCI	V_{DD_IO}	—
PSC Interface (61 Total)				
PSC_MCLK_IN	C17	General IO	V_{DD_IO}	—
PSC0_0	D16	General IO	V_{DD_IO}	—
PSC0_1	A17	General IO	V_{DD_IO}	—
PSC0_2	E15	General IO	V_{DD_IO}	—
PSC0_3	C16	General IO	V_{DD_IO}	—
PSC0_4	B16	General IO	V_{DD_IO}	—
PSC1_0	C15	General IO	V_{DD_IO}	—
PSC1_1	A16	General IO	V_{DD_IO}	—
PSC1_2	E14	General IO	V_{DD_IO}	—
PSC1_3	A15	General IO	V_{DD_IO}	—
PSC1_4	D14	General IO	V_{DD_IO}	—
PSC2_0	C14	General IO	V_{DD_IO}	—
PSC2_1	B14	General IO	V_{DD_IO}	—
PSC2_2	E13	General IO	V_{DD_IO}	—
PSC2_3	A14	General IO	V_{DD_IO}	—
PSC2_4	D13	General IO	V_{DD_IO}	—
PSC3_0	AF3	General IO	V_{DD_IO}	—
PSC3_1	AB5	General IO	V_{DD_IO}	—
PSC3_2	AC4	General IO	V_{DD_IO}	—
PSC3_3	AD4	General IO	V_{DD_IO}	—
PSC3_4	AF4	General IO	V_{DD_IO}	—
PSC4_0	AB1	General IO	V_{DD_IO}	—
PSC4_1	AA3	General IO	V_{DD_IO}	—
PSC4_2	AB3	General IO	V_{DD_IO}	—
PSC4_3	AA5	General IO	V_{DD_IO}	—
PSC4_4	AC2	General IO	V_{DD_IO}	—
PSC5_0	AC1	General IO	V_{DD_IO}	—
PSC5_1	AC3	General IO	V_{DD_IO}	—
PSC5_2	AD1	General IO	V_{DD_IO}	—

3.1.3 DC Electrical Specifications

Table 6 gives the DC Electrical characteristics for the MPC5121e/MPC5123 at recommended operating conditions.

Table 6. DC Electrical Specifications

Characteristic	Condition	Symbol	Min	Max	Unit	SpecID
Input high voltage	Input type = TTL V_{DD_IO}	V_{IH}	0.51 × V_{DD_IO}	—	V	D3.1
Input high voltage	Input type = TTL $V_{DD\_MEM\_IO\_DDR}$	V_{IH}	MVREF + 0.15	—	V	D3.2
Input high voltage	Input type = TTL $V_{DD\_MEM\_IO\_DDR2}$	V_{IH}	MVREF + 0.125	—	V	D3.3
Input high voltage	Input type = TTL $V_{DD\_MEM\_IO\_LPDDR}$	V_{IH}	0.7 × $V_{DD\_MEM\_IO\_LPDDR}$	—	V	D3.4
Input high voltage	Input type = PCI V_{DD_IO}	V_{IH}	0.5 × V_{DD_IO}	—	V	D3.5
Input high voltage	Input type = Schmitt V_{DD_IO}	V_{IH}	0.65 × V_{DD_IO}	—	V	D3.6
Input high voltage	SYS_XTALI crystal mode[1] Bypass mode[2]	CV_{IH}	Vxtal + 0.4V (V_{DD_IO}/2) + 0.4V	—	V	D3.7
Input high voltage	SATA_XTALI crystal mode Bypass mode	SV_{IH}	Vxtal + 0.4V (V_{DD_IO}/2) + 0.4V	—	V	D3.8
Input high voltage	USB_XTALI crystal mode Bypass mode	UV_{IH}	Vxtal + 0.4V (V_{DD_IO}/2) + 0.4V	—	V	D3.9
Input high voltage	RTC_XTALI crystal mode[3] Bypass mode[4]	RV_{IH}	(VBAT_RTC/5) + 0.5V (VBAT_RTC/2) + 0.4V	—	V	D3.10
Input low voltage	Input type = TTL V_{DD_IO}	V_{IL}	—	0.42 × V_{DD_IO}	V	D3.11
Input low voltage	Input type = TTL $V_{DD\_MEM\_IO\_DDR}$	V_{IL}	—	MVREF – 0.15	V	D3.12
Input low voltage	Input type = TTL $V_{DD\_MEM\_IO\_DDR2}$	V_{IL}	—	MVREF – 0.125	V	D3.13
Input low voltage	Input type = TTL $V_{DD\_MEM\_IO\_LPDDR}$	V_{IL}	—	0.3 × $V_{DD\_MEM\_IO\_LPDDR}$	V	D3.14
Input low voltage	Input type = PCI V_{DD_IO}	V_{IL}	—	0.3 × V_{DD_IO}	V	D3.15
Input low voltage	Input type = Schmitt V_{DD_IO}	V_{IL}	—	0.35 × V_{DD_IO}	V	D3.16
Input low voltage	SYS_XTALI crystal mode Bypass mode	CV_{IL}	—	Vxtal – 0.4 (V_{DD_IO}/2) – 0.4	V	D3.17
Input low voltage	SATA_XTALI crystal mode Bypass mode	SV_{IL}	—	Vxtal – 0.4 V (V_{DD_IO}/2) – 0.4	V	D3.18
Input low voltage	USB_XTALI crystal mode Bypass mode	UV_{IL}	—	Vxtal – 0.4 (V_{DD_IO}/2) – 0.4	V	D3.19
Input low voltage	RTC_XTALI crystal mode Bypass mode	RV_{IL}	—	(VBAT_RTC/5) – 0.5 (VBAT_RTC/2) – 0.4	V	D3.20
Input leakage current	Vin = 0 or V_{DD_IO}/$V_{DD\_MEM\_IO\_DDR/2}$ (depending on input type)[5]	I_{IN}	–2.5	2.5	µA	D3.21
Input leakage current	SYS_XTALI Vin = 0 or V_{DD_IO}	I_{IN}	—	20	µA	D3.22

3.1.6.1 Heat Dissipation

An estimation of the chip-junction temperature, T_J, can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \text{Eqn. 3}$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
P_D = power dissipation in package (W)

The junction to ambient thermal resistance is an industry standard value, which provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board, and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is correct depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 4}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction to case thermal resistance (°C/W)
$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. You control the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, you can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for ceramic packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \text{Eqn. 5}$$

where:

T_T = thermocouple temperature on top of package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned, so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over approximately one mm of wire extending

from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

3.2 Oscillator and PLL Electrical Characteristics

The MPC5121e/MPC5123 System requires a system-level clock input SYS_XTALI. This clock input may be driven directly from an external oscillator or with a crystal using the internal oscillator.

There is a separate oscillator for the independent Real Time Clock (RTC) system.

The MPC5121e/MPC5123 clock generation uses two phase locked loop (PLL) blocks.

- The system PLL (SYS_PLL) takes an external reference frequency and generates the internal system clock. The system clock frequency is determined by the external reference frequency and the settings of the SYS_PLL configuration.
- The e300 core PLL (CORE_PLL) generates a master clock for all of the CPU circuitry. The e300 core clock frequency is determined by the system clock frequency and the settings of the CORE_PLL configuration.

The USB PHY contains its own oscillator with the input USB_XTALI and an embedded PLL.

The SATA PHY contains its own oscillator with the input SATA_XTALI and an embedded PLL.

3.2.1 System Oscillator Electrical Characteristics

Table 11. System Oscillator Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit	SpecID
SYS_XTALI frequency	f_{sys_xtal}	15.6	33.3	35.0	MHz	O1.1

The system oscillator can work in oscillator mode or in bypass mode to support an external input clock as clock reference.

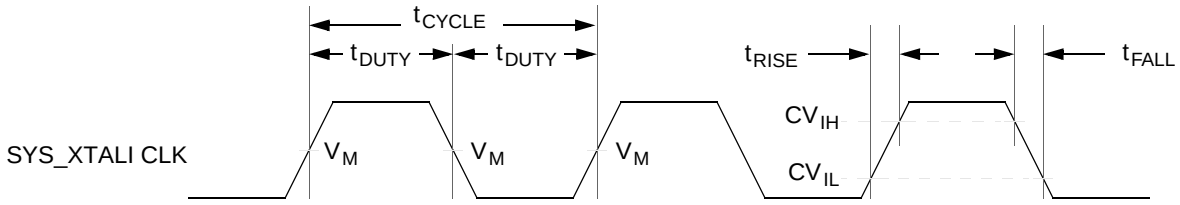

Figure 3. Timing Diagram—SYS_XTALI

Table 12. SYS_XTALI Timing

Sym	Description	Min	Max	Units	SpecID
t_{CYCLE}	SYS_XTALI cycle time[1, 2]	64.1	28.57	ns	O.1.2
t_{RISE}	SYS_XTALI rise time[3]	1	4	ns	O.1.3
t_{FALL}	SYS_XTALI fall time[4]	1	4	ns	O.1.4
t_{DUTY}	SYS_XTALI duty cycle[5]	40	60	%	O.1.5

1 The SYS_XTALI frequency and system PLL settings must be chosen such that the resulting system frequencies do not exceed their respective maximum or minimum operating frequencies. See the *MPC5121e Microcontroller Reference Manual*.

2 The MIN/Max cycle times are calculated using $1/f_{sys\_xtal\ (MIN/MAX)}$ where the $f_{sys\_xtal\ (MIN/MAX)}$ (15.6/35 MHz) are taken from Table 11.

3 Rise time is measured from 20% of vdd to 80% of V_{DD}.

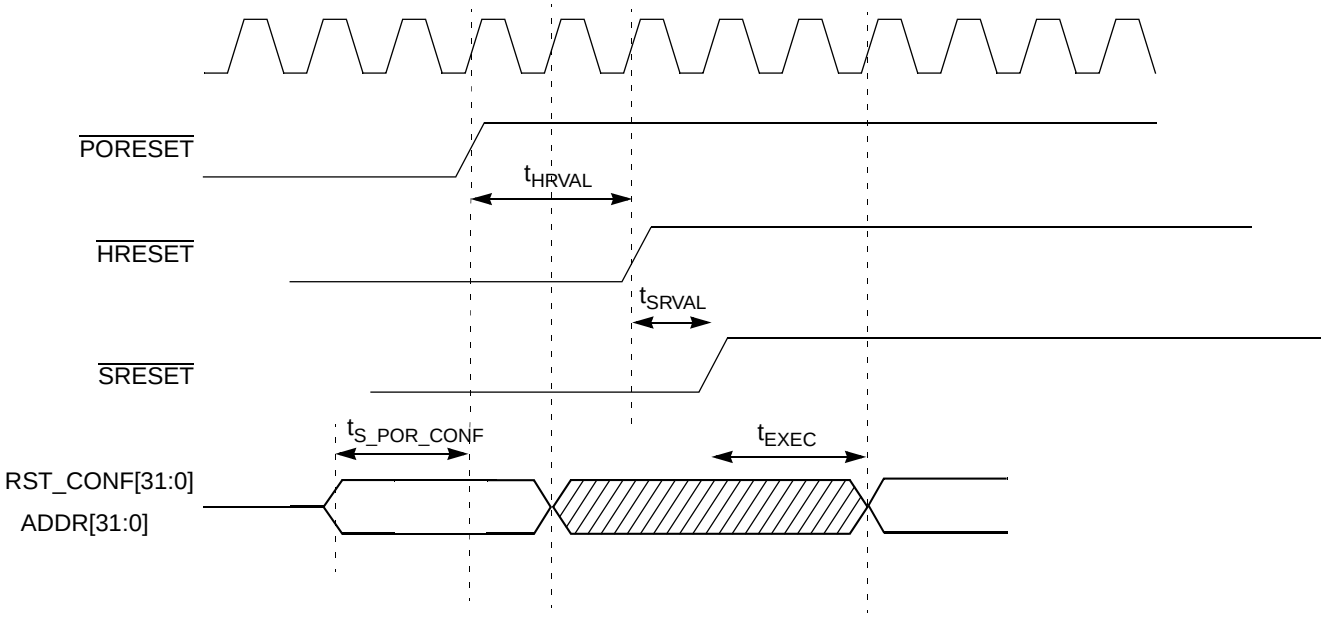

Figure 4. Power-Up Behavior

Figure 5. Power-On Reset Behavior

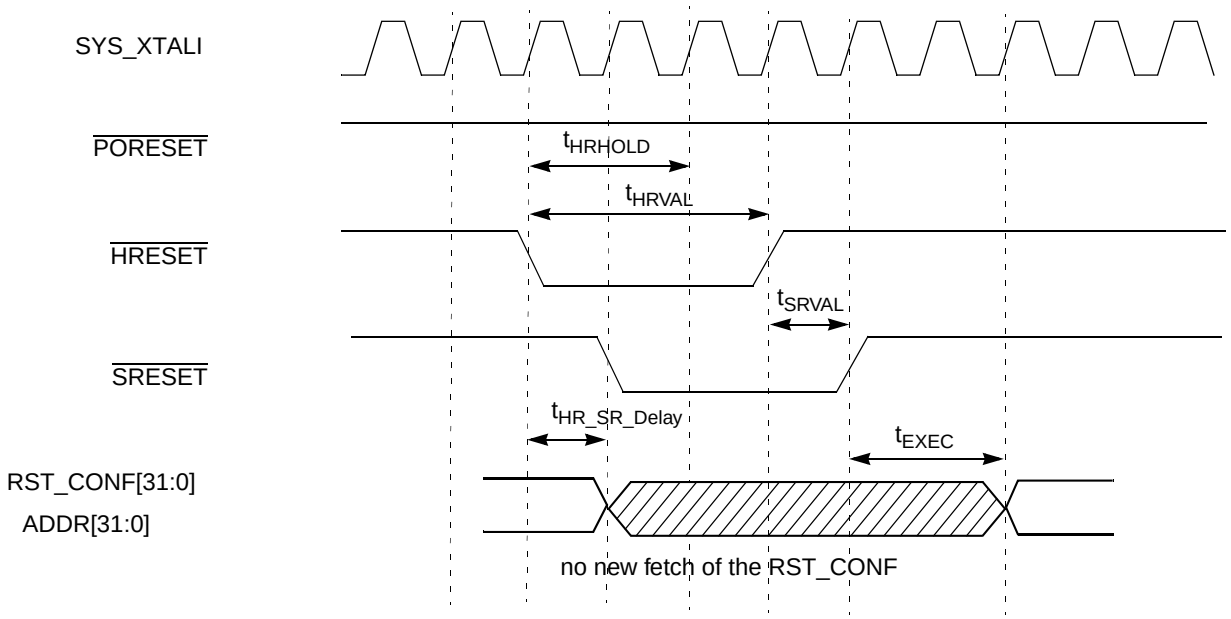

Figure 6. HRESET Behavior

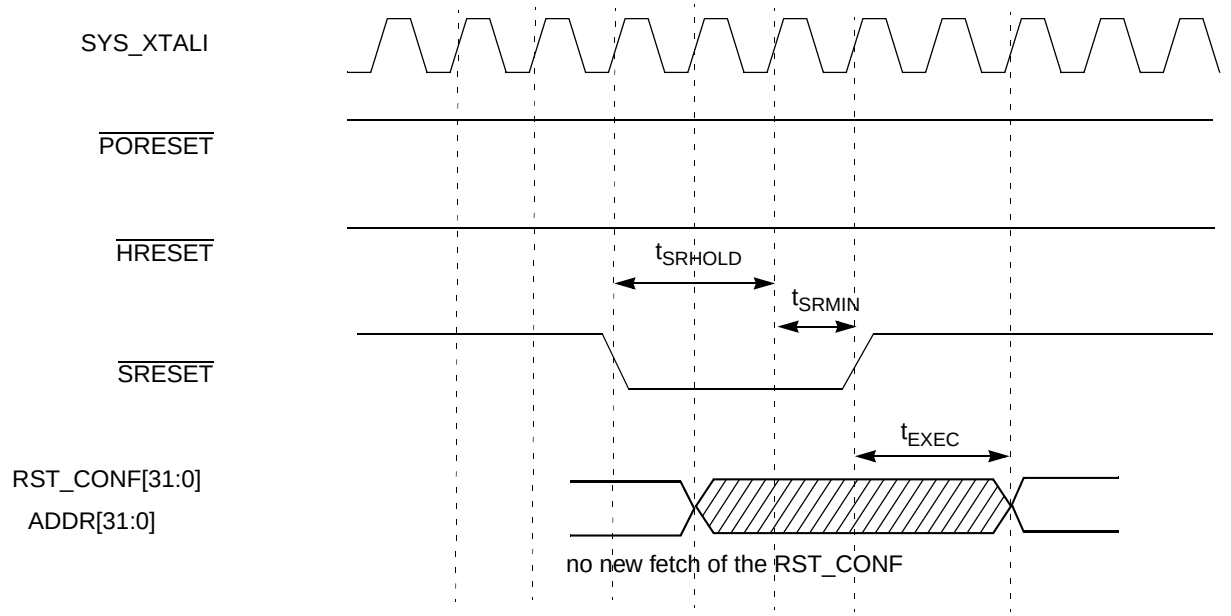

Figure 7. SRESET Behavior

Table 18. Reset Timing

Symbol	Description	Value SYS_XTALI	SpecID
$t_{PORHOLD}$	Time $\overline{\text{PORESET}}$ must be held low before a qualified reset occurs	4 cycles	A3.10
t_{HRVAL}	Time $\overline{\text{HRESET}}$ is asserted after a qualified reset occurs	26810 cycles	A3.11
t_{SRVAL}	Time $\overline{\text{SRESET}}$ is asserted after assertion of $\overline{\text{HRESET}}$	32 cycles	A3.12
t_{EXEC}	Time between $\overline{\text{SRESET}}$ assertion and first core instruction fetch	4 cycles	A3.13

Table 18. Reset Timing (continued)

Symbol	Description	Value SYS_XTALI	SpecID
$t_{S\_POR\_CONF}$	Reset configuration setup time before assertion of $\overline{\text{PORESET}}$	1 cycle	A3.14
$t_{H\_POR\_CONF}$	Reset configuration hold time after assertion of $\overline{\text{PORESET}}$	1 cycle	A3.15
$t_{HR\_SR\_DELAY}$	Time from falling edge of HRESET to falling edge of SRESET	4 cycles	A3.16
t_{HRHOLD}	Time $\overline{\text{HRESET}}$ must be held low before a qualified reset occurs	4 cycles	A3.17
t_{SRHOLD}	Time $\overline{\text{SRESET}}$ must be held low before a qualified reset occurs	4 cycles	A3.18
t_{SRMIN}	Time $\overline{\text{SRESET}}$ is asserted after it has been qualified	1 cycles	A3.19

3.3.4 External Interrupts

The MPC5121e/MPC5123 provides three different kinds of external interrupts:

- IRQ interrupts
- GPIO interrupts with simple interrupt capability (not available in power-down mode)
- WakeUp interrupts

Table 19. IPIC Input AC Timing Specifications[1]

Description	Symbol	Min	Unit	SpecID
IPIC inputs—minimum pulse witdh	t_{PICWID}	2T	ns	A4.1

1 T is the IP bus clock cycle. T = 12 ns is the minimum value (for the maximum IP bus freqency of 83 MHz).

IPIC inputs must be valid for at least tPICWID to ensure proper operation in edge triggered mode.

3.3.5 SDRAM (DDR)

The MPC5121e/MPC5123 memory controller supports three types of DDR devices:

- DDR-1 (SSTL_2 class II interface)
- DDR-2 (SSTL_18 interface)
- LPDDR/Mobile-DDR (1.8V I/O supply voltage)

JEDEC standards define the minimum set of requirements for complient memory devices:

- JEDEC STANDARD, DDR2 SDRAM SPECIFICATION, JESD79-2C, May 2006
- JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification, JESD79E, May 2005
- JEDEC STANDARD, Low Power Double Data Rate (LPDDR) SDRAM Specification, JESD79-4, May 2006

The MPC5121e/MPC5123 supports the configuration of two output drive strengths for DDR2 and LPDDR:

- Full drive strength
- Half drive strengh (intended for ligther loads or point-to-point environments)

The MPC5121e/MPC5123 memory controller supports dynamic on-die termination in the host device and in the DDR2 memory device.

This section includes AC specifications for all DDR SDRAM pins. The DC parameters are specified in the DC Electrical Characteristics.

3.3.7.1 Non-MUXed Mode

3.3.7.1.1 Non-MUXed Non-Burst Mode

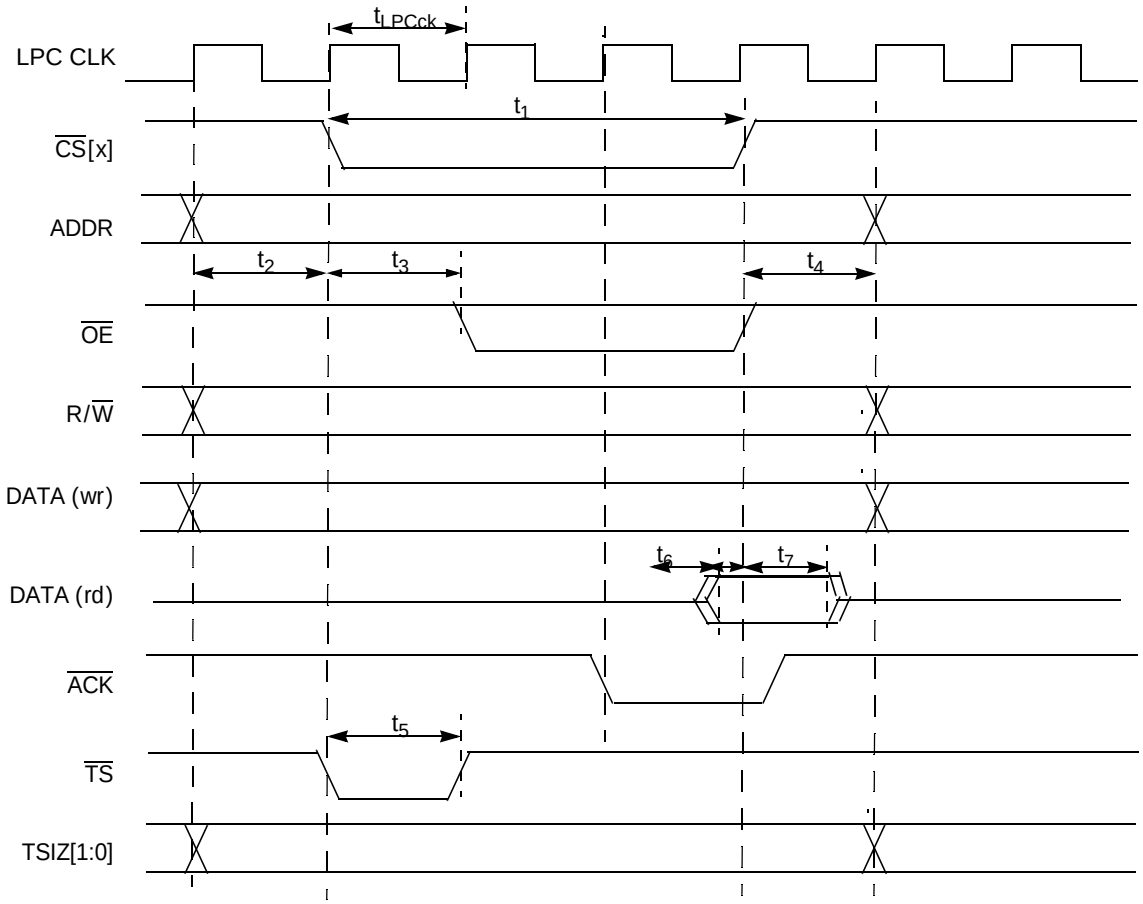

Figure 13. Timing Diagram – Non-MUXed Non-Burst Mode

NOTE

ACK is asynchonous input signal and has no timing requirements. ACK needs to be deasserted after CS[x] is deasserted.

Table 3-27. Timing Parameters PIO Read (continued)

ATA Parameter	PIO Read Mode Timing Parameter	Value	How to meet	SpecID
t_5	t_5	$t_5(min) = t_{co} + t_{su} + t_{buf} + t_{buf} + t_{cable1} + t_{cable2}$	If not met, increase time_2r	A9.23
t_6	t_6	0	—	A9.24
t_A	t_A	$t_{A(min)} = (1.5 + time\_ax) \times T - (t_{co} + t_{sui} + t_{cable2} + t_{cable2} + 2 \times t_{buf})$	calculate and programming time_ax. [1]	A9.25
t_{rd}	t_{rd1}	$t_{rd1(max)} = (-t_{rd}) + (t_{skew3} + t_{skew4})$ $t_{rd1(min)} = (time\_pio\_rdx - 0.5) \times T - (t_{su} + t_{hi})$ $(time\_pio\_rdx - 0.5) \times T > t_{su} + t_{hi} + t_{skew3} + t_{skew4}$	calculate and programming time_pio_rdx. [1]	A9.26
t_0	—	$t_{0(min)} = (time\_1 + time\_2 + time\_9) \times T$	time_1, time_2r, time_9	A9.27

1 See the *MPC5121e Microcontroller Reference Manual.*

In PIO write mode, timing waveforms are somewhat different as shown in Figure 27.

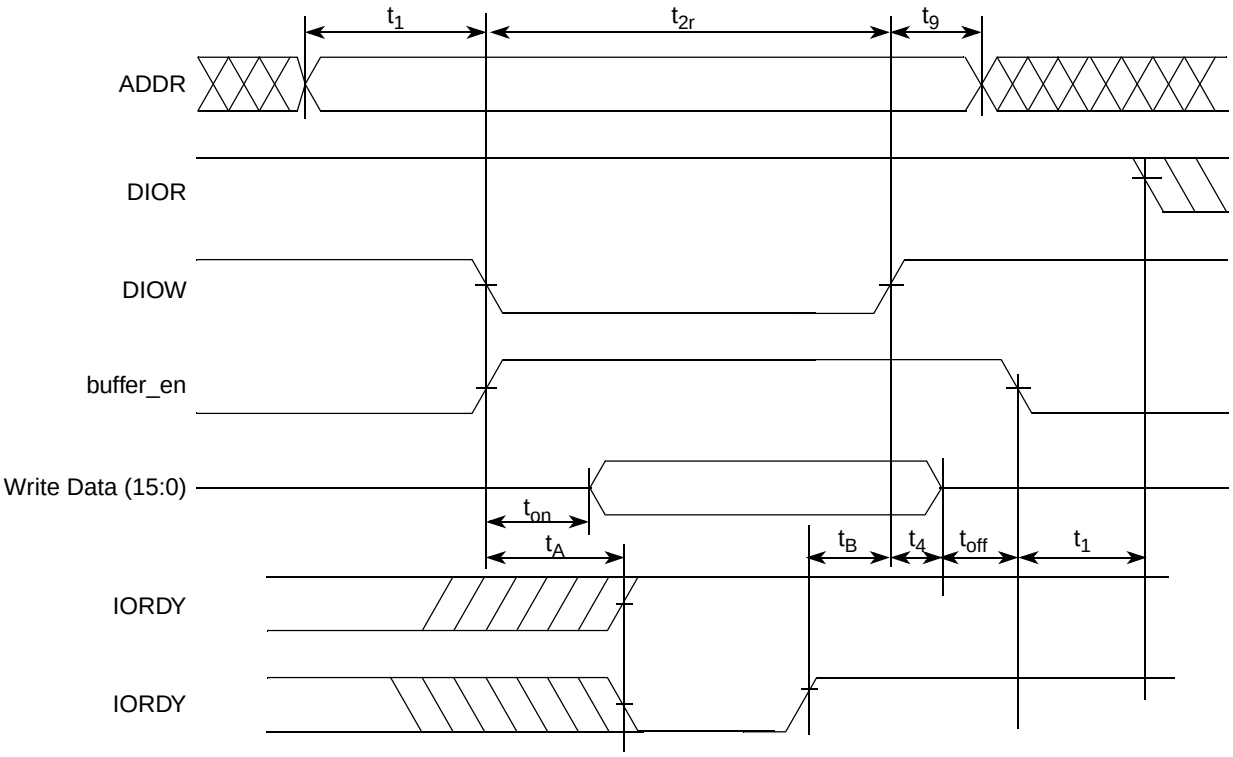

Figure 27. PIO Write Mode Timing

To fulfill this timing, several parameters need to be observed as shown in Table 3-28.

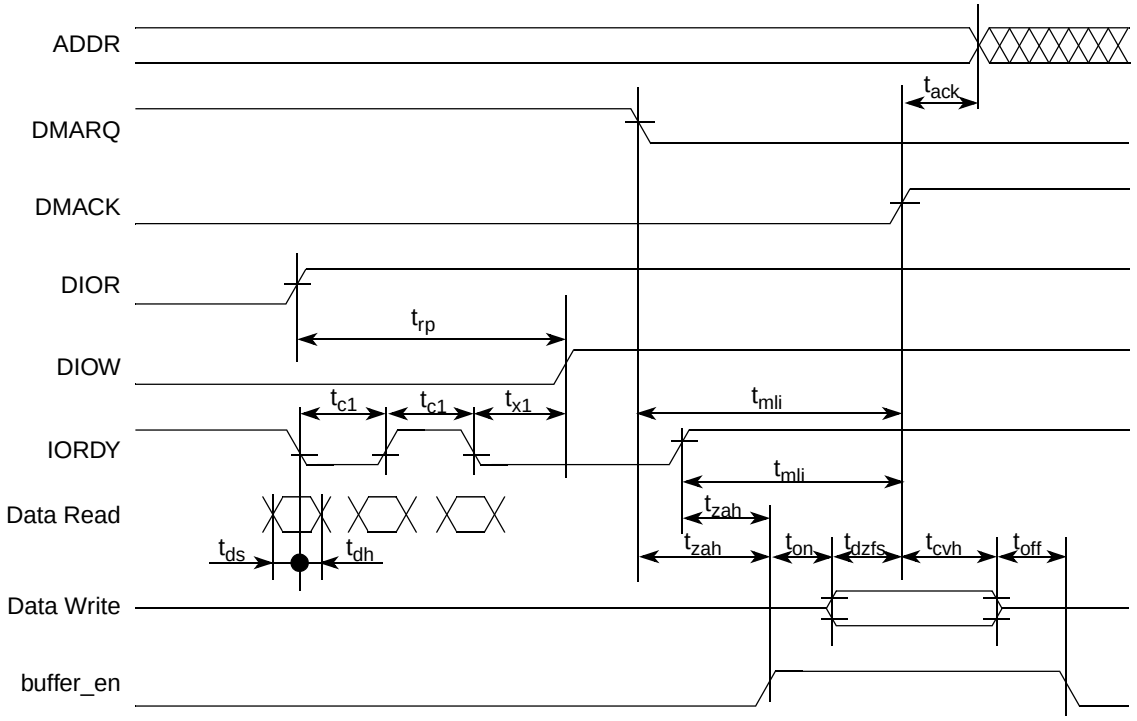

Figure 31. UDMA In Host Terminates Transfer

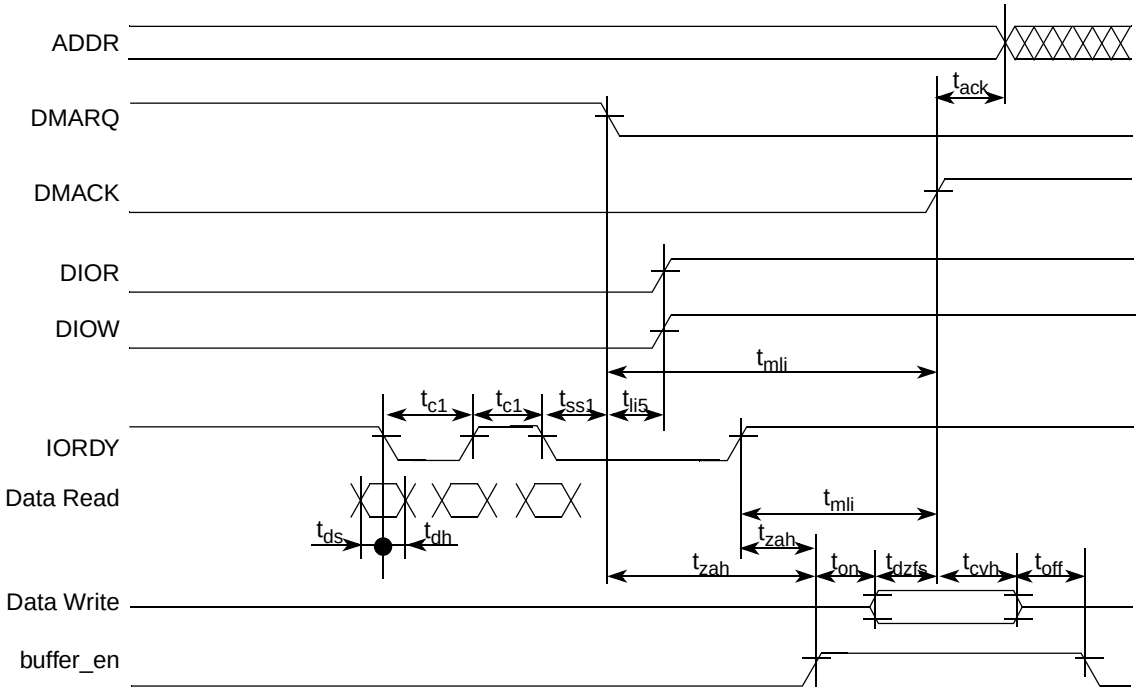

Figure 32. UDMA In Device Terminates Transfer

Timing parameters are explained in Table 30.

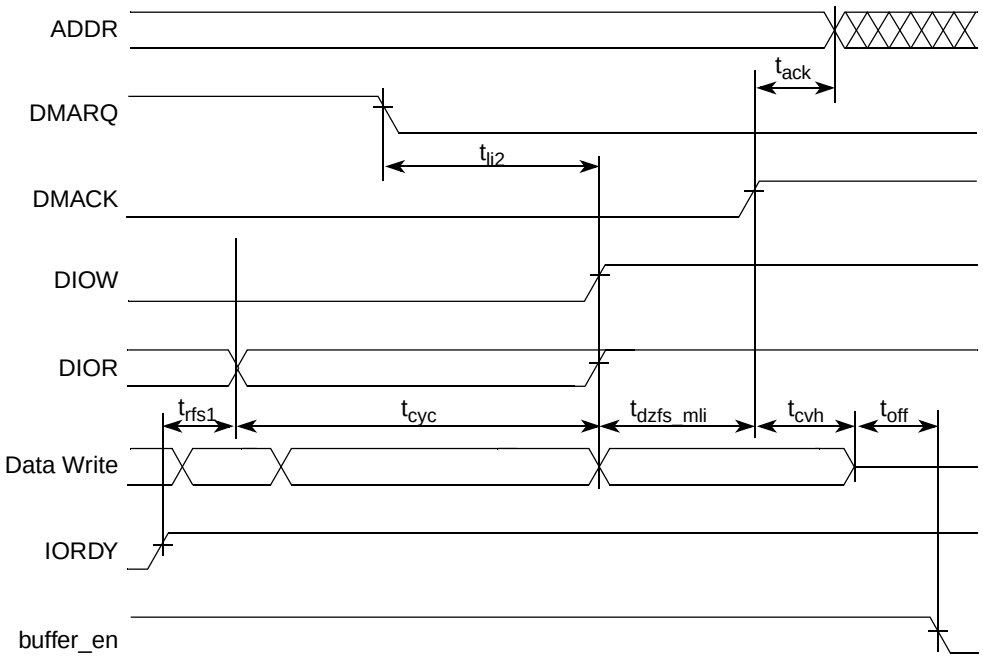

Figure 35. UDMA Out Device Terminates Transfer

Timing parameters are explained in Table 31.

Table 31. Timing Parameters UDMA Out Burst

ATA Parameter	UDMA Out Timing Parameter	Value	How to meet	SpecID
t_{ack}	t_{ack}	$t_{ack(min)} = (time\_ack \times T) - (t_{skew1} + t_{skew2})$	calculate and program time_ack. [1]	A9.63
t_{env}	t_{env}	$t_{env(min)} = (time\_env \times T) - (t_{skew1} + t_{skew2})$ $t_{env(max)} = (time\_env \times T) + (t_{skew1} + t_{skew2})$	calculate and program time_env. [1]	A9.64
t_{dvs}	t_{dvs}	$t_{dvs} = (time\_dvs \times T) - (t_{skew1} + t_{skew2})$	calculate and program time_dvs. [1]	A9.65
t_{dvh}	t_{dvh}	$t_{dvs} = (time\_dvh \times T) - (t_{skew1} + t_{skew2})$	calculate and program time_dvh. [1]	A9.66
t_{cyc}	t_{cyc}	$t_{cyc} = time\_cyc \times T - (t_{skew1} + t_{skew2})$	calculate and program time_cyc. [1]	A9.67
t_{2cyc}	—	$t_{2cyc} = time\_cyc \times 2 \times T$	calculate and program time_cyc. [1]	A9.68
t_{rfs1}	t_{rfs1}	$t_{rfs1} = 1.6 \times T + t_{sui} + t_{co} + t_{buf} + t_{buf}$	—	A9.69
—	t_{dzfs}	$t_{dzfs} = time\_dzfs \times T - (t_{skew1})$	calculate and program time_dzfs. [1]	A9.70
t_{ss}	t_{ss}	$t_{ss} = time\_ss \times T - (t_{skew1} + t_{skew2})$	calculate and program time_ss. [1]	A9.71
t_{mli}	t_{dzfs_mli}	$t_{dzfs\_mli} = \max(time\_dzfs, time\_mli) \times T - (t_{skew1} + t_{skew2})$	—	A9.72
t_{li}	t_{li1}	$t_{li1} > 0$	—	A9.73

Table 31. Timing Parameters UDMA Out Burst (continued)

ATA Parameter	UDMA Out Timing Parameter	Value	How to meet	SpecID
t_{li}	t_{li2}	$t_{li2} > 0$	—	A9.74
t_{li}	t_{li3}	$t_{li3} > 0$	—	A9.75
t_{cvh}	t_{cvh}	$t_{cvh} = (time\_cvh \times T) - (t_{skew1} + t_{skew2})$	calculate and program time_cvh. [1]	A9.76
—	t_{on} t_{off}	$t_{on} = time\_on \times T - t_{skew1}$ $t_{off} = time\_off \times T - t_{skew1}$	—	A9.77

1 See the *MPC5121e Microcontroller Reference Manual.*

3.3.10 SATA PHY

1.5 Gbps SATA PHY Layer

See “Serial ATA: High Speed Serialized AT Attachment” Revision 1.0a, 7-January-2003.

3.3.11 FEC

AC Test Timing Conditions:

- Output Loading
  All Outputs: 25 pF

Table 32. MII Rx Signal Timing

Symbol	Description	Min	Max	Unit	SpecID
1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns	A11.1
2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns	A11.2
3	RX_CLK pulse width high	35%	65%	RX_CLK Period[1]	A11.3
4	RX_CLK pulse width low	35%	65%	RX_CLK Period[1]	A11.4

1 RX_CLK shall have a frequency of 25% of data rate of the received signal. See the IEEE 802.3 Specification.

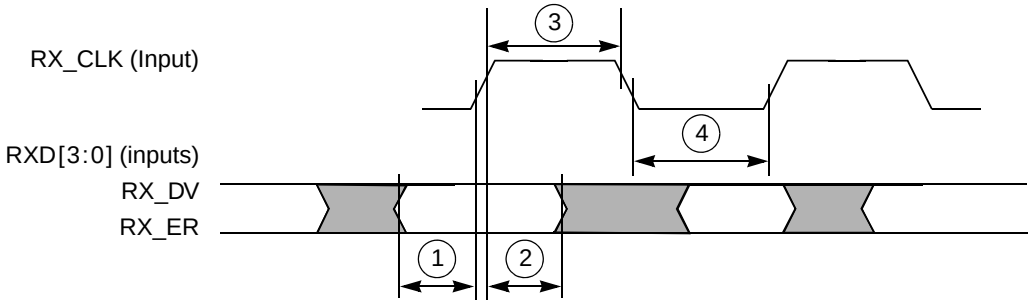

Figure 36. Ethernet Timing Diagram – MII Rx Signal

3.3.12 USB ULPI

This section specifies the USB ULPI timing.

For more information refer to UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1, October 20, 2004.

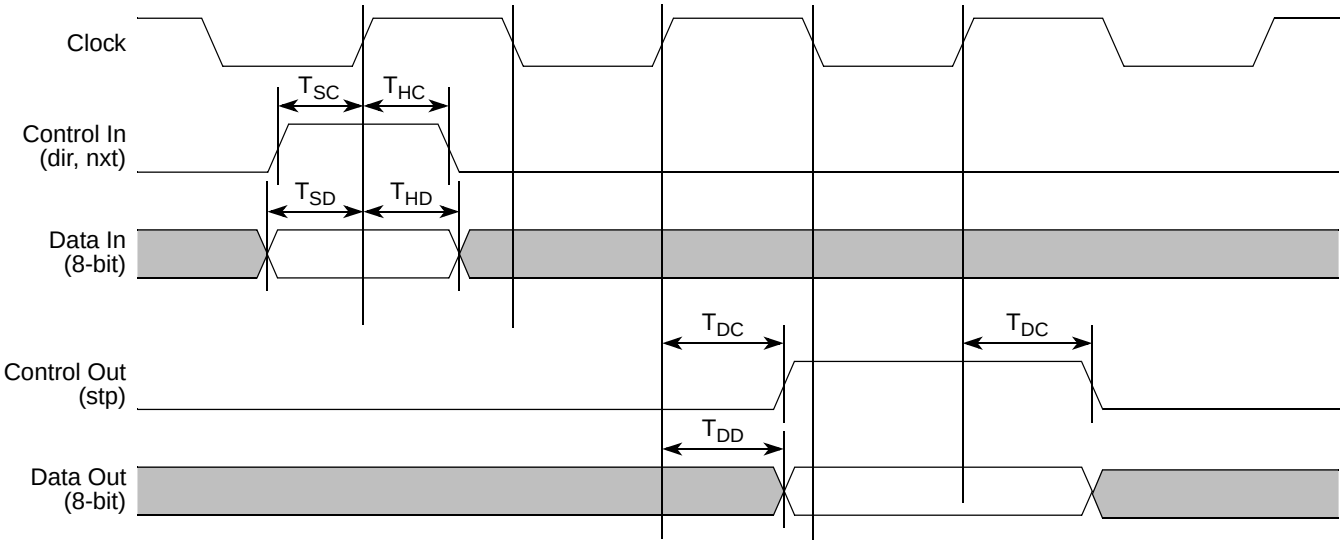

Figure 40. ULPI Timing Diagram

Table 36. Timing Specifications – ULPI

Symbol	Description	Min	Max	Units	SpecID
T_{CK}	Clock Period	15	—	ns	A12.1
T_{SC}, T_{SD}	Setup time (control in, 8-bit data in)	—	6.0	ns	A12.2
T_{HC}, T_{HD}	Hold time (control in, 8-bit data in)	0.0	—	ns	A12.3
T_{DC}, T_{DD}	Output delay (control out, 8-bit data out)	—	9.0	ns	A12.4

NOTE

Output timing is specified at a nominal 50 pF load.

3.3.13 On-Chip USB PHY

The USB PHY is an USB2.0 compatible PHY integrated on-chip. See Chapter 7 in the USB Specification Rev. 2.0 at www.usb.org.

3.3.14 SDHC

Figure 41 shows the timings of the SDHC.

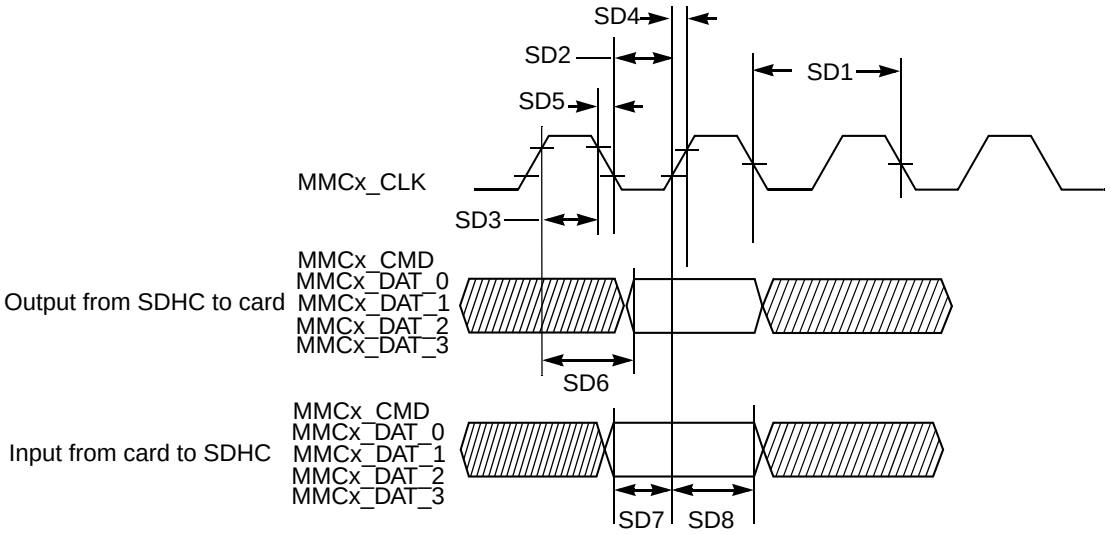

Figure 41. SDHC Timing Diagram

Table 37 lists the timing parameters.

Table 37. MMC/SD Interface Timing Parameters

ID	Parameter	Symbols	Min	Max	Unit	SpecID
Card Input Clock						
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz	A14.1
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz	A14.2
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz	A14.3
	Clock Frequency (Identification Mode)	f_{OD}[4]	100	400	kHz	A14.4
SD2	Clock Low Time (Full Speed/High Speed)	t_{WL}	10/7		ns	A14.5
SD3	Clock High Time (Full Speed/High Speed)	t_{WH}	10/7		ns	A14.6
SD4	Clock Rise Time (Full Speed/High Speed)	t_{TLH}		10/3	ns	A14.7
SD5	Clock Fall Time (Full Speed/High Speed)	t_{THL}		10/3	ns	A14.8
SDHC Output / Card Inputs CMD, DAT (Reference to CLK)						
SD6	SDHC Output Delay	t_{OD}	TH[5] – 3	TH+3	ns	A14.9
SDHC Input / Card Outputs CMD, DAT (Reference to CLK)						
SD7	SDHC Input Setup Time	t_{ISU}	2.5		ns	A14.10
SD8	SDHC Input Hold Time	t_{IH}	2.5		ns	A14.11

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal data transfer mode for SD/SDIO card, clock frequency can be any value between 0 ~ 25 MHz.

3 In normal data transfer mode for MMC card, clock frequency can be any value between 0 ~ 20 MHz.

4 In card identification mode, card clock must be 100 kHz ~ 400 kHz, voltage ranges from 2.7 to 3.6 V.

5 Suggested ClockPeriod = T, CLK_DIVIDER (in SDHC Clock Rate Register) = D, then TH = [(D + 1)/2]/(D + 1) × T where the value is rounded.

3.3.16 SPDIF

The Sony/Philips Digital Interface (SPDIF) timing is totally asynchronous, therefore there is no need for relationship with the clock.

3.3.17 CAN

The CAN functions are available as TX and CAN3/4_RX pins at normal IO pads and as CAN1/2 RX pins at the VBAT_RTC domain. There is no filter for the WakeUp dominant pulse. Any High-to-Low edge can cause WakeUp, if configured.

3.3.18 I^2C

This section specifies the timing parameters of the Inter-Integrated Circuit (I^2C) interface. Refer to the I^2C Bus Specification.

Table 40. I^2C Input Timing Specifications – SCL and SDA

Symbol	Description	Min	Max	Units	SpecID
1	Start condition hold time	2	—	IP-Bus Cycle[1]	A18.1
2	Clock low time	8	—	IP-Bus Cycle[1]	A18.2
4	Data hold time	0.0	—	ns	A18.3
6	Clock high time	4	—	IP-Bus Cycle[1]	A18.4
7	Data setup time	0.0	—	ns	A18.5
8	Start condition setup time (for repeated start condition only)	2	—	IP-Bus Cycle[1]	A18.6
9	Stop condition setup time	2	—	IP-Bus Cycle[1]	A18.7

1 Inter Peripheral Clock is defined in the MPC5121e/MPC5123 *Reference Manual*.

Table 41. I^2C Output Timing Specifications – SCL and SDA

Symbol	Description	Min	Max	Units	SpecID
1[1]	Start condition hold time	6	—	IP-Bus Cycle[2]	A18.8
2[1]	Clock low time	10	—	IP-Bus Cycle[2]	A18.9
3[3]	SCL/SDA rise time	—	7.9	ns	A18.10
4[1]	Data hold time	7	—	IP-Bus Cycle[2]	A18.11
5[1]	SCL/SDA fall time	—	7.9	ns	A18.12
6[1]	Clock high time	10	—	IP-Bus Cycle[2]	A18.13
7[1]	Data setup time	2	—	IP-Bus Cycle[2]	A18.14
8[1]	Start condition setup time (for repeated start condition only)	20	—	IP-Bus Cycle[2]	A18.15
9[1]	Stop condition setup time	10	—	IP-Bus Cycle[2]	A18.16

1 Programming IFDR with the maximum frequency results in the minimum output timings listed. The I^2C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.

2 Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Inter Peripheral Clock is defined in the *MPC5121e/MPC5123 Reference Manual.*

NOTE

Output timing is specified at a nominal 50 pF load.

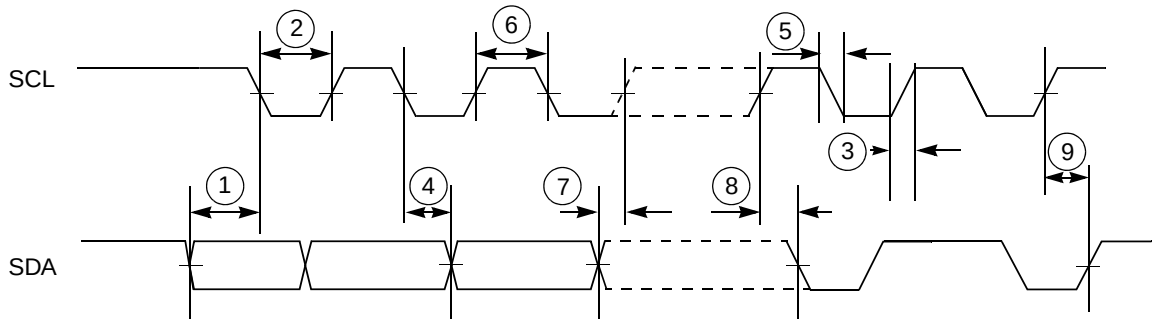

Figure 46. Timing Diagram – I²C Input/Output

3.3.19 J1850

See the MPC5121e/MPC5123 Reference Manual.

3.3.20 PSC

The Programmable Serial Controllers (PSC) support different modes of operation (UART, Codec, AC97, SPI). UART is an asynchronous interface, there is no AC characteristic.

3.3.20.1 Codec Mode (8,16,24 and 32-bit)/I²S Mode

Table 42. Timing Specifications – 8,16, 24, and 32-bit CODEC/I²S Master Mode

Symbol	Description	Min	Typ	Max	Units	SpecID
1	Bit Clock cycle time, programmed in CCS register	40.0	—	—	ns	A20.1
2	Clock duty cycle	45	50	55	%[1]	A20.2
3	Bit Clock fall time	—	—	7.9	ns	A20.3
4	Bit Clock rise time	—	—	7.9	ns	A20.4
5	FrameSync valid after clock edge	—	—	8.4	ns	A20.5
6	FrameSync invalid after clock edge	—	—	8.4	ns	A20.6
7	Output Data valid after clock edge	—	—	9.3	ns	A20.7
8	Input Data setup time	6.0	—	—	ns	A20.8

1 Bit Clock cycle time

NOTE

Output timing is specified at a nominal 50 pF load.

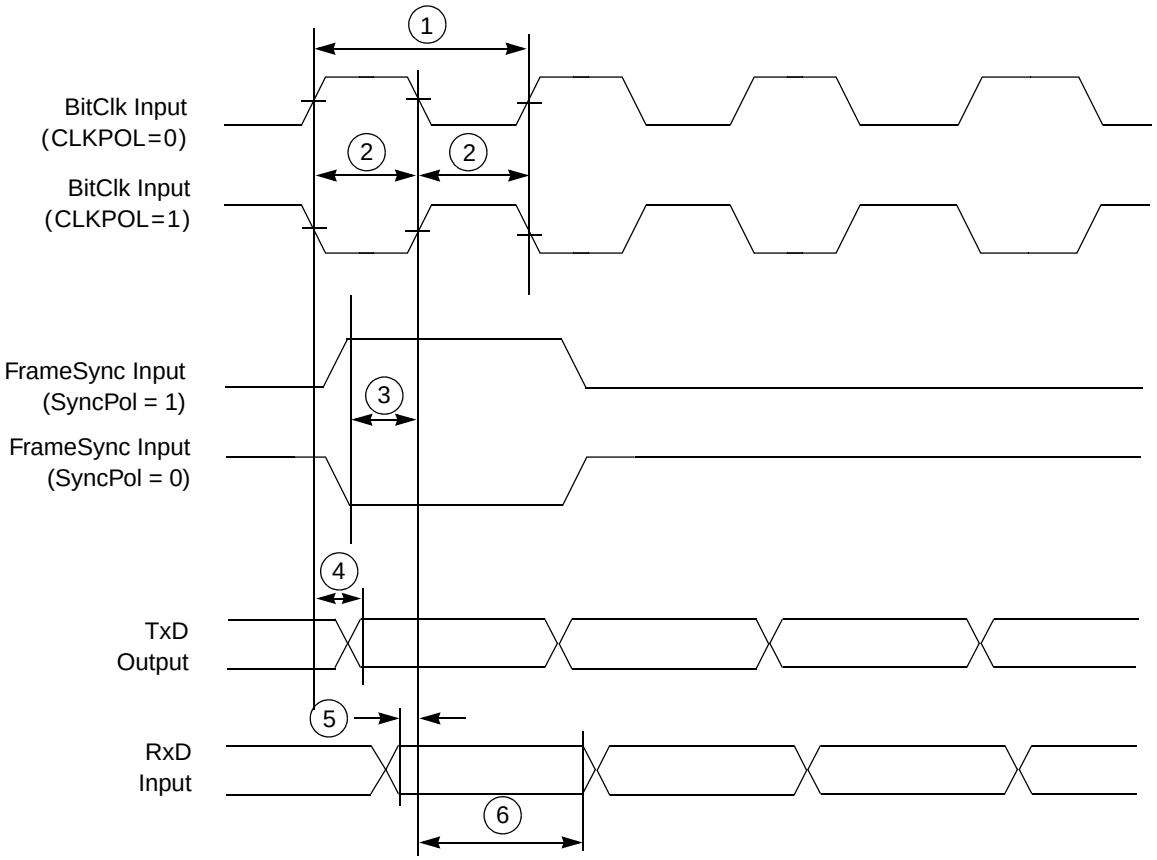

Figure 48. Timing Diagram – 8,16, 24, and 32-bit CODEC/I^{2}S Slave Mode

3.3.20.2 AC97 Mode

Table 44. Timing Specifications – AC97 Mode

Symbol	Description	Min	Typ	Max	Units	SpecID
1	Bit Clock cycle time	—	81.4	—	ns	A20.15
2	Clock pulse high time	—	40.7	—	ns	A20.16
3	Clock pulse low time	—	40.7	—	ns	A20.17
4	FrameSync valid after rising clock edge	—	—	13.0	ns	A20.18
5	Output Data valid after rising clock edge	—	—	14.0	ns	A20.19
6	Input Data setup time	1.0	—	—	ns	A20.20
7	Input Data hold time	1.0	—	—	ns	A20.21

NOTE

Output timing is specified at a nominal 50 pF load.

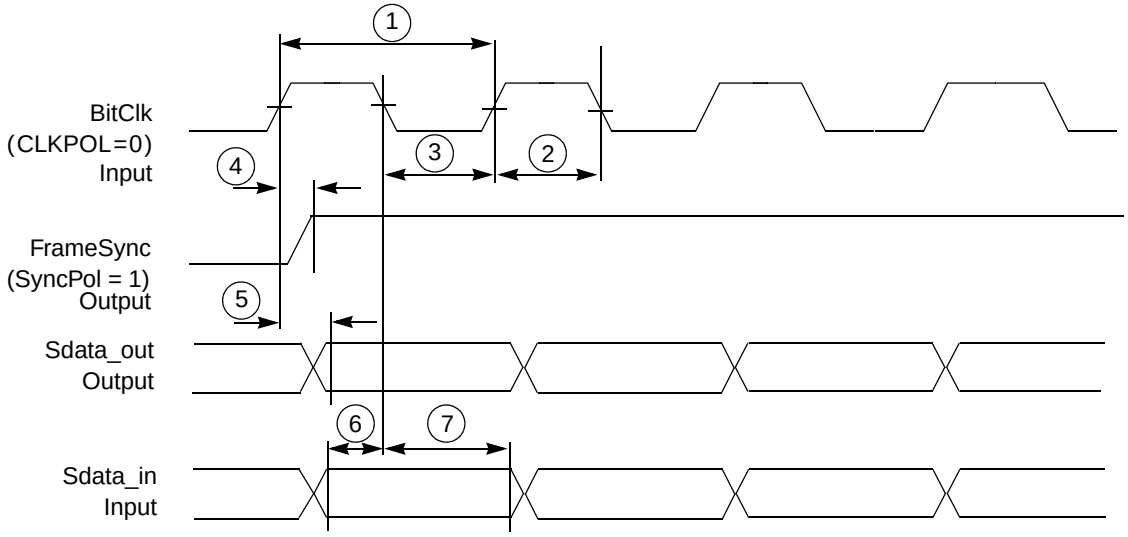

Figure 49. Timing Diagram – AC97 Mode

3.3.20.3 SPI Mode

Table 45. Timing Specifications – SPI Master Mode, Format 0 (CPHA = 0)

Symbol	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A20.26
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A20.27
3	Slave select clock delay, programable in the PSC CCS register	30.0	—	ns	A20.28
4	Output Data valid after Slave Select ($\overline{SS}$)	—	8.9	ns	A20.29
5	Output Data valid after SCK	—	8.9	ns	A20.30
6	Input Data setup time	6.0	—	ns	A20.31
7	Input Data hold time	1.0	—	ns	A20.32
8	Slave disable lag time	—	TSCK	ns	A20.33
9	Sequential Transfer delay, programmable in the PSC CTUR / CTLR register	15.0	—	ns	A20.34
10	Clock falling time	—	7.9	ns	A20.35
11	Clock rising time	—	7.9	ns	A20.36

NOTE

Output timing is specified at a nominal 50 pF load.

4 System Design Information

4.1 Power Up/Down Sequencing

Power sequencing between the 1.4 V power supply V_{DD_CORE} and the remaining supplies is required to prevent excessive current during power up phase.

The required power sequence is as follows:

- Use 12 V/millisecond or slower time for all supplies.
- Power up V_{DD_IO}, PLL_AV_{DD}, V_{BAT_RTC} (if not applied permanently), $V_{DD\_MEM\_IO}$, USB PHY, and SATA PHY supplies first in any order and then power up V_{DD_CORE}. If required, AV_{DD_FUSEWR} should be powered up afterwards.
- All the supplies must reach the specified operating conditions before the $\overline{\text{PORESET}}$ can be released.
- For power down, drop AV_{DD_FUSEWR} to 0 V first, drop V_{DD_CORE} to 0 V, and then drop all other supplies.
- V_{DD_CORE} should not exceed V_{DD_IO}, $V_{DD\_MEM\_IO}$, V_{BAT_RTC}, or PLL_AV_{DD}s by more than 0.4 V at any time, including power-up.

4.2 System and CPU Core AVDD Power Supply Filtering

Each of the independent PLL power supplies require filtering external to the device. The following drawing Figure 59 is a recommendation for the required filter circuit.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits.

All traces should be as low impedance as possible, especially ground pins to the ground plane.

The filter for System/Core $PLLV_{DD}$ to V_{SS} should be connected to the power and ground planes, respectively, not fingers of the planes.

In addition to keeping the filter components for System/Core $PLLV_{DD}$ as close as practical to the body of the MPC5121e as previously mentioned, special care should be taken to avoid coupling switching power supply noise or digital switching noise onto the portion of that supply between the filter and the MPC5121e.

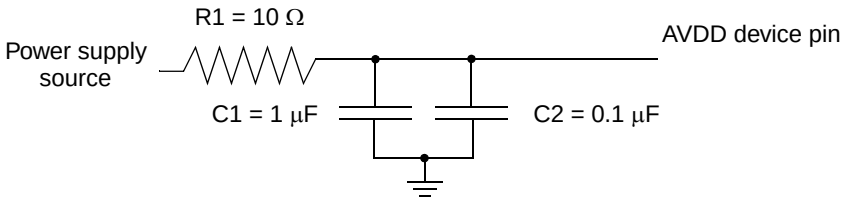

Figure 59. Power Supply Filtering

The capacitors for C2 in Figure 59 should be rated X5R or better due to temperature performance. It is recommended to add a bypass capacitance of at least 1 µF for the V_{BAT_RTC} pin.

4.3 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to V_{DD_IO}. Unused active high inputs should be connected to V_{SS}. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} and V_{SS} pins of the MPC5121e/MPC5123.

The unused AV_{DD_FUSEWR} power should be connected to V_{SS} directly or via a resistor.

For DDR or LPDDR modes the unused pins MVTT[3:0] for DDR2 Termination voltage can be unconnected.

6 Product Documentation

This Data Sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com.

Table 55 provides a revision history for this document.

Table 55. Document Revision History

Revision	Substantive Change(s)
Rev. 0, DraftA	First Draft (5/2008)
Rev. 0, DraftB	Second Draft (5/2008)
Rev. 0, DraftC	Third Draft (7/2008)
Rev. 1	Advance Information (10/2008)
Rev. 2	Technical Data (2/2009)
Rev. 3	Technical Data (2/2009). Corrected Table 5, Footnote 3.
Rev. 3.1	Technical Data (12/2009). Interim release for removing AVDD_FUSERD throughout document, changing pin D9 to VDD_IO, and adding D9 to list of pins for VDD_IO.
Rev. 4	Technical Data (1/2010). Minor editorial and graphical updates. No technical updates.
Rev 5	— Updated table “DDR and DDR2 SDRAM Timing Specification”, removed the row of ‘MCK AC differential crosspoint voltage' . — Updated table “Thermal Resistance Data”. — Added table “NFC Timing Characteristics in Symmetric Mode ”and added figure “Read data latch timing in Symmetric Mode”. —Published as Rev. 5