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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	e300
Core Size	32-Bit Single-Core
Speed	400MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, USB OTG
Peripherals	DMA, WDT
Number of I/O	147
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc5121yvy400b

Figure 1 shows a simplified MPC5121e/MPC5123 block diagram.

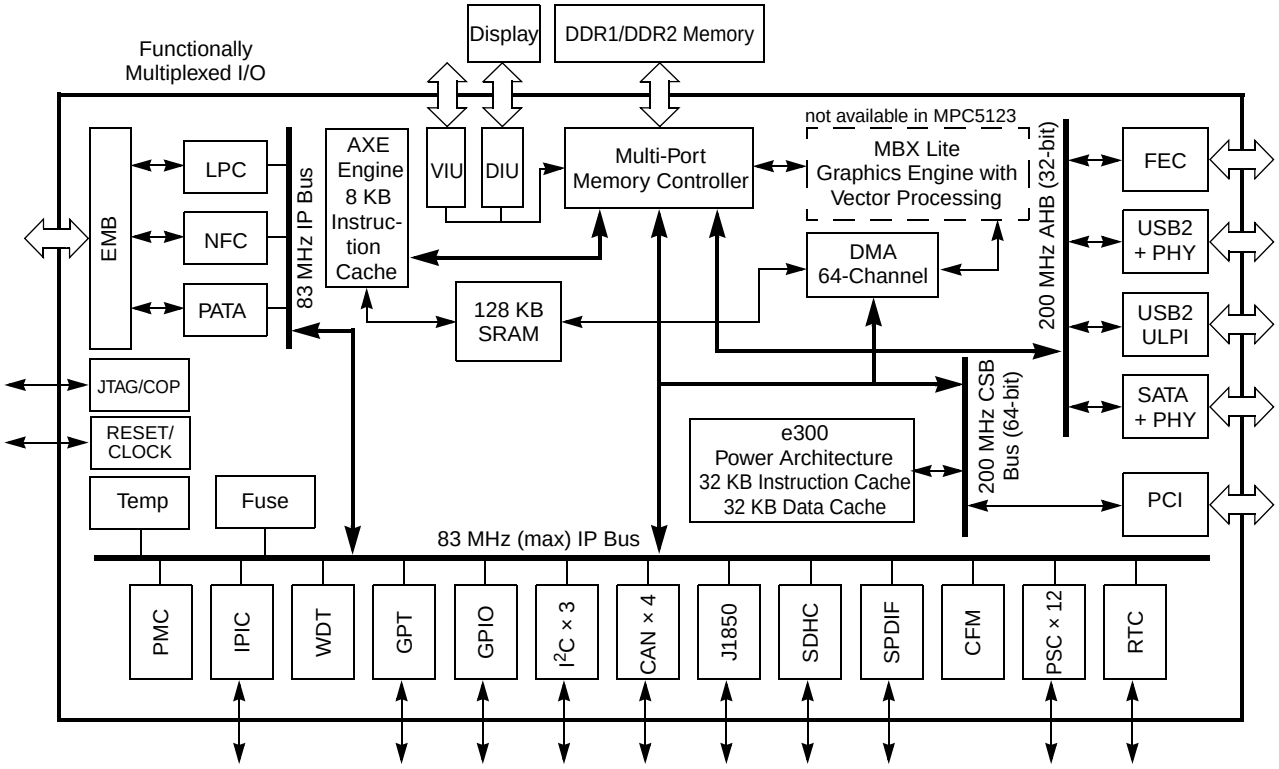

Figure 1. Simplified MPC5121e/MPC5123 Block Diagram

1 Ordering Information

Table 1. MPC5121e Orderable Part Numbers

Freescale Part Number	Speed (MHz)	Temperature (ambient)	Qualification	Package	Availability
MPC5121VY400B	400	0 °C to 70 °C	Consumer	RoHS and Pb-free	Tray
MPC5121VY400BR	400	0 °C to 70 °C	Consumer	RoHS and Pb-free	Tape and Reel
MPC5121YVY400B	400	–40 °C to 85 °C	Industrial	RoHS and Pb-free	Tray
MPC5121YVY400BR	400	–40 °C to 85 °C	Industrial	RoHS and Pb-free	Tape and Reel
SPC5121YVY400B	400	–40 °C to 85 °C	Automotive—AEC	RoHS and Pb-free	Tray
SPC5121YVY400BR	400	–40 °C to 85 °C	Automotive—AEC	RoHS and Pb-free	Tape and Reel

Table 2. MPC5123 Orderable Part Numbers

Freescale Part Number	Speed (MHz)	Temperature (ambient)	Qualification	Package	Availability
MPC5123VY400B	400	0 °C to 70 °C	Consumer	RoHS and Pb-free	Tray
MPC5123VY400BR	400	0 °C to 70 °C	Consumer	RoHS and Pb-free	Tape and Reel
MPC5123YVY400B	400	–40 °C to 85 °C	Industrial	RoHS and Pb-free	Tray

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 4 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
EMB_AD11	P3	General IO	V_{DD_IO}	—
EMB_AD10	N1	General IO	V_{DD_IO}	—
EMB_AD09	N2	General IO	V_{DD_IO}	—
EMB_AD08	N3	General IO	V_{DD_IO}	—
EMB_AD07	N4	General IO	V_{DD_IO}	—
EMB_AD06	M1	General IO	V_{DD_IO}	—
EMB_AD05	M3	General IO	V_{DD_IO}	—
EMB_AD04	M5	General IO	V_{DD_IO}	—
EMB_AD03	L1	General IO	V_{DD_IO}	—
EMB_AD02	L2	General IO	V_{DD_IO}	—
EMB_AD01	L3	General IO	V_{DD_IO}	—
EMB_AD00	L4	General IO	V_{DD_IO}	—
PATA Interface (9 Total)				
$\overline{\text{PATA\_CE1}}$	K1	General IO	V_{DD_IO}	ATA name: CS0
$\overline{\text{PATA\_CE2}}$	L5	General IO	V_{DD_IO}	ATA name: CS1
PATA_ISOLATE	K3	General IO	V_{DD_IO}	—
$\overline{\text{PATA\_IOR}}$	J1	General IO	V_{DD_IO}	ATA name: DIOR
$\overline{\text{PATA\_IOW}}$	K5	General IO	V_{DD_IO}	ATA name: DIOW
PATA_IOCHRDY	J2	General IO	V_{DD_IO}	ATA name: IORDY
PATA_INTRQ	J3	General IO	V_{DD_IO}	—
PATA_DRQ	J4	General IO	V_{DD_IO}	ATA name: DMARQ
$\overline{\text{PATA\_DACK}}$	H2	General IO	V_{DD_IO}	ATA name: DMACK
NFC Interface (7 Total)				
$\overline{\text{NFC\_WP}}$	G4	General IO	V_{DD_IO}	—
NFC_R/$\overline{\text{B}}$	H1	General IO	V_{DD_IO}	—
$\overline{\text{NFC\_WE}}$	G3	General IO	V_{DD_IO}	—
$\overline{\text{NFC\_RE}}$	G2	General IO	V_{DD_IO}	—
NFC_ALE	H4	General IO	V_{DD_IO}	—
NFC_CLE	H5	General IO	V_{DD_IO}	—
$\overline{\text{NFC\_CE0}}$	H3	General IO	V_{DD_IO}	—
I2C Interface (6 Total)				
I2C0_SCL	AC23	General IO	V_{DD_IO}	—
I2C0_SDA	AD26	General IO	V_{DD_IO}	—
I2C1_SCL	AB22	General IO	V_{DD_IO}	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 9 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
TDI	Y23	General IO	V_{DD_IO}	3
TDO	W22	General IO	V_{DD_IO}	—
TMS	Y25	General IO	V_{DD_IO}	3
$\overline{\text{TRST}}$	AA26	General IO	V_{DD_IO}	3
Test / Debug (2 Total)				
TEST	W25	General IO	V_{DD_IO}	4, 5
$\overline{\text{CKSTP\_OUT}}$	Y26	General IO	V_{DD_IO}	—
System Control (3 Total)				
$\overline{\text{HRESET}}$	W24	General IO	V_{DD_IO}	6, 2
$\overline{\text{PORESET}}$	W23	General IO	V_{DD_IO}	4, 2
$\overline{\text{SRESET}}$	V22	General IO	V_{DD_IO}	6, 2
System Clock (2 Total)				
SYS_XTALI	V24	Analog Input	SYS_PLL_AVDD	Oscillator Input
SYS_XTALO	W26	Analog Output	SYS_PLL_AVDD	Oscillator Output
RTC (3 Total)				
RTC_XTALI	C20	Analog Input	VBAT_RTC	Oscillator Input
RTC_XTALO	A20	Analog Output	VBAT_RTC	Oscillator Output
$\overline{\text{HIB\_MODE}}$	D18	Analog Output	VBAT_RTC	—
GP Input Only (4 Total)				
GPIO28	A19	Analog Input	VBAT_RTC	—
GPIO29	E17	Analog Input	VBAT_RTC	—
GPIO30	C18	Analog Input	VBAT_RTC	—
GPIO31	B18	Analog Input	VBAT_RTC	—
DDR Reference Voltage				
MVREF	AB11	Analog Input	Voltage Reference for SSTL input pads	
USB – PHY without Power and Ground Supplies (7 Total)				
USB_XTALI	C24	Analog Input	USB_PLL_PWR3	Oscillator Input
USB_XTALO	B24	Analog Output	USB_PLL_PWR3	Oscillator Output
USB_DP	A23	Analog IO	USB_VDDA	—
USB_DM	A22	Analog IO	USB_VDDA	—
USB_TPA	A24	Analog Output	—	USB PHY debug output
USB_VBUS	D21	Analog IO	—	—

Table 6. DC Electrical Specifications (continued)

Characteristic	Condition	Symbol	Min	Max	Unit	SpecID
Input leakage current	RTC_XTALI Vin = 0 or V_{DD_IO}	I_{IN}	—	1.0	µA	D3.23
Input current, pullup resistor[6]	Pullup V_{DD_IO} Vin = VIL	I_{INpu}	25	150	µA	D3.24
Input current, pulldown resistor [8]	Pulldown V_{DD_IO} Vin = VIH	I_{INpd}	25	150	µA	D3.25
Output high voltage	IOH is driver dependent[7] V_{DD_IO}	V_{OH}	0.8 × V_{DD_IO}	—	V	D3.26
Output high voltage	IOH is driver dependent[7] $V_{DD\_MEM\_IO\_DDR}$	V_{OHDDR}	1.90	—	V	D3.27
Output high voltage	IOH is driver dependent[7] $V_{DD\_MEM\_IO\_DDR2}$	V_{OHDDR2}	1.396	—	V	D3.28
Output high voltage	IOH is driver dependent[7] $V_{DD\_MEM\_IO\_LPDDR}$	$V_{OHLPDDR}$	$V_{DD\_MEM\_IO}$ – 0.28	—	V	D3.28
Output low voltage	IOL is driver dependent[7] V_{DD_IO}	V_{OL}	—	0.2 × V_{DD_IO}	V	D3.30
Output low voltage	IOL is driver dependent[7] $V_{DD\_MEM\_IO\_DDR}$	V_{OLDDR}	—	0.36	V	D3.31
Output low voltage	IOL is driver dependent[7] $V_{DD\_MEM\_IO\_DDR2}$	V_{OLDDR2}	—	0.28	V	D3.32
Output low voltage	IOL is driver dependent[7] $V_{DD\_MEM\_IO\_LPDDR}$	$V_{OLLPDDR}$	—	0.28	V	D3.33
Differential cross point voltage (DDR MCK/$\overline{\text{MCK}}$)	—	V_{OXMCK}	0.5 × $V_{DD\_MEM\_IO}$ – 0.125	0.5 × $V_{DD\_MEM\_IO}$ + 0.125	V	D3.34
DC Injection Current Per Pin[8]	—	I_{CS}	–1.0	1.0	mA	D3.35
Input Capacitance (digital pins)	—	C_{in}	—	7	pF	D3.36
Input Capacitance (analog pins)	—	C_{in}	—	10	pF	D3.37
On Die Termination (DDR2)	—	R_{ODT}	120	180	Ω	D3.38

1 This parameter is meant for those who do not use quartz crystals or resonators, but CAN osc, in crystal mode. In that case, Vextal – Vxtal - 400mV criteria has to be met for oscillator's comparator to produce output clock.

2 This parameter is meant for those who do not use quartz crystals or resonators, but signal generator clock to drive, in bypass mode. In that case, drive only the EXTAL pin not connecting anything to other pin for the oscillator's comparator to produce output clock.

3 This parameter is meant for those who do not use quartz crystals or resonators, but CAN osc, in crystal mode. In that case, drive one of the XTAL_IN or XTAL_OUT pins not connecting anything to other pin for the oscillator's comparator to produce output clock.

4 This parameter is meant for those who do not use quartz crystals or resonators, but signal generator clock to drive, in bypass mode. In that case, drive only the xtal_in pin not connecting anything to other pin for the oscillator's comparator to produce output clock.

5 Leakage current is measured with output drivers disabled and pull-up/pull-downs inactive.

6 Pullup current is measured at VIL and pulldown current is measured at VIH.

3.1.4 Electrostatic Discharge

This device contains circuitry that protects against damage due to high-static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages. Operational reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (GND or VDD). Table 10 gives package thermal characteristics for this device.

Table 8. ESD and Latch-Up Protection Characteristics

Symbol	Rating	Min	Max	Unit	SpecID
V_{HBM}	Human Body Model (HBM) – JEDEC JESD22-A114-B	2000	—	V	D4.1
V_{MM}	Machine Model (MM) – JEDEC JESD22-A115	200	—	V	D4.2
V_{CDM}	Charge Device Model (CDM) – JEDEC JESD22-C101	500	—	V	D4.3

3.1.5 Power Dissipation

Power dissipation of the MPC5121e/MPC5123 is caused by 4 different components: the dissipation of the internal or core digital logic (supplied by $V_{DD\_CORE)}$, the dissipation of the analog circuitry (supplied by SYS_PLL_AVDD and CORE_PLL_AVDD), the dissipation of the IO logic (supplied by $V_{DD\_MEM\_IO}$ and V_{DD_IO}) and the dissipation of the PHYs (supplied by own supplies). Table 9 details typical measured core and analog power dissipation figures for a range of operating modes. However, the dissipation due to the switching of the IO pins can not be given in general, but must be calculated for each application case using the following formula:

$$P_{IO} = P_{IOint} + \sum_{M} N \times C \times VDD\_IO^2 \times f \qquad \textit{Eqn. 1}$$

where N is the number of output pins switching in a group M, C is the capacitance per pin, V_{DD_IO} is the IO voltage swing, f is the switching frequency and P_{IOint} is the power consumed by the unloaded IO stage. The total power consumption of the device must not exceed the value that would cause the maximum junction temperature to be exceeded.

$$P_{total} = P_{core} + P_{analog} + P_{IO} + PPHYs \qquad \textit{Eqn. 2}$$

Table 9. Power Dissipation

Core Power Supply (V_{DD_CORE})			SpecID
Mode	High-Performance	Unit	
	e300 = 300 MHz, CSB = 200 MHz		
Operational[1]	800	mW	D5.1
Deep-Sleep[1]	1	mW	D5.2
Hibernation	20	uW	D5.3
PLL/OSC Power Supplies (SYS_PLL_AVDD, CORE_PLL_AVDD)			
Typical	25	mW	D5.4
Unloaded I/O Power Supplies (V_{DD_IO}, $V_{DD\_MEM\_IO}$)			

4 Fall time is measured from 20% of vdd to 80% of V_{DD}.
5 SYS_XTALI duty cycle is measured at V_M.

3.2.2 RTC Oscillator Electrical Characteristics

Table 13. RTC Oscillator Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit	SpecID
RTC_XTALI frequency	f_{rtc_xtal}	—	32.768	—	kHz	O2.1

3.2.3 System PLL Electrical Characteristics

Table 14. System PLL Specifications

Characteristic	Symbol	Min	Typical	Max	Unit	SpecID
Sys PLL input clock frequency[1]	f_{sys_xtal}	16	33.3	67	MHz	O3.1
Sys PLL input clock jitter[2]	t_{jitter}	—	—	10	ps	O3.2
Sys PLL VCO frequency[1]	f_{VCOsys}	400	—	800	MHz	O3.3
Sys PLL VCO output jitter (Dj), peak to peak / cycle	$f_{VCOjitterDj}$	—	—	40	ps	O3.4
Sys PLL VCO output jitter (Rj), RMS 1 sigma	$f_{VCOjitterRj}$	—	—	12	ps	O3.5
Sys PLL relock time—after power up[3]	t_{lock1}	—	—	200	µs	O3.6
Sys PLL relock time—when power was on[4]	t_{lock2}	—	—	170	µs	O3.7

1 The SYS_XTALI frequency and PLL Configuration bits must be chosen such that the resulting system frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
2 This represents total input jitter—short term and long term combined. Two different types of jitter can exist on the input to CORE_SYSCLK, systemic and true random jitter. True random jitter is rejected. Systemic jitter is passed into and through the PLL to the internal clock circuitry.
3 PLL relock time is the maximum amount of time required for the PLL lock after a stable VDD and CORE_SYSCLK are reached during the power-on reset sequence.
4 PLL relock time is the maximum amount of time required for the PLL lock after the PLL has been disabled and subsequently re-enabled during sleep modes.

3.2.4 e300 Core PLL Electrical Characteristics

The internal clocking of the e300 core is generated from and synchronized to the system clock by means of a voltage-controlled core PLL.

Table 15. e300 PLL Specifications

Characteristic	Symbol	Min	Typical	Max	Unit	SpecID
e300 frequency[1]	f_{core}	200	—	400	MHz	O4.1
e300 PLL VCO frequency[1]	$f_{VCOcore}$	400	—	800	MHz	O4.3
e300 PLL input clock frequency	f_{CSB_CLK}	50	—	200	MHz	O4.4
e300 PLL input clock cycle time	t_{CSB_CLK}	5	—	20	ns	O4.5
e300 PLL relock time[2]	t_{lock}	—	—	200	µs	O4.6

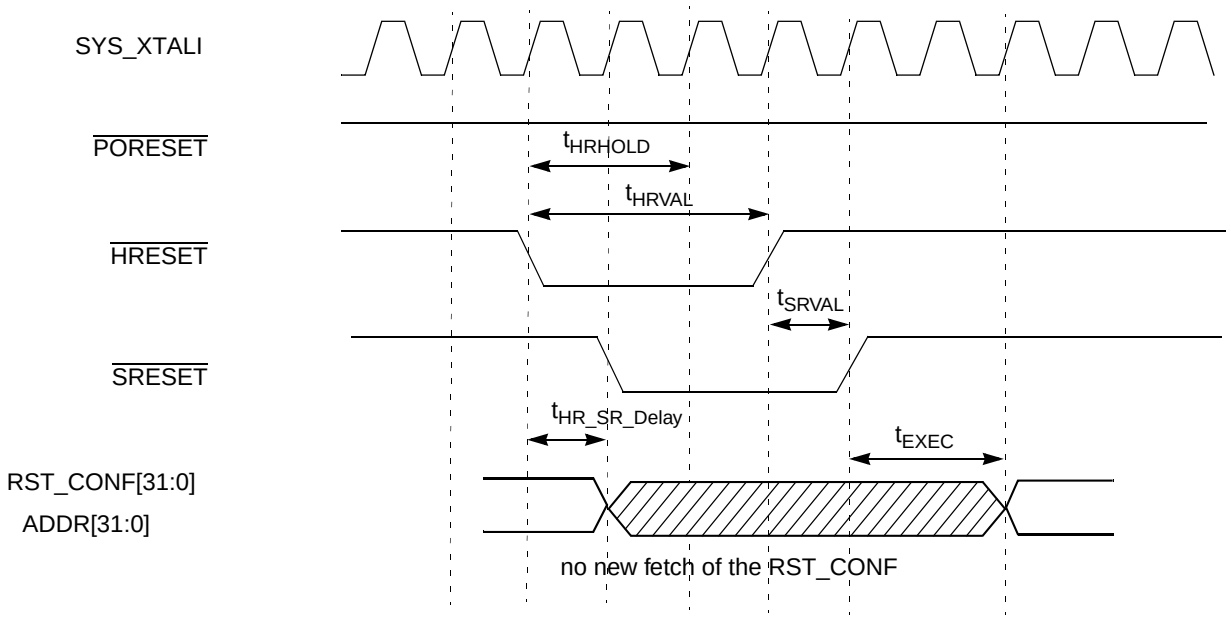

Figure 6. HRESET Behavior

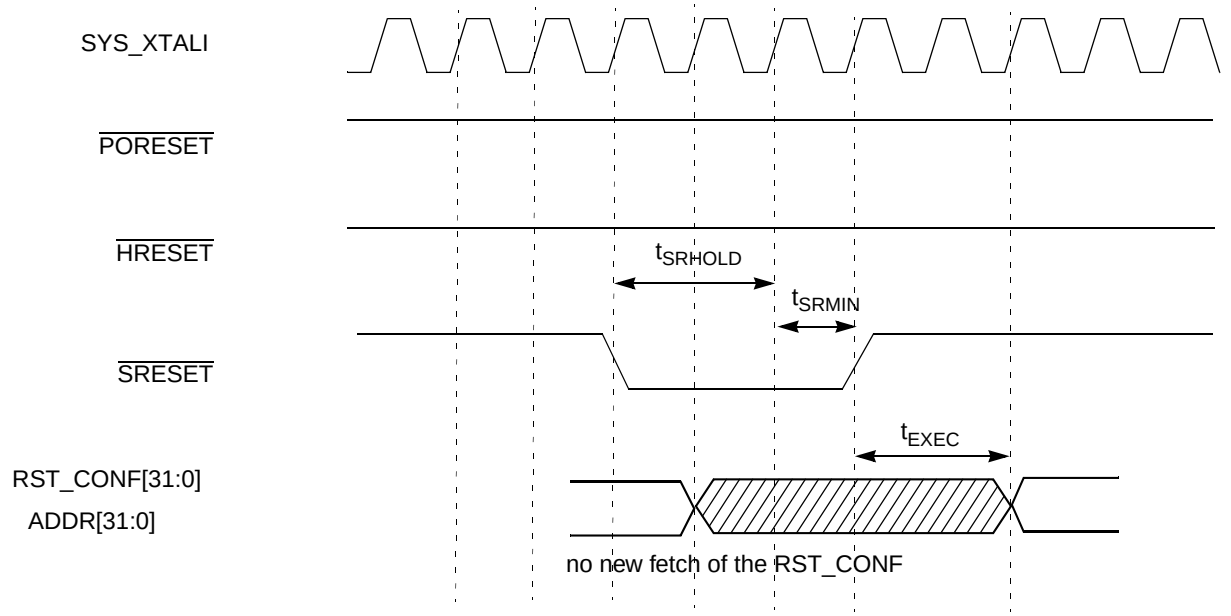

Figure 7. SRESET Behavior

Table 18. Reset Timing

Symbol	Description	Value SYS_XTALI	SpecID
$t_{PORHOLD}$	Time $\overline{\text{PORESET}}$ must be held low before a qualified reset occurs	4 cycles	A3.10
t_{HRVAL}	Time $\overline{\text{HRESET}}$ is asserted after a qualified reset occurs	26810 cycles	A3.11
t_{SRVAL}	Time $\overline{\text{SRESET}}$ is asserted after assertion of $\overline{\text{HRESET}}$	32 cycles	A3.12
t_{EXEC}	Time between $\overline{\text{SRESET}}$ assertion and first core instruction fetch	4 cycles	A3.13

3.3.5.1 DDR and DDR2 SDRAM AC Timing Specifications

Table 20. DDR and DDR2 (DDR2-400) SDRAM Timing Specifications

At recommended operating conditions with $V_{DD\_MEM\_IO}$ of ±5%

Parameter	Symbol	Min	Max	Unit	Notes	SpecID
Clock cycle time, CL=x	t_{CK}	5000	—	ps		A5.1
CK HIGH pulse width	t_{CH}	0.47	0.53	t_{CK}	1,2	A5.3
CK LOW pulse width	t_{CL}	0.47	0.53	t_{CK}	1,2	A5.4
Skew between MCK and DQS transitions	t_{DQSS}	–0.25	0.25	t_{CK}	2, 3	A5.5
Address and control output setup time relative to MCK rising edge	$t_{OS(base)}$	(t_{CK}/2 – 750)	—	ps	2, 3	A5.6
Address and control output hold time relative to MCK rising edge	$t_{OH(base)}$	(t_{CK}/2 – 750)	—	ps	2, 3	A5.7
DQ and DM output setup time relative to DQS	$t_{DS1(base)}$	(t_{CK}/4 – 500)	—	ps	2, 3	A5.8
DQ and DM output hold time relative to DQS	$t_{DH1(base)}$	(t_{CK}/4 – 500)	—	ps	2, 3	A5.9
DQS-DQ skew for DQS and associated DQ inputs	t_{DQSQ}	–(t_{CK}/4 – 600)	(t_{CK}/4 – 600)	ps	2	A5.10
DQS window start position related to CAS read command	t_{DQSEN}	TBD	TBD	ps	1,2,3,4,5	A5.11

1 Measured with clock pin loaded with differential 100 termination resistor.

2 All transitions measured at mid-supply (VDD_MEM_IO/2).

3 Measured with all outputs except the clock loaded with 50 Ω termination resistor to $V_{DD\_MEM\_IO}$/2.

4 In this window, the first rising edge of DQS should occur. From the start of the window to DQS rising edge, DQS should be low.

5 Window position is given for t_{DQSEN} = 2.0 t_{CK}. For other values of t_{DQSEN}, window position is shifted accordingly.

Figure 8 shows the DDR SDRAM write timing.

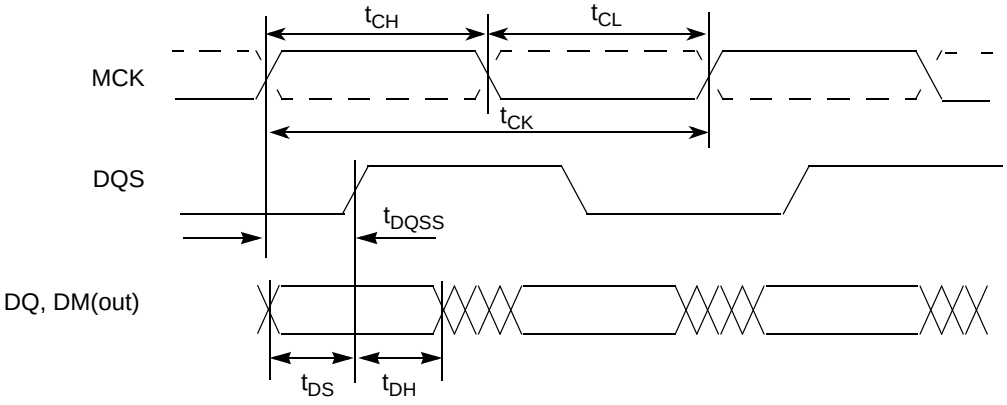

Figure 8. DDR Write Timing

Figure 9 and Figure 10 shows the DDR SDRAM read timing.

3.3.7.2 MUXed Mode

3.3.7.2.1 MUXed Non-Burst Mode

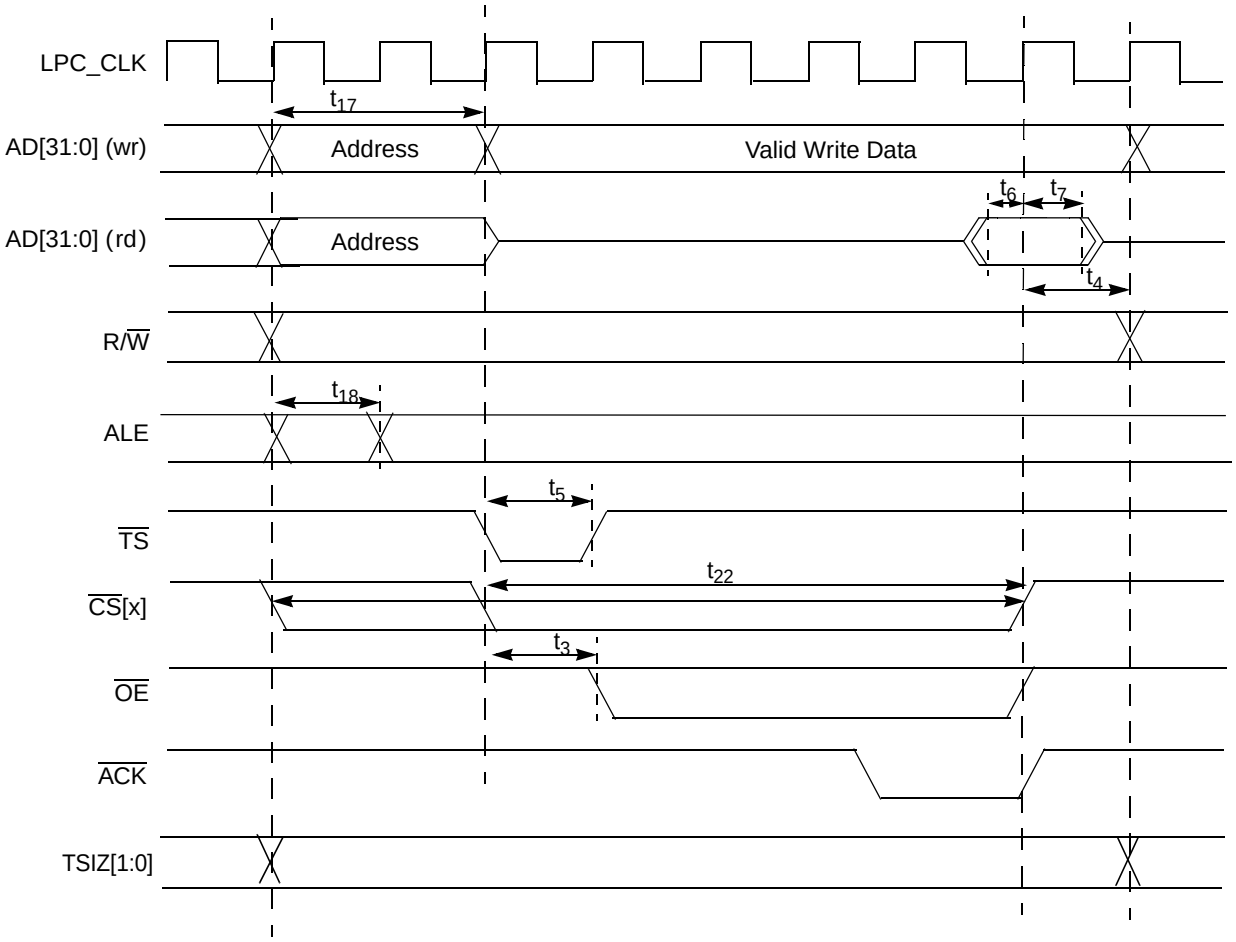

Figure 18. Timing Diagram – MUXed Non-Burst Mode

NOTE

$\overline{\text{ACK}}$ is asynchonous input signal and has no timing requirements. $\overline{\text{ACK}}$ needs to be deasserted after $\overline{\text{CS}}$[x] is deasserted.

Table 25. NFC Timing Characteristics in Symmetric mode(SYM=1)[1]

Timing Parameter	Description	Min. value	Max. value	Unit	SpecID
t_{CLS}	NFC_CLE Setup time	T	—	ns	A8.21
t_{CLH}	NFC_CLE Hold time	T	—	ns	A8.22
t_{CS}	NFC_CE[1:0] Setup time	T-2	—	ns	A8.23
t_{CH}	NFC_CE[1:0] Hold time	1.5T-1	—	ns	A8.24
t_{WP}	NFC_WE Pulse width	0.5T+1	—	ns	A8.25
t_{ALS}	NFC_ALE Setup time	T	—	ns	A8.26
t_{ALH}	NFC_ALE Hold time	T	—	ns	A8.27
t_{DS}	Data Setup time	0.5T-3	—	ns	A8.28
t_{DH}	Data Hold time	0.5T	—	ns	A8.29
t_{WC}	Write Cycle time	T	—	ns	A8.30
t_{WH}	NFC_WE Hold time	0.5T-1	—	ns	A8.31
t_{RR}	Ready to NFC_RE low	5T+2	—	ns	A8.32
t_{RP}	NFC_RE pulse width	0.5T	—	ns	A8.33
t_{RC}	Read Cycle time	T	—	ns	A8.34
t_{REH}	NFC_RE High hold time	0.5T	—	ns	A8.35
t_{SS}	NFC Read Data setup time	9.6	—	ns	A8.36

1 T is the flash clock cycle.
T = 45 ns, frequency = 22 MHz (boot configuration, IP bus = 66 MHz)
T = 36 ns, frequency = 27 MHz (maximum configurable frequency, IP bus = 83 MHz)

3.3.9 PATA

The MPC5121e/MPC5123 ATA Controller (PATA) is completely software programmable. It can be programmed to operate with ATA protocols using their respective timing, as described in the ANSI ATA-4 specification. The ATA interface is completely asynchronous in nature. Signal relationships are based on specific fixed timing in terms of timing units (nanoseconds).

ATA data setup and hold times, with respect to Read/Write strobes, are software programmable inside the ATA Controller. Data setup and hold times are implemented using counters. The counters count the number of ATA clock cycles needed to meet the ANSI ATA-4 timing specifications. For details, see the ANSI ATA-4 specification and how to program an ATA Controller and ATA drive for different ATA protocols and their respective timing. See the *MPC5121e Microcontroller Reference Manual*.

The MPC5121e/MPC5123 ATA Host Controller design makes data available coincidentally with the active edge of the WRITE strobe in PIO and Multiword DMA modes.

- Write data is latched by the drive at the inactive edge of the WRITE strobe. This gives ample setup-time beyond that required by the ATA-4 specification.
- Data is held unchanged until the next active edge of the WRITE strobe. This gives ample hold-time beyond that required by the ATA-4 specification.

Table 3-27. Timing Parameters PIO Read (continued)

ATA Parameter	PIO Read Mode Timing Parameter	Value	How to meet	SpecID
t_5	t_5	$t_5(min) = t_{co} + t_{su} + t_{buf} + t_{buf} + t_{cable1} + t_{cable2}$	If not met, increase time_2r	A9.23
t_6	t_6	0	—	A9.24
t_A	t_A	$t_{A(min)} = (1.5 + time\_ax) \times T - (t_{co} + t_{sui} + t_{cable2} + t_{cable2} + 2 \times t_{buf})$	calculate and programming time_ax. [1]	A9.25
t_{rd}	t_{rd1}	$t_{rd1(max)} = (-t_{rd}) + (t_{skew3} + t_{skew4})$ $t_{rd1(min)} = (time\_pio\_rdx - 0.5) \times T - (t_{su} + t_{hi})$ $(time\_pio\_rdx - 0.5) \times T > t_{su} + t_{hi} + t_{skew3} + t_{skew4}$	calculate and programming time_pio_rdx. [1]	A9.26
t_0	—	$t_{0(min)} = (time\_1 + time\_2 + time\_9) \times T$	time_1, time_2r, time_9	A9.27

1 See the *MPC5121e Microcontroller Reference Manual.*

In PIO write mode, timing waveforms are somewhat different as shown in Figure 27.

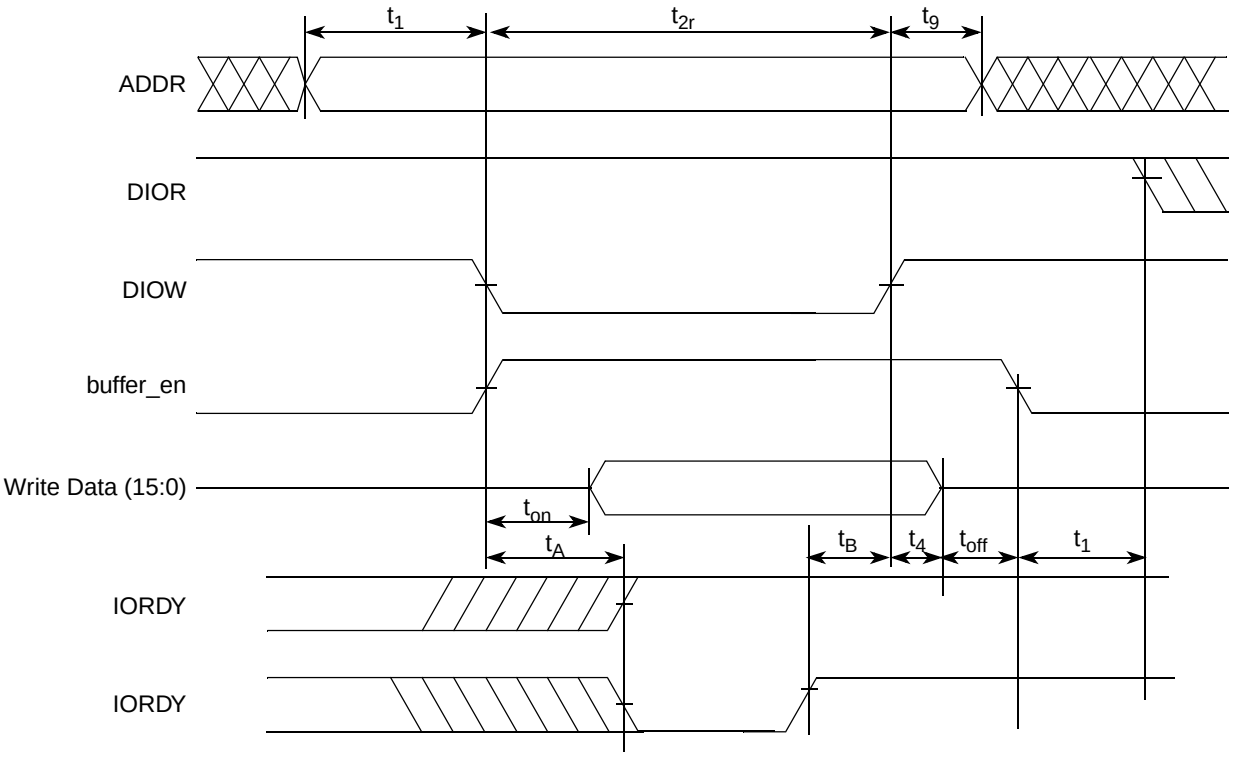

Figure 27. PIO Write Mode Timing

To fulfill this timing, several parameters need to be observed as shown in Table 3-28.

3.3.9.3 Timing in Multiword DMA Mode

Timing in multiword DMA mode is given in Figure 28 and Figure 29.

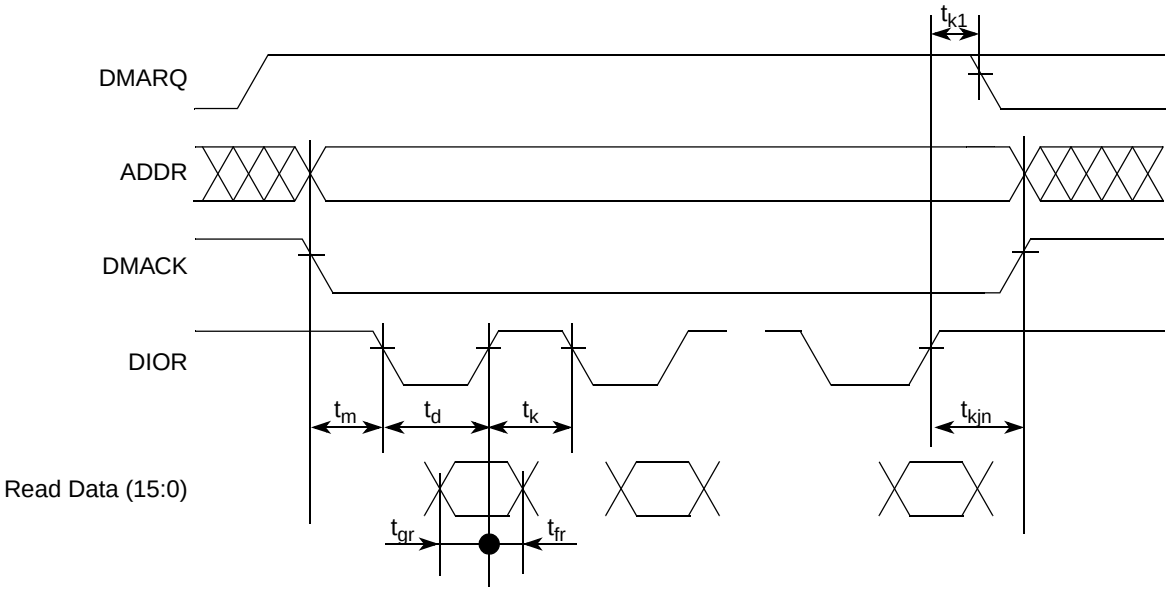

Figure 28. MDMA Read Timing

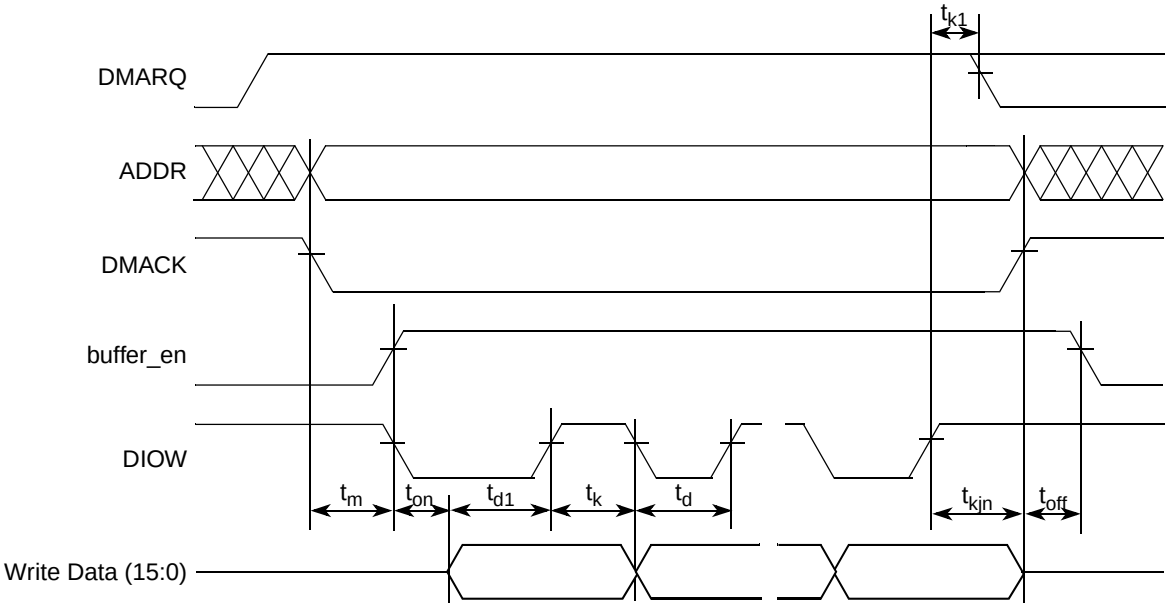

Figure 29. MDMA Write Timing

To meet this timing, a number of timing parameters must be controlled as shown in Table 3-29.

Table 31. Timing Parameters UDMA Out Burst (continued)

ATA Parameter	UDMA Out Timing Parameter	Value	How to meet	SpecID
t_{li}	t_{li2}	$t_{li2} > 0$	—	A9.74
t_{li}	t_{li3}	$t_{li3} > 0$	—	A9.75
t_{cvh}	t_{cvh}	$t_{cvh} = (time\_cvh \times T) - (t_{skew1} + t_{skew2})$	calculate and program time_cvh. [1]	A9.76
—	t_{on} t_{off}	$t_{on} = time\_on \times T - t_{skew1}$ $t_{off} = time\_off \times T - t_{skew1}$	—	A9.77

1 See the *MPC5121e Microcontroller Reference Manual.*

3.3.10 SATA PHY

1.5 Gbps SATA PHY Layer

See “Serial ATA: High Speed Serialized AT Attachment” Revision 1.0a, 7-January-2003.

3.3.11 FEC

AC Test Timing Conditions:

- Output Loading
  All Outputs: 25 pF

Table 32. MII Rx Signal Timing

Symbol	Description	Min	Max	Unit	SpecID
1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns	A11.1
2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns	A11.2
3	RX_CLK pulse width high	35%	65%	RX_CLK Period[1]	A11.3
4	RX_CLK pulse width low	35%	65%	RX_CLK Period[1]	A11.4

1 RX_CLK shall have a frequency of 25% of data rate of the received signal. See the IEEE 802.3 Specification.

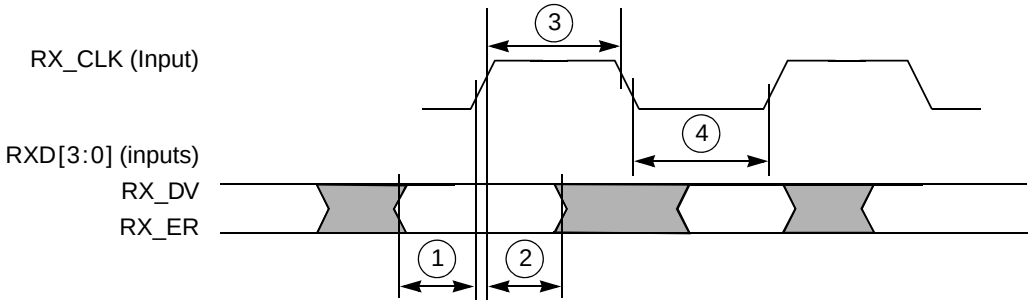

Figure 36. Ethernet Timing Diagram – MII Rx Signal

Table 33. MII Tx Signal Timing

Symbol	Description	Min	Max	Unit	SpecID
5	TX_CLK rising edge to TXD[3:0], TX_EN, TX_ER invalid	3	—	ns	A11.5
6	TX_CLK rising edge to TXD[3:0], TX_EN, TX_ER valid	—	25	ns	A11.6
7	TX_CLK pulse width high	35%	65%	TX_CLK Period[1]	A11.7
8	TX_CLK pulse width low	35%	65%	TX_CLK Period[1]	A11.8

1 The TX_CLK frequency shall be 25% of the nominal transmit frequency, e.g., a PHY operating at 100 Mb/s must provide a TX_CLK frequency of 25 MHz and a PHY operating at 10 Mb/s must provide a TX_CLK frequency of 2.5 MHz. See the IEEE 802.3 Specification.

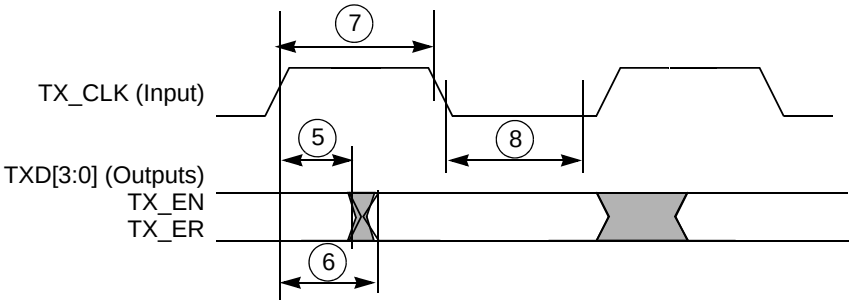

Figure 37. Ethernet Timing Diagram – MII Tx Signal

Table 34. MII Async Signal Timing

Symbol	Description	Min	Max	Unit	SpecID
9	CRS, COL minimum pulse width	1.5	—	TX_CLK Period	A11.9

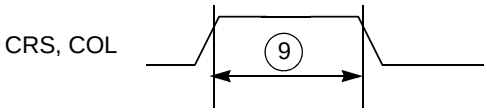

Figure 38. Ethernet Timing Diagram – MII Async

Table 35. MII Serial Management Channel Signal Timing

Symbol	Description	Min	Max	Unit	SpecID
10	MDC falling edge to MDIO output delay	0	25	ns	A11.10
11	MDIO (input) to MDC rising edge setup	10	—	ns	A11.11
12	MDIO (input) to MDC rising edge hold	0	—	ns	A11.12
13	MDC pulse width high[1]	160	—	ns	A11.13
14	MDC pulse width low[1]	160	—	ns	A11.14
15	MDC period[2]	400	—	ns	A11.15

1 MDC is generated by MPC5121e/MPC5123 with a duty cycle of 50% except when MII_SPEED in the FEC MII_SPEED control register is changed during operation. See the MPC5121e/MPC5123 Reference Manual.

3.3.15 DIU

The DIU is a display controller designed to manage the TFT LCD display.

3.3.15.1 Interface to TFT LCD Panels, Functional Description

Figure 42 shows the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with positive polarity. The sequence of events for active matrix interface timing is:

- DIU_CLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, DIU_CLK runs continuously. This signal frequency could be from 5 to 100 MHz depending on the panel type.
- DIU_HSYNC causes the panel to start a new line. It always encompasses at least one DIU_CLK pulse.
- DIU_VSYNC causes the panel to start a new frame. It always encompasses at least one DIU_HSYNC pulse.
- DIU_DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

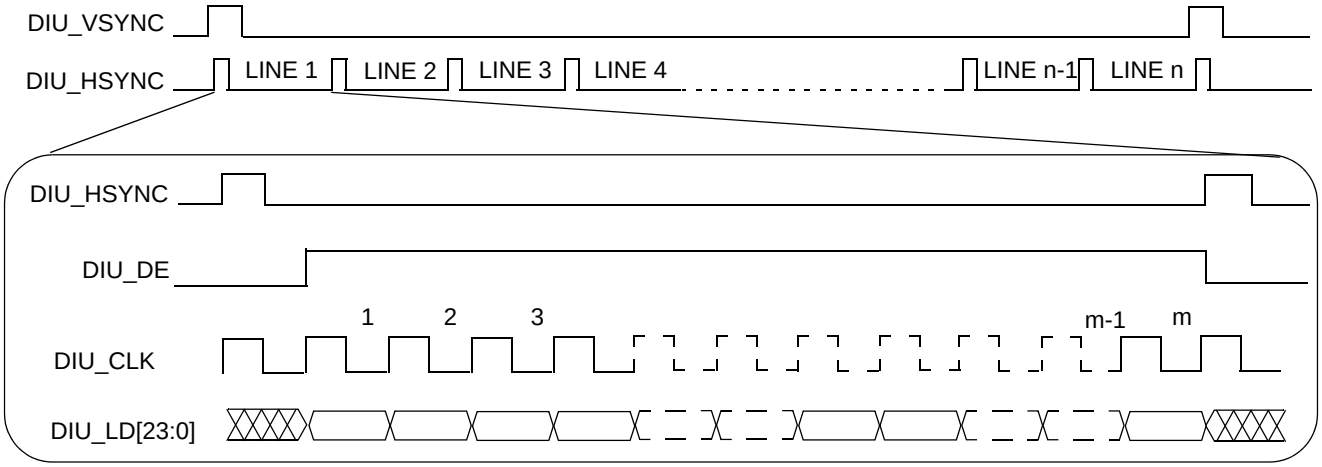

Figure 42. Interface Timing Diagram for TFT LCD Panels

3.3.15.2 Interface to TFT LCD Panels, Electrical Characteristics

Figure 43 shows the horizontal timing (timing of one line), including the horizontal sync pulse and the data. All parameters shown in the diagram are programmable. This timing diagram corresponds to positive polarity of the DIU_CLK signal (meaning the data and sync. signals change at the rising edge of it) and active-high polarity of the DIU_HSYNC, DIU_VSYNC and DIU_DE signal. You can select the polarity of the DIU_HSYNC and DIU_VSYNC signal via the SYN_POL register, whether active-high or active-low, the default is active-high. The DIU_DE signal is always active-high. And, pixel clock inversion and a flexible programmable pixel clock delay is also supported, programed via the DIU Clock Config Register (DCCR) in the system clock module.

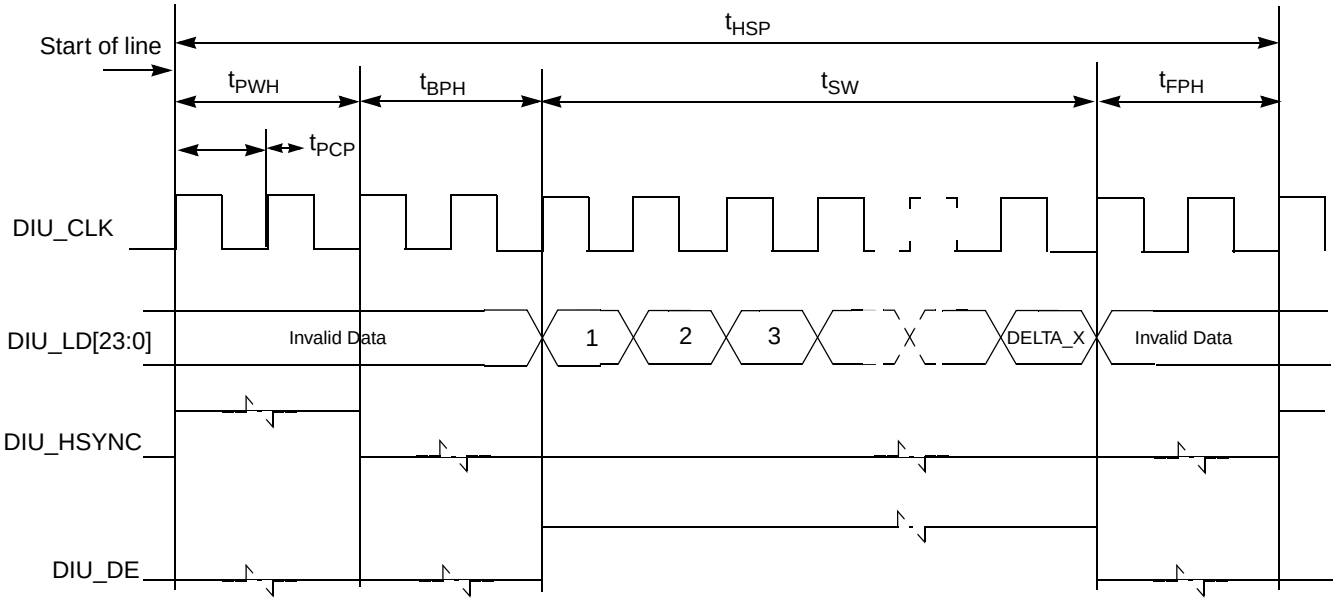

Figure 43. TFT LCD Interface Timing Diagram – Horizontal Sync Pulse

Figure 44 shows the vertical timing (timing of one frame), including the vertical sync pulse and the data. All parameters shown in the diagram are programmable.

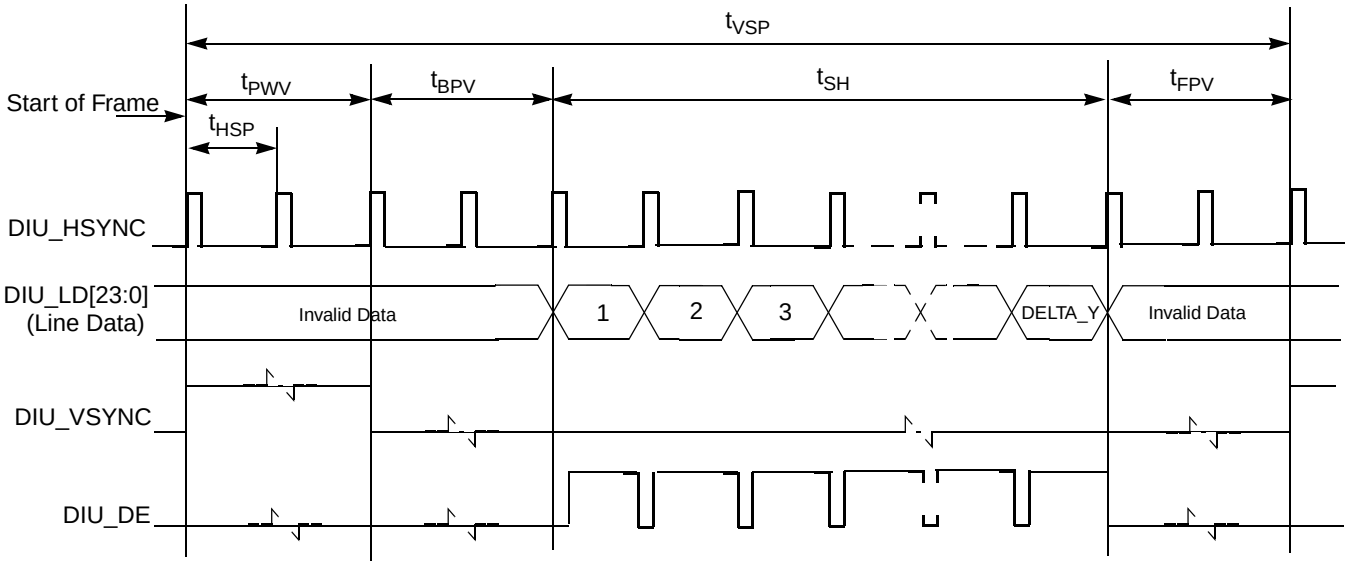

Figure 44. TFT LCD Interface Timing Diagram – Vertical Sync Pulse

Table 38 shows timing parameters of signals.

Table 38. LCD Interface Timing Parameters – Pixel Level

Name	Description	Value	Unit	SpecID
t_{PCP}	Display Pixel Clock Period	15[1]	ns	A15.1
t_{PWH}	HSYNC Pulse Width	PW_H × t_{PCP}	ns	A15.2
t_{BPH}	HSYNC Back Porch Width	BP_H × t_{PCP}	ns	A15.3

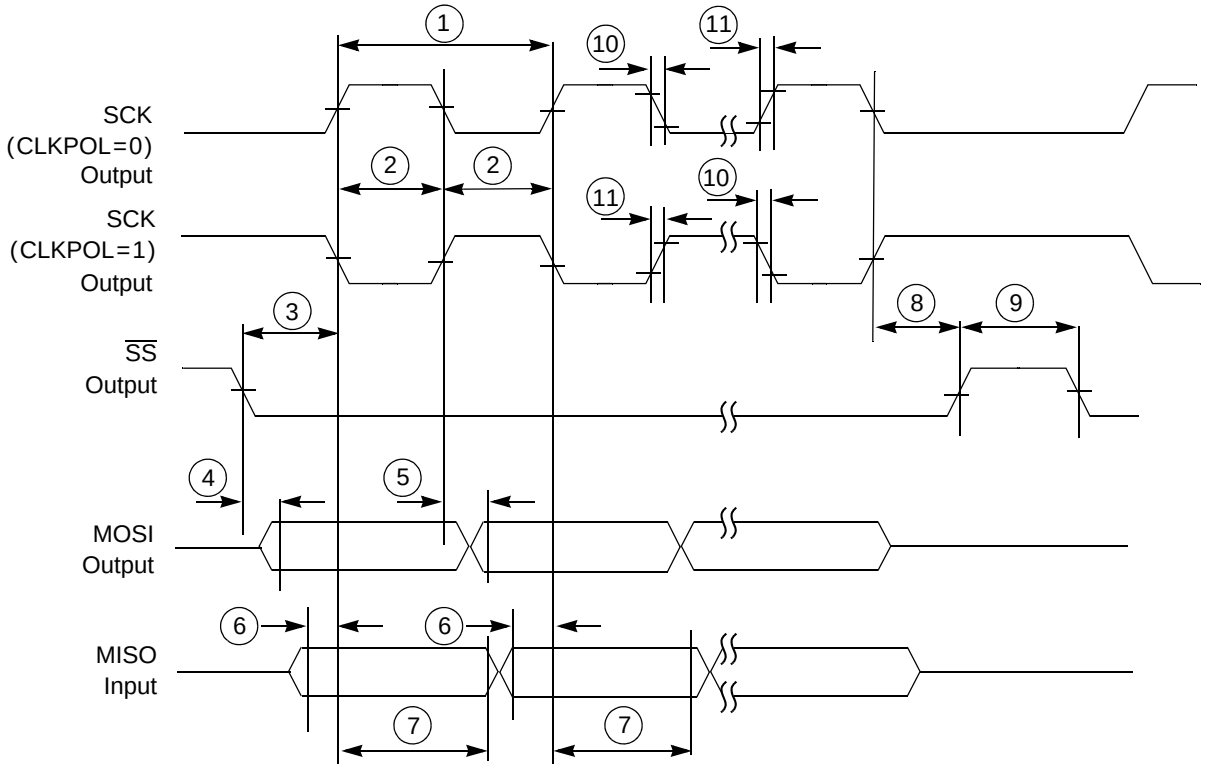

Figure 50. Timing Diagram – SPI Master Mode, Format 0 (CPHA = 0)

Table 46. Timing Specifications – SPI Slave Mode, Format 0 (CPHA = 0)

Symbol	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A20.37
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A20.38
3	Slave select clock delay	1.0	—	ns	A20.39
4	Input Data setup time	1.0	—	ns	A20.40
5	Input Data hold time	1.0	—	ns	A20.41
6	Output data valid after $\overline{SS}$	—	14.0	ns	A20.42
7	Output data valid after SCK	—	14.0	ns	A20.43
8	Slave disable lag time	0.0	—	ns	A20.44
9	Minimum Sequential Transfer delay = 2 × IP Bus clock cycle time	30.0	—	—	A20.45

NOTE

Output timing is specified at a nominal 50 pF load.

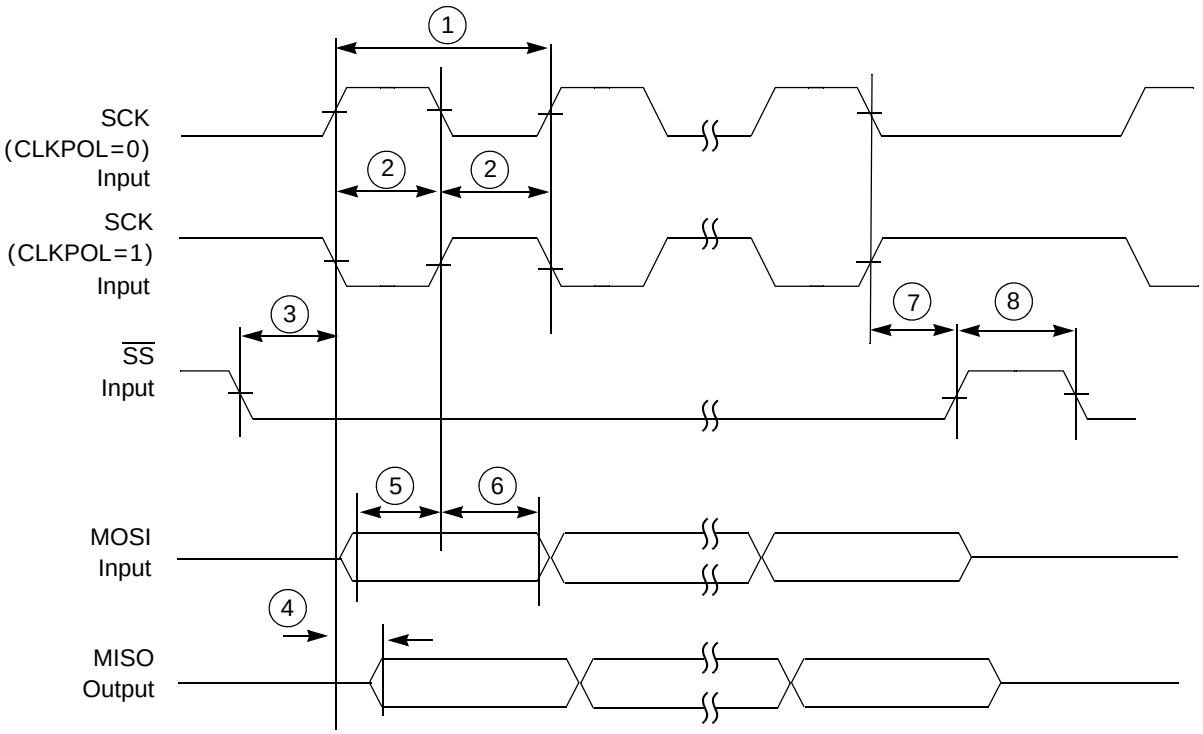

Figure 53. Timing Diagram – SPI Slave Mode, Format 1 (CPHA = 1)

3.3.21 GPIOs and Timers

The MPC5121e/MPC5123 contains several sets of I/Os that do not require special setup, hold, or valid requirements. The external events (GPIO or timer inputs) are asynchronous to the system clock. The inputs must be valid for at least tIOWID to ensure proper capture by the internal IP clock.

Table 49. GPIO/Timers Input AC Timing Specifications

Symbol	Description	Min	Unit	SpecID
t_{IOWID}	GPIO/Timers inputs—minimum pulse width	2T[1]	ns	A21.1

1 T is the IP bus clock cycle. T= 12 ns is the minimum value (for the maximum IP bus frequency of 83 MHz).

3.3.22 Fusebox

Table 50 gives the Fusebox specification.

Table 50. Fusebox Characteristics

Symbol	Description	Min	Max	Units	SpecID
t_{FUSEWR}	Program time[1] for Fuse	125	—	us	A22.1
I_{FUSEWR}	Program current to program one fuse bit	—	10	mA	A22.2

1 The program length is defined by the value defined in the EPM_PGM_LENGTH bits of the IIM module.

4.4.2 Pull-Up Requirements for the PCI Control Lines

PCI control signals always require pull-up resistors on the motherboard (not the expansion board) to ensure that they contain stable values when no agent is actively driving the bus. This includes PCI_FRAME, PCI_TRDY, PCI_IRDY, PCI_DEVSEL, PCI_STOP, PCI_SERR, PCI_PERR, and PCI_REQ.

Refer to the PCI Local Bus specification.

4.5 JTAG

The MPC5121e/MPC5123 provides you with an IEEE 1149.1 JTAG interface to facilitate board/system testing. It also provides a Common On-Chip Processor (COP) Interface, which shares the IEEE 1149.1 JTAG port.

The COP Interface provides access to the MPC5121e/MPC5123's embedded e300 processor and to other on-chip resources. This interface provides a means for executing test routines and for performing software development and debug functions.

4.5.1 TRST

Boundary scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification but is provided on all processors that implement the Power Architecture. To obtain a reliable power-on reset performance, the TRST signal must be asserted during power-on reset.

4.5.1.1 TRST and PORESET

The JTAG interface can control the direction of the MPC5121e/MPC5123 I/O pads via the boundary scan chain. The JTAG module must be reset before the MPC5121e/MPC5123 comes out of power-on reset; do this by asserting TRST before PORESET is released.

For more details refer to the Reset and JTAG Timing Specification.

Figure 62. PORESET vs. TRST

4.5.2 e300 COP/BDM Interface

There are two possibilities to connect the JTAG interface: using it with a COP connector and without a COP connector.

4.5.2.1 Boards Interfacing the JTAG Port via a COP Connector

The MPC5121e/MPC5123 functional pin interface and internal logic provides access to the embedded e300 processor core through the Freescale standard COP/BDM interface. Table 53 gives the COP/BDM interface signals. The pin order shown reflects only the COP/BDM connector order.

5 Package Information

This section details package parameters and dimensions. The MPC5121e/MPC5123 is available in a Thermally Enhanced Plastic Ball Grid Array (TEPBGA), see Section 5.1, “Package Parameters,” and Section 5.2, “Mechanical Dimensions,” for information on the TEPBGA.

5.1 Package Parameters

Table 54. TEPBGA Parameters

Package outline	27 mm × 27 mm
Interconnects	516
Pitch	1.00 mm
Module height (typical)	2.25 mm
Solder Balls	96.5 Sn/3.5Ag (VY *package)*
Ball diameter (typical)	0.6 mm

5.2 Mechanical Dimensions

Figure 65 shows the mechanical dimensions and bottom surface nomenclature of the MPC5121e/MPC5123 516 PBGA package.