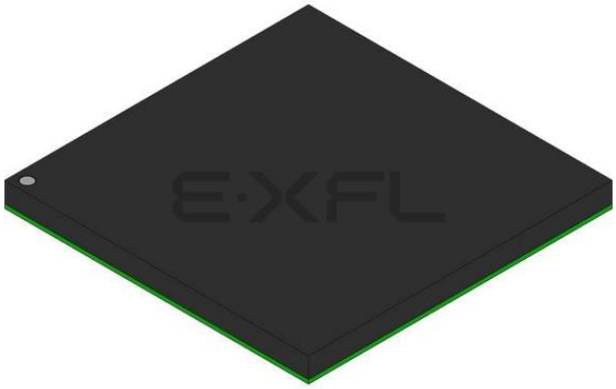

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e300
Core Size	32-Bit Single-Core
Speed	400MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, USB OTG
Peripherals	DMA, WDT
Number of I/O	147
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc5123vy400b

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 7 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
$\overline{\text{PCI\_GNT0}}$	E25	PCI	V_{DD_IO}	—
$\overline{\text{PCI\_GNT1}}$	G22	PCI	V_{DD_IO}	—
$\overline{\text{PCI\_GNT2}}$	E24	PCI	V_{DD_IO}	—
PCI_CLK	C26	PCI	V_{DD_IO}	—
PSC Interface (61 Total)				
PSC_MCLK_IN	C17	General IO	V_{DD_IO}	—
PSC0_0	D16	General IO	V_{DD_IO}	—
PSC0_1	A17	General IO	V_{DD_IO}	—
PSC0_2	E15	General IO	V_{DD_IO}	—
PSC0_3	C16	General IO	V_{DD_IO}	—
PSC0_4	B16	General IO	V_{DD_IO}	—
PSC1_0	C15	General IO	V_{DD_IO}	—
PSC1_1	A16	General IO	V_{DD_IO}	—
PSC1_2	E14	General IO	V_{DD_IO}	—
PSC1_3	A15	General IO	V_{DD_IO}	—
PSC1_4	D14	General IO	V_{DD_IO}	—
PSC2_0	C14	General IO	V_{DD_IO}	—
PSC2_1	B14	General IO	V_{DD_IO}	—
PSC2_2	E13	General IO	V_{DD_IO}	—
PSC2_3	A14	General IO	V_{DD_IO}	—
PSC2_4	D13	General IO	V_{DD_IO}	—
PSC3_0	AF3	General IO	V_{DD_IO}	—
PSC3_1	AB5	General IO	V_{DD_IO}	—
PSC3_2	AC4	General IO	V_{DD_IO}	—
PSC3_3	AD4	General IO	V_{DD_IO}	—
PSC3_4	AF4	General IO	V_{DD_IO}	—
PSC4_0	AB1	General IO	V_{DD_IO}	—
PSC4_1	AA3	General IO	V_{DD_IO}	—
PSC4_2	AB3	General IO	V_{DD_IO}	—
PSC4_3	AA5	General IO	V_{DD_IO}	—
PSC4_4	AC2	General IO	V_{DD_IO}	—
PSC5_0	AC1	General IO	V_{DD_IO}	—
PSC5_1	AC3	General IO	V_{DD_IO}	—
PSC5_2	AD1	General IO	V_{DD_IO}	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 11 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
V_{SS}	A2, A3, A25, B1,B2, B3, B5, B7, B12, B17, B20, B22, B26, C1, C4, C23, C25, D2, D12, D17, D24, D25, E18, F2, F3, F4, F5, F6, F8, F10, F16, F17, F21, G5, H6, H23, H25, K6, K21, L6, L11, L12, L13, L14, L15, L16, L21, M2, M4, M11, M12, M13, M14, M15, M16, N5, N11, N12, N13, N14, N15, N16,	Ground	—	—
V_{SS}	N23, N25, P11, P12, P13, P14, P15, P16, R11, R12, R13, R14, R15, R16, T6, T11, T12, T13, T14, T15, T16, T21, U2, U4, U6, U21, V23, V25, Y24, AA6, AA10, AA11, AA16, AA17, AA21, AB2, AB4, AB10, AB24, AC8, AC12, AC17, AC22, AD3, AD25, AE7, AE12, AE17, AE23, AE26	Ground	—	—
SYS_PLL_AVDD	T22	Analog Power	—	—
SYS_PLL_AVSS	U22	Analog Ground	—	—
CORE_PLL_AVDD	AA19	Analog Power	—	—
CORE_PLL_AVSS	AD23	Analog Ground	—	—
VBAT_RTC	D19	Power	—	—
AVDD_FUSEWR	C9	Power	—	—
MVTT0	AB7	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
MVTT1	AF9	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
MVTT2	AE11	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
MVTT3	AE14	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
Power and Ground Supplies (USB PHY)				
USB_PLL_GND	E23	Analog Ground	—	—
USB_PLL_PWR3	D23	Analog Power	—	—
USB_RREF	E22	Analog Power	—	—
USB_VSSA_BIAS	B23	Analog Ground	—	—

Table 6. DC Electrical Specifications (continued)

Characteristic	Condition	Symbol	Min	Max	Unit	SpecID
Input leakage current	RTC_XTALI Vin = 0 or V_{DD_IO}	I_{IN}	—	1.0	µA	D3.23
Input current, pullup resistor[6]	Pullup V_{DD_IO} Vin = VIL	I_{INpu}	25	150	µA	D3.24
Input current, pulldown resistor [8]	Pulldown V_{DD_IO} Vin = VIH	I_{INpd}	25	150	µA	D3.25
Output high voltage	IOH is driver dependent[7] V_{DD_IO}	V_{OH}	0.8 × V_{DD_IO}	—	V	D3.26
Output high voltage	IOH is driver dependent[7] $V_{DD\_MEM\_IO\_DDR}$	V_{OHDDR}	1.90	—	V	D3.27
Output high voltage	IOH is driver dependent[7] $V_{DD\_MEM\_IO\_DDR2}$	V_{OHDDR2}	1.396	—	V	D3.28
Output high voltage	IOH is driver dependent[7] $V_{DD\_MEM\_IO\_LPDDR}$	$V_{OHLPDDR}$	$V_{DD\_MEM\_IO}$ – 0.28	—	V	D3.28
Output low voltage	IOL is driver dependent[7] V_{DD_IO}	V_{OL}	—	0.2 × V_{DD_IO}	V	D3.30
Output low voltage	IOL is driver dependent[7] $V_{DD\_MEM\_IO\_DDR}$	V_{OLDDR}	—	0.36	V	D3.31
Output low voltage	IOL is driver dependent[7] $V_{DD\_MEM\_IO\_DDR2}$	V_{OLDDR2}	—	0.28	V	D3.32
Output low voltage	IOL is driver dependent[7] $V_{DD\_MEM\_IO\_LPDDR}$	$V_{OLLPDDR}$	—	0.28	V	D3.33
Differential cross point voltage (DDR MCK/$\overline{\text{MCK}}$)	—	V_{OXMCK}	0.5 × $V_{DD\_MEM\_IO}$ – 0.125	0.5 × $V_{DD\_MEM\_IO}$ + 0.125	V	D3.34
DC Injection Current Per Pin[8]	—	I_{CS}	–1.0	1.0	mA	D3.35
Input Capacitance (digital pins)	—	C_{in}	—	7	pF	D3.36
Input Capacitance (analog pins)	—	C_{in}	—	10	pF	D3.37
On Die Termination (DDR2)	—	R_{ODT}	120	180	Ω	D3.38

1 This parameter is meant for those who do not use quartz crystals or resonators, but CAN osc, in crystal mode. In that case, Vextal – Vxtal - 400mV criteria has to be met for oscillator's comparator to produce output clock.

2 This parameter is meant for those who do not use quartz crystals or resonators, but signal generator clock to drive, in bypass mode. In that case, drive only the EXTAL pin not connecting anything to other pin for the oscillator's comparator to produce output clock.

3 This parameter is meant for those who do not use quartz crystals or resonators, but CAN osc, in crystal mode. In that case, drive one of the XTAL_IN or XTAL_OUT pins not connecting anything to other pin for the oscillator's comparator to produce output clock.

4 This parameter is meant for those who do not use quartz crystals or resonators, but signal generator clock to drive, in bypass mode. In that case, drive only the xtal_in pin not connecting anything to other pin for the oscillator's comparator to produce output clock.

5 Leakage current is measured with output drivers disabled and pull-up/pull-downs inactive.

6 Pullup current is measured at VIL and pulldown current is measured at VIH.

4 Fall time is measured from 20% of vdd to 80% of V_{DD}.
5 SYS_XTALI duty cycle is measured at V_M.

3.2.2 RTC Oscillator Electrical Characteristics

Table 13. RTC Oscillator Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit	SpecID
RTC_XTALI frequency	f_{rtc_xtal}	—	32.768	—	kHz	O2.1

3.2.3 System PLL Electrical Characteristics

Table 14. System PLL Specifications

Characteristic	Symbol	Min	Typical	Max	Unit	SpecID
Sys PLL input clock frequency[1]	f_{sys_xtal}	16	33.3	67	MHz	O3.1
Sys PLL input clock jitter[2]	t_{jitter}	—	—	10	ps	O3.2
Sys PLL VCO frequency[1]	f_{VCOsys}	400	—	800	MHz	O3.3
Sys PLL VCO output jitter (Dj), peak to peak / cycle	$f_{VCOjitterDj}$	—	—	40	ps	O3.4
Sys PLL VCO output jitter (Rj), RMS 1 sigma	$f_{VCOjitterRj}$	—	—	12	ps	O3.5
Sys PLL relock time—after power up[3]	t_{lock1}	—	—	200	µs	O3.6
Sys PLL relock time—when power was on[4]	t_{lock2}	—	—	170	µs	O3.7

1 The SYS_XTALI frequency and PLL Configuration bits must be chosen such that the resulting system frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
2 This represents total input jitter—short term and long term combined. Two different types of jitter can exist on the input to CORE_SYSCLK, systemic and true random jitter. True random jitter is rejected. Systemic jitter is passed into and through the PLL to the internal clock circuitry.
3 PLL relock time is the maximum amount of time required for the PLL lock after a stable VDD and CORE_SYSCLK are reached during the power-on reset sequence.
4 PLL relock time is the maximum amount of time required for the PLL lock after the PLL has been disabled and subsequently re-enabled during sleep modes.

3.2.4 e300 Core PLL Electrical Characteristics

The internal clocking of the e300 core is generated from and synchronized to the system clock by means of a voltage-controlled core PLL.

Table 15. e300 PLL Specifications

Characteristic	Symbol	Min	Typical	Max	Unit	SpecID
e300 frequency[1]	f_{core}	200	—	400	MHz	O4.1
e300 PLL VCO frequency[1]	$f_{VCOcore}$	400	—	800	MHz	O4.3
e300 PLL input clock frequency	f_{CSB_CLK}	50	—	200	MHz	O4.4
e300 PLL input clock cycle time	t_{CSB_CLK}	5	—	20	ns	O4.5
e300 PLL relock time[2]	t_{lock}	—	—	200	µs	O4.6

3.3 AC Electrical Characteristics

3.3.1 Overview

Hyperlinks to the indicated timing specification sections are provided in the following:

- AC Operating Frequency Data
- Resets
- External Interrupts
- SDRAM (DDR)
- PCI
- LPC
- NFC
- PATA
- SATA PHY
- FEC
- USB ULPI
- On-Chip USB PHY
- SDHC
- DIU
- SPDIF
- CAN
- I^2C
- J1850
- PSC
- GPIOs and Timers
- Fusebox
- IEEE 1149.1 (JTAG)
- VIU

AC Test Timing Conditions:

Unless otherwise noted, all test conditions are as follows:

- T_A = –40 to 85 ^oC
- V_{DD_CORE} = 1.33 to 1.47 V
  V_{DD_IO} = 3.0 to 3.6 V
- Input conditions:
  All Inputs: tr, tf ≤ 1 ns
- Output Loading:
  All Outputs: 50 pF

3.3.2 AC Operating Frequency Data

Table 16 provides the operating frequency information for the MPC5121e/MPC5123.

Table 16. Clock Frequencies

	Min	Max	Units	SpecID
e300 Processor Core	200	400	MHz	A1.1
SDRAM Clock	28.6	200	MHz	A1.2
CSB Bus Clock	50.0	200	MHz	A1.3
IP Bus Clock	8.3	83	MHz	A1.4
PCI Clock	4.43	66	MHz	A1.5
LPC Clock	2.08	83	MHz	A1.6

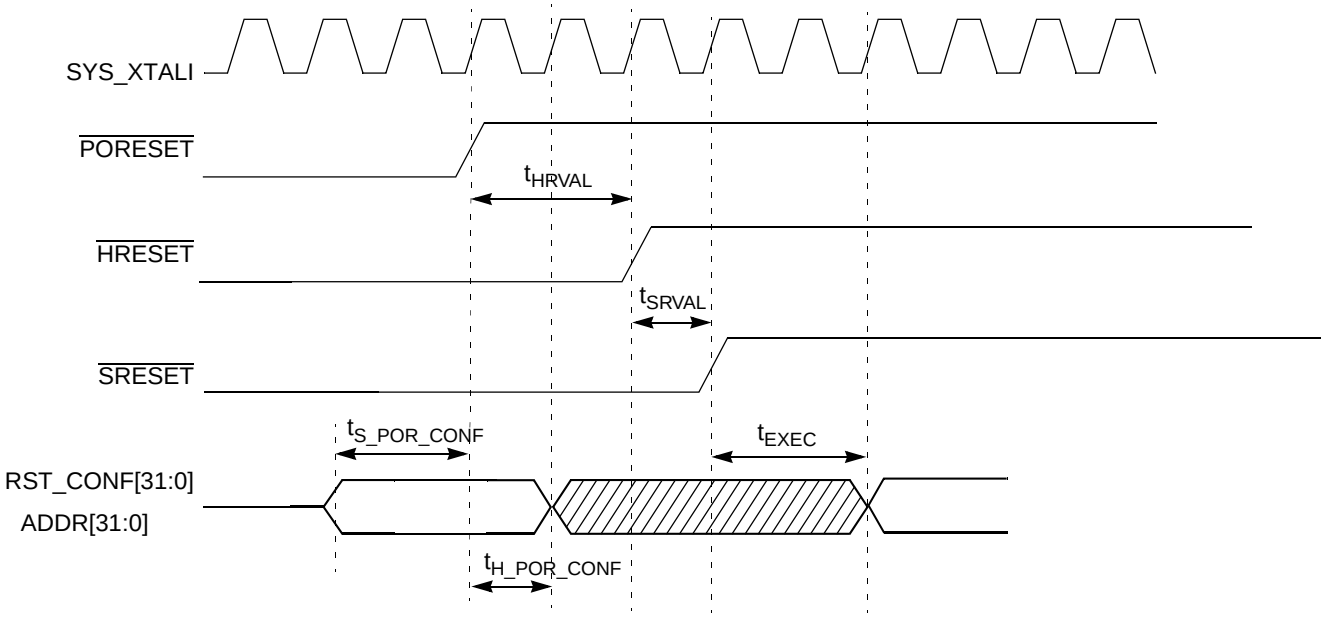

Figure 4. Power-Up Behavior

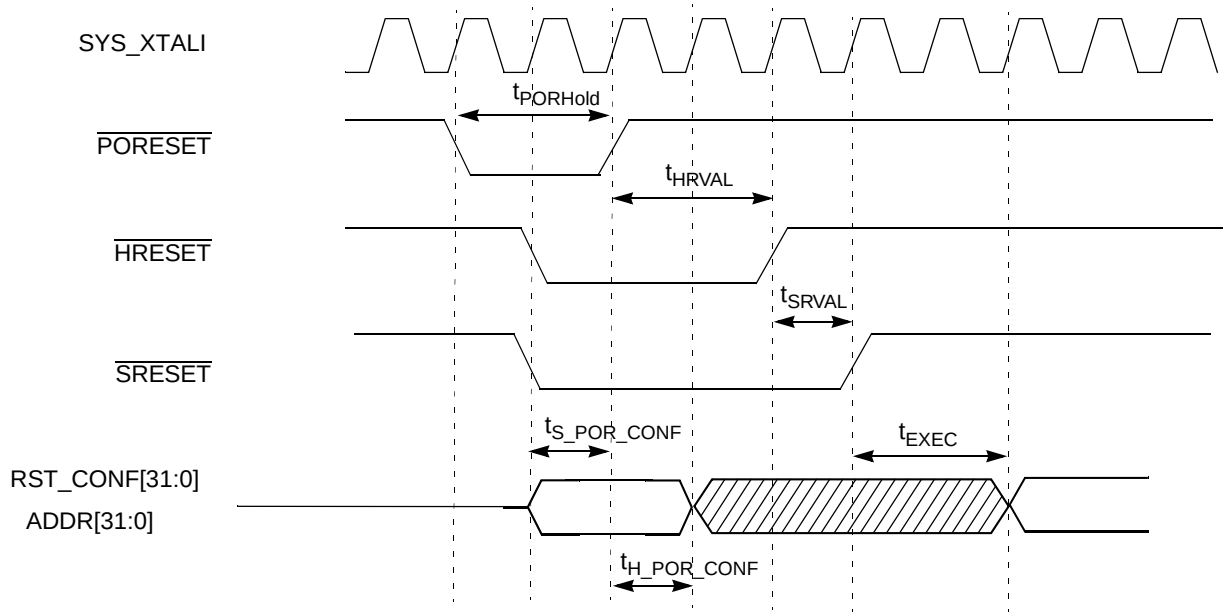

Figure 5. Power-On Reset Behavior

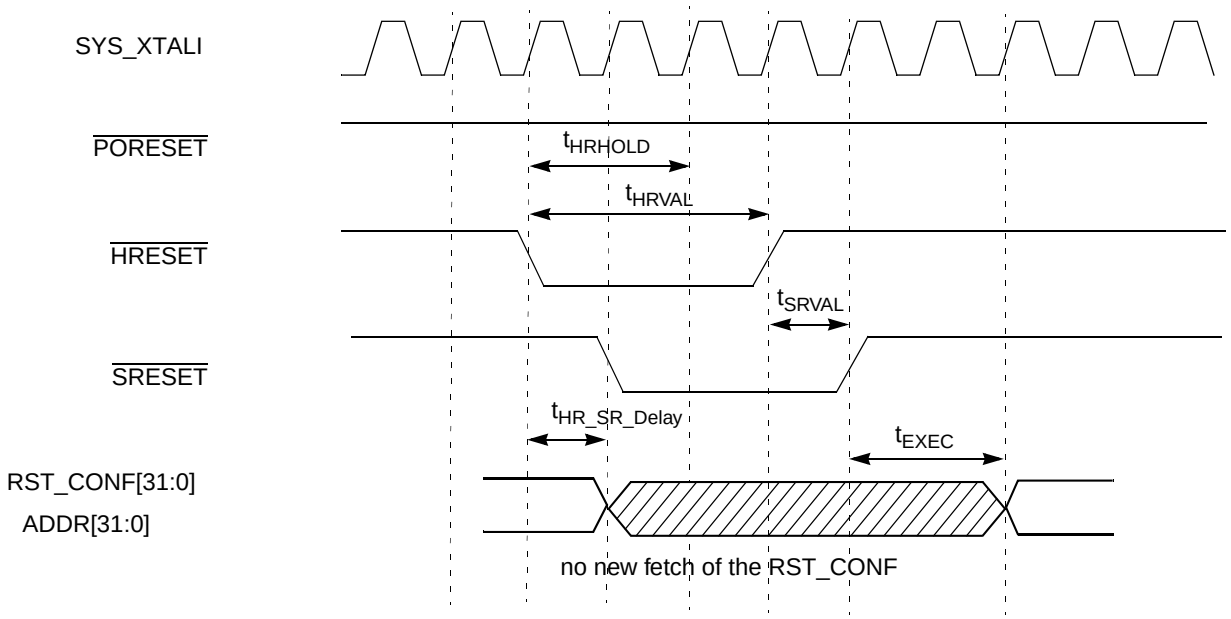

Figure 6. HRESET Behavior

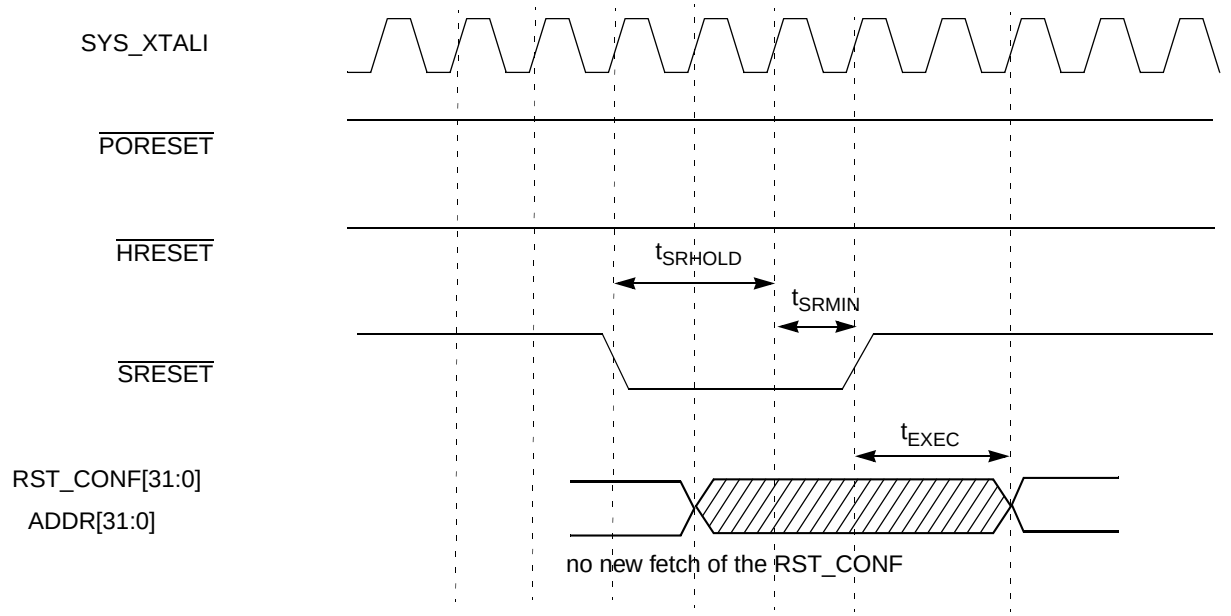

Figure 7. SRESET Behavior

Table 18. Reset Timing

Symbol	Description	Value SYS_XTALI	SpecID
$t_{PORHOLD}$	Time $\overline{\text{PORESET}}$ must be held low before a qualified reset occurs	4 cycles	A3.10
t_{HRVAL}	Time $\overline{\text{HRESET}}$ is asserted after a qualified reset occurs	26810 cycles	A3.11
t_{SRVAL}	Time $\overline{\text{SRESET}}$ is asserted after assertion of $\overline{\text{HRESET}}$	32 cycles	A3.12
t_{EXEC}	Time between $\overline{\text{SRESET}}$ assertion and first core instruction fetch	4 cycles	A3.13

3.3.5.1 DDR and DDR2 SDRAM AC Timing Specifications

Table 20. DDR and DDR2 (DDR2-400) SDRAM Timing Specifications

At recommended operating conditions with $V_{DD\_MEM\_IO}$ of ±5%

Parameter	Symbol	Min	Max	Unit	Notes	SpecID
Clock cycle time, CL=x	t_{CK}	5000	—	ps		A5.1
CK HIGH pulse width	t_{CH}	0.47	0.53	t_{CK}	1,2	A5.3
CK LOW pulse width	t_{CL}	0.47	0.53	t_{CK}	1,2	A5.4
Skew between MCK and DQS transitions	t_{DQSS}	–0.25	0.25	t_{CK}	2, 3	A5.5
Address and control output setup time relative to MCK rising edge	$t_{OS(base)}$	(t_{CK}/2 – 750)	—	ps	2, 3	A5.6
Address and control output hold time relative to MCK rising edge	$t_{OH(base)}$	(t_{CK}/2 – 750)	—	ps	2, 3	A5.7
DQ and DM output setup time relative to DQS	$t_{DS1(base)}$	(t_{CK}/4 – 500)	—	ps	2, 3	A5.8
DQ and DM output hold time relative to DQS	$t_{DH1(base)}$	(t_{CK}/4 – 500)	—	ps	2, 3	A5.9
DQS-DQ skew for DQS and associated DQ inputs	t_{DQSQ}	–(t_{CK}/4 – 600)	(t_{CK}/4 – 600)	ps	2	A5.10
DQS window start position related to CAS read command	t_{DQSEN}	TBD	TBD	ps	1,2,3,4,5	A5.11

1 Measured with clock pin loaded with differential 100 termination resistor.

2 All transitions measured at mid-supply (VDD_MEM_IO/2).

3 Measured with all outputs except the clock loaded with 50 Ω termination resistor to $V_{DD\_MEM\_IO}$/2.

4 In this window, the first rising edge of DQS should occur. From the start of the window to DQS rising edge, DQS should be low.

5 Window position is given for t_{DQSEN} = 2.0 t_{CK}. For other values of t_{DQSEN}, window position is shifted accordingly.

Figure 8 shows the DDR SDRAM write timing.

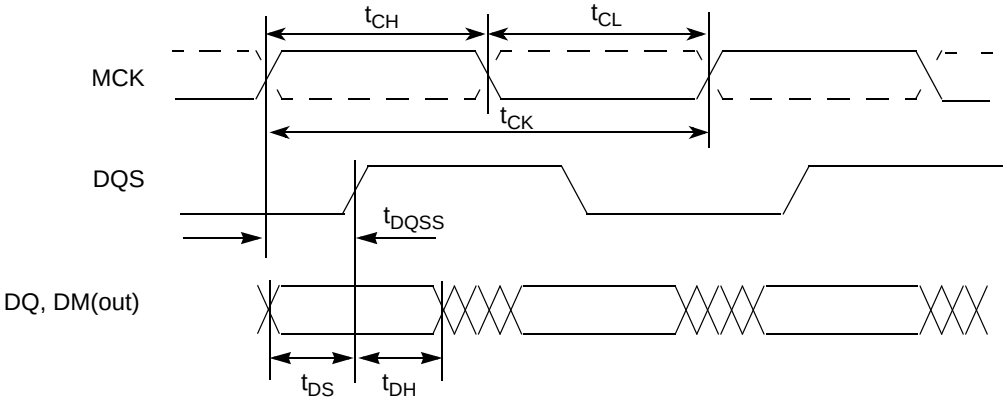

Figure 8. DDR Write Timing

Figure 9 and Figure 10 shows the DDR SDRAM read timing.

3.3.7.2 MUXed Mode

3.3.7.2.1 MUXed Non-Burst Mode

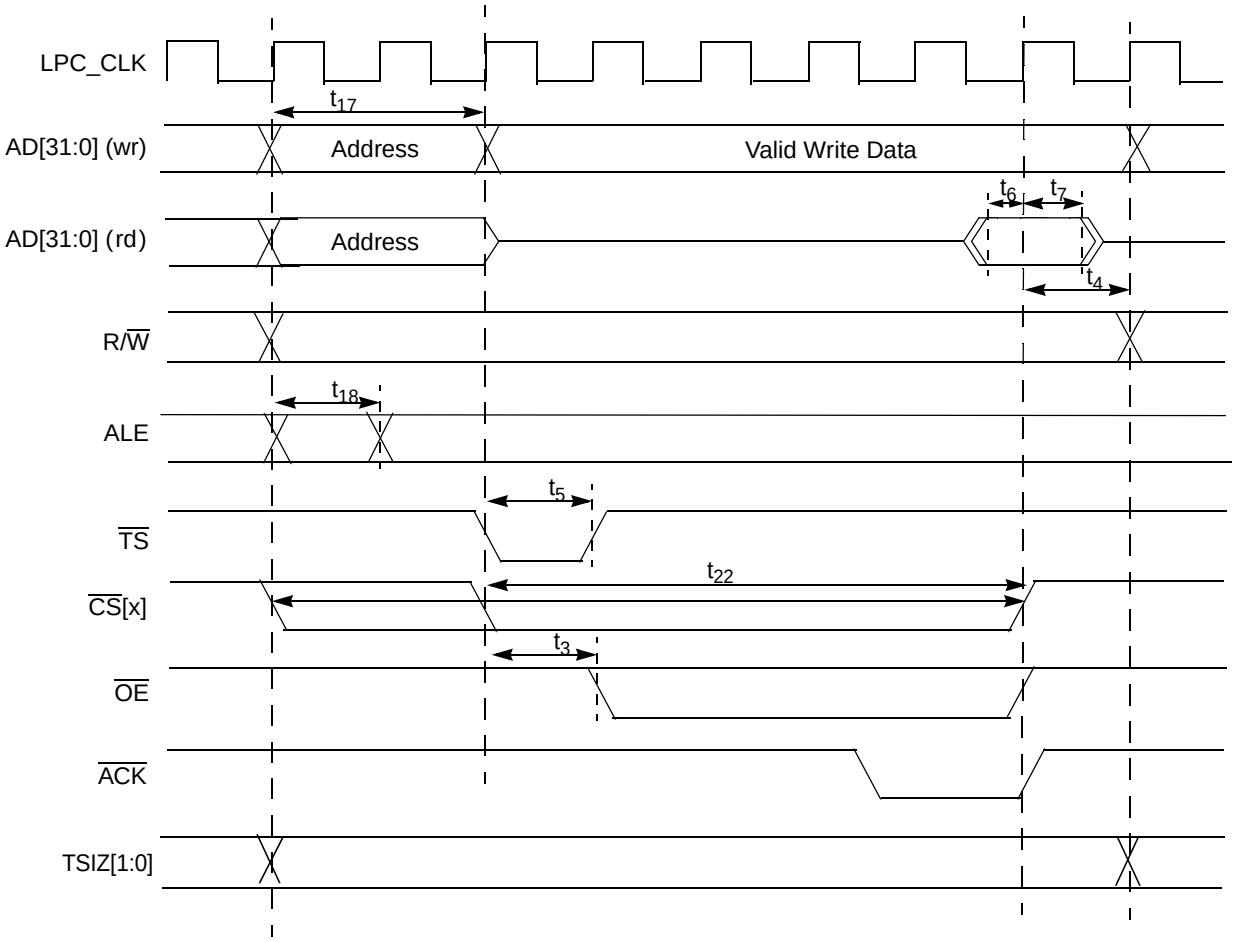

Figure 18. Timing Diagram – MUXed Non-Burst Mode

NOTE

$\overline{\text{ACK}}$ is asynchonous input signal and has no timing requirements. $\overline{\text{ACK}}$ needs to be deasserted after $\overline{\text{CS}}$[x] is deasserted.

3.3.7.2.2 MUXed Synchronous Read Burst Mode

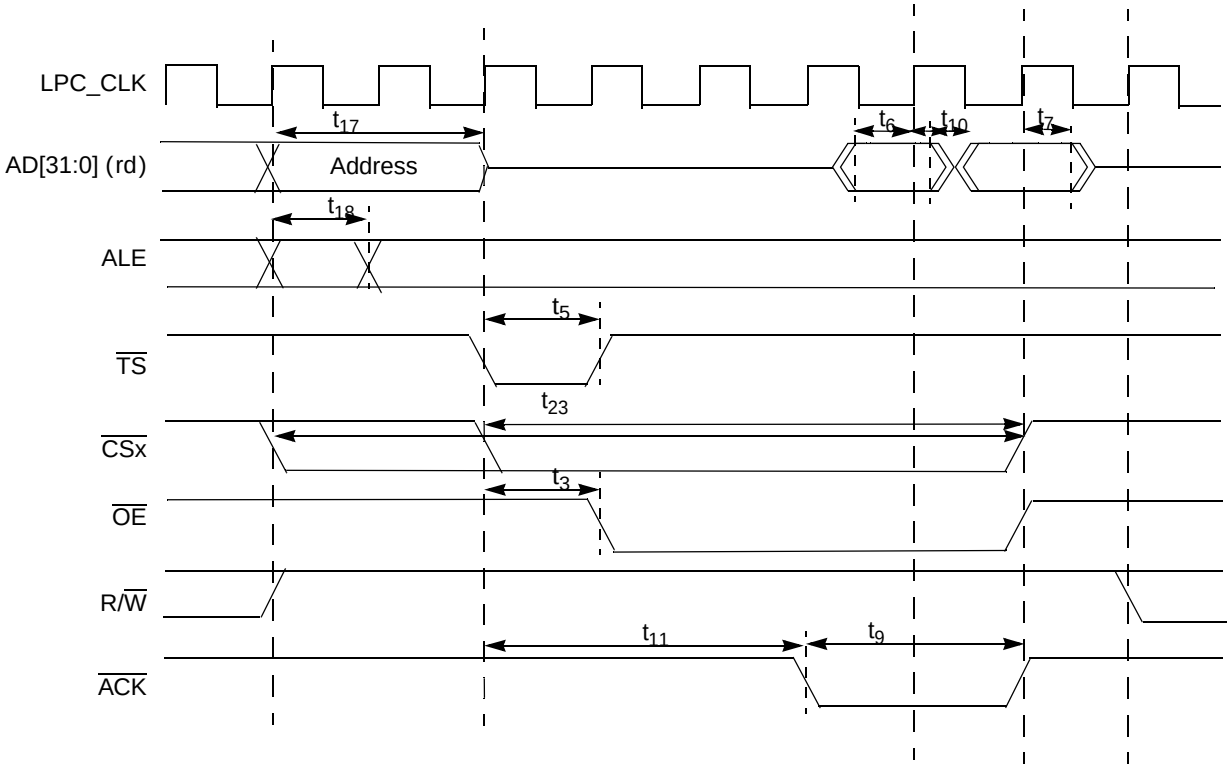

Figure 19. Timing Diagram – MUXed Synchronous Read Burst

3.3.7.2.3 MUXed Synchronous Write Burst Mode

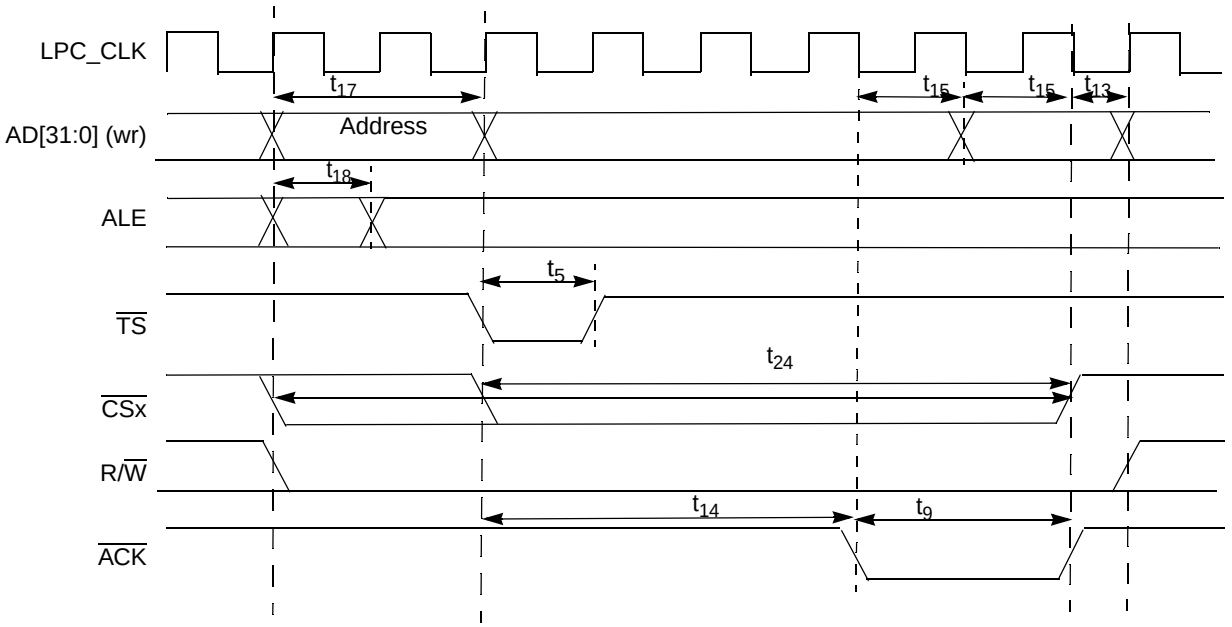

Figure 20. Timing Diagram – MUXed Synchronous Write Burst

3.3.8 NFC

The NAND flash controller (NFC) implements the interface to standard NAND Flash memory devices. This section describes the timing parameters of the NFC.

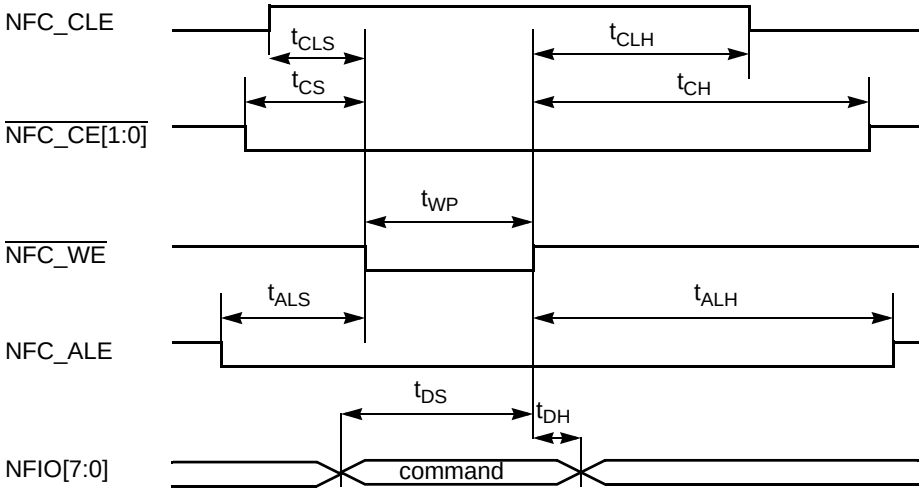

Figure 21. Command Latch Cycle Timing

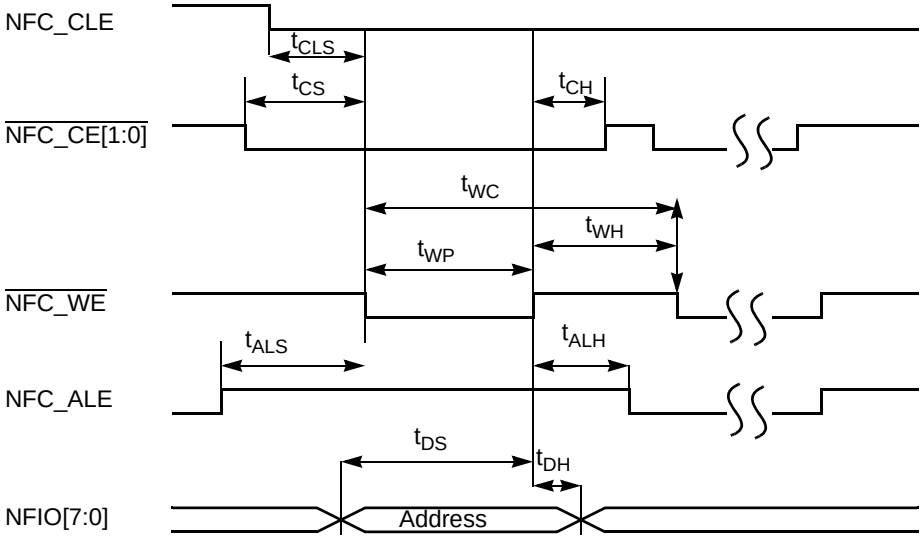

Figure 22. Address Latch Cycle Timing

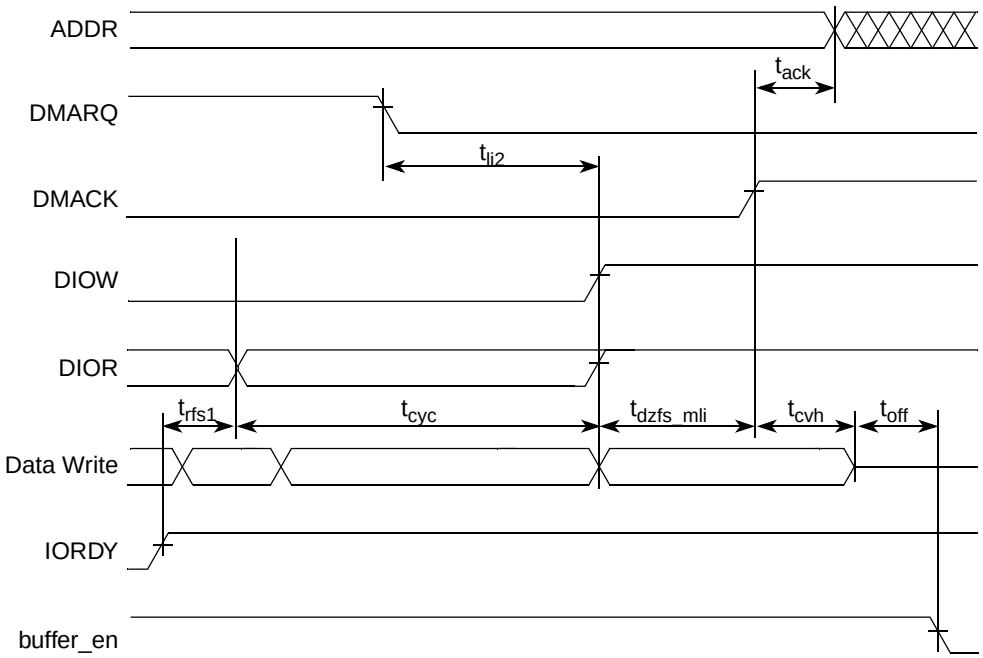

Figure 35. UDMA Out Device Terminates Transfer

Timing parameters are explained in Table 31.

Table 31. Timing Parameters UDMA Out Burst

ATA Parameter	UDMA Out Timing Parameter	Value	How to meet	SpecID
t_{ack}	t_{ack}	$t_{ack(min)} = (time\_ack \times T) - (t_{skew1} + t_{skew2})$	calculate and program time_ack. [1]	A9.63
t_{env}	t_{env}	$t_{env(min)} = (time\_env \times T) - (t_{skew1} + t_{skew2})$ $t_{env(max)} = (time\_env \times T) + (t_{skew1} + t_{skew2})$	calculate and program time_env. [1]	A9.64
t_{dvs}	t_{dvs}	$t_{dvs} = (time\_dvs \times T) - (t_{skew1} + t_{skew2})$	calculate and program time_dvs. [1]	A9.65
t_{dvh}	t_{dvh}	$t_{dvs} = (time\_dvh \times T) - (t_{skew1} + t_{skew2})$	calculate and program time_dvh. [1]	A9.66
t_{cyc}	t_{cyc}	$t_{cyc} = time\_cyc \times T - (t_{skew1} + t_{skew2})$	calculate and program time_cyc. [1]	A9.67
t_{2cyc}	—	$t_{2cyc} = time\_cyc \times 2 \times T$	calculate and program time_cyc. [1]	A9.68
t_{rfs1}	t_{rfs1}	$t_{rfs1} = 1.6 \times T + t_{sui} + t_{co} + t_{buf} + t_{buf}$	—	A9.69
—	t_{dzfs}	$t_{dzfs} = time\_dzfs \times T - (t_{skew1})$	calculate and program time_dzfs. [1]	A9.70
t_{ss}	t_{ss}	$t_{ss} = time\_ss \times T - (t_{skew1} + t_{skew2})$	calculate and program time_ss. [1]	A9.71
t_{mli}	t_{dzfs_mli}	$t_{dzfs\_mli} = \max(time\_dzfs, time\_mli) \times T - (t_{skew1} + t_{skew2})$	—	A9.72
t_{li}	t_{li1}	$t_{li1} > 0$	—	A9.73

Table 31. Timing Parameters UDMA Out Burst (continued)

ATA Parameter	UDMA Out Timing Parameter	Value	How to meet	SpecID
t_{li}	t_{li2}	$t_{li2} > 0$	—	A9.74
t_{li}	t_{li3}	$t_{li3} > 0$	—	A9.75
t_{cvh}	t_{cvh}	$t_{cvh} = (time\_cvh \times T) - (t_{skew1} + t_{skew2})$	calculate and program time_cvh. [1]	A9.76
—	t_{on} t_{off}	$t_{on} = time\_on \times T - t_{skew1}$ $t_{off} = time\_off \times T - t_{skew1}$	—	A9.77

1 See the *MPC5121e Microcontroller Reference Manual.*

3.3.10 SATA PHY

1.5 Gbps SATA PHY Layer

See “Serial ATA: High Speed Serialized AT Attachment” Revision 1.0a, 7-January-2003.

3.3.11 FEC

AC Test Timing Conditions:

- Output Loading
  All Outputs: 25 pF

Table 32. MII Rx Signal Timing

Symbol	Description	Min	Max	Unit	SpecID
1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns	A11.1
2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns	A11.2
3	RX_CLK pulse width high	35%	65%	RX_CLK Period[1]	A11.3
4	RX_CLK pulse width low	35%	65%	RX_CLK Period[1]	A11.4

1 RX_CLK shall have a frequency of 25% of data rate of the received signal. See the IEEE 802.3 Specification.

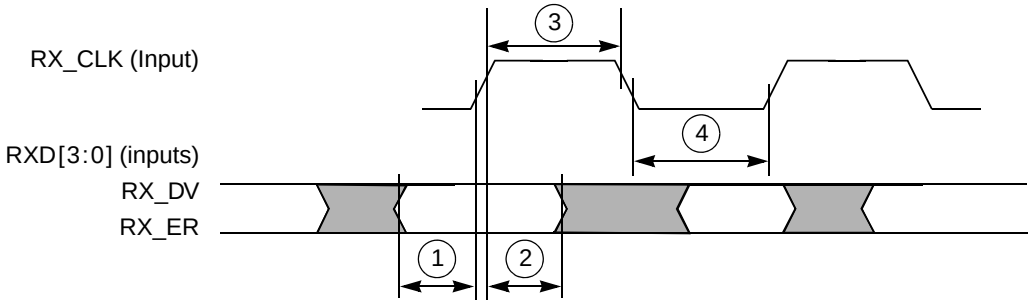

Figure 36. Ethernet Timing Diagram – MII Rx Signal

3.3.16 SPDIF

The Sony/Philips Digital Interface (SPDIF) timing is totally asynchronous, therefore there is no need for relationship with the clock.

3.3.17 CAN

The CAN functions are available as TX and CAN3/4_RX pins at normal IO pads and as CAN1/2 RX pins at the VBAT_RTC domain. There is no filter for the WakeUp dominant pulse. Any High-to-Low edge can cause WakeUp, if configured.

3.3.18 I^2C

This section specifies the timing parameters of the Inter-Integrated Circuit (I^2C) interface. Refer to the I^2C Bus Specification.

Table 40. I^2C Input Timing Specifications – SCL and SDA

Symbol	Description	Min	Max	Units	SpecID
1	Start condition hold time	2	—	IP-Bus Cycle[1]	A18.1
2	Clock low time	8	—	IP-Bus Cycle[1]	A18.2
4	Data hold time	0.0	—	ns	A18.3
6	Clock high time	4	—	IP-Bus Cycle[1]	A18.4
7	Data setup time	0.0	—	ns	A18.5
8	Start condition setup time (for repeated start condition only)	2	—	IP-Bus Cycle[1]	A18.6
9	Stop condition setup time	2	—	IP-Bus Cycle[1]	A18.7

1 Inter Peripheral Clock is defined in the MPC5121e/MPC5123 *Reference Manual*.

Table 41. I^2C Output Timing Specifications – SCL and SDA

Symbol	Description	Min	Max	Units	SpecID
1[1]	Start condition hold time	6	—	IP-Bus Cycle[2]	A18.8
2[1]	Clock low time	10	—	IP-Bus Cycle[2]	A18.9
3[3]	SCL/SDA rise time	—	7.9	ns	A18.10
4[1]	Data hold time	7	—	IP-Bus Cycle[2]	A18.11
5[1]	SCL/SDA fall time	—	7.9	ns	A18.12
6[1]	Clock high time	10	—	IP-Bus Cycle[2]	A18.13
7[1]	Data setup time	2	—	IP-Bus Cycle[2]	A18.14
8[1]	Start condition setup time (for repeated start condition only)	20	—	IP-Bus Cycle[2]	A18.15
9[1]	Stop condition setup time	10	—	IP-Bus Cycle[2]	A18.16

1 Programming IFDR with the maximum frequency results in the minimum output timings listed. The I^2C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.

2 Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Inter Peripheral Clock is defined in the *MPC5121e/MPC5123 Reference Manual.*

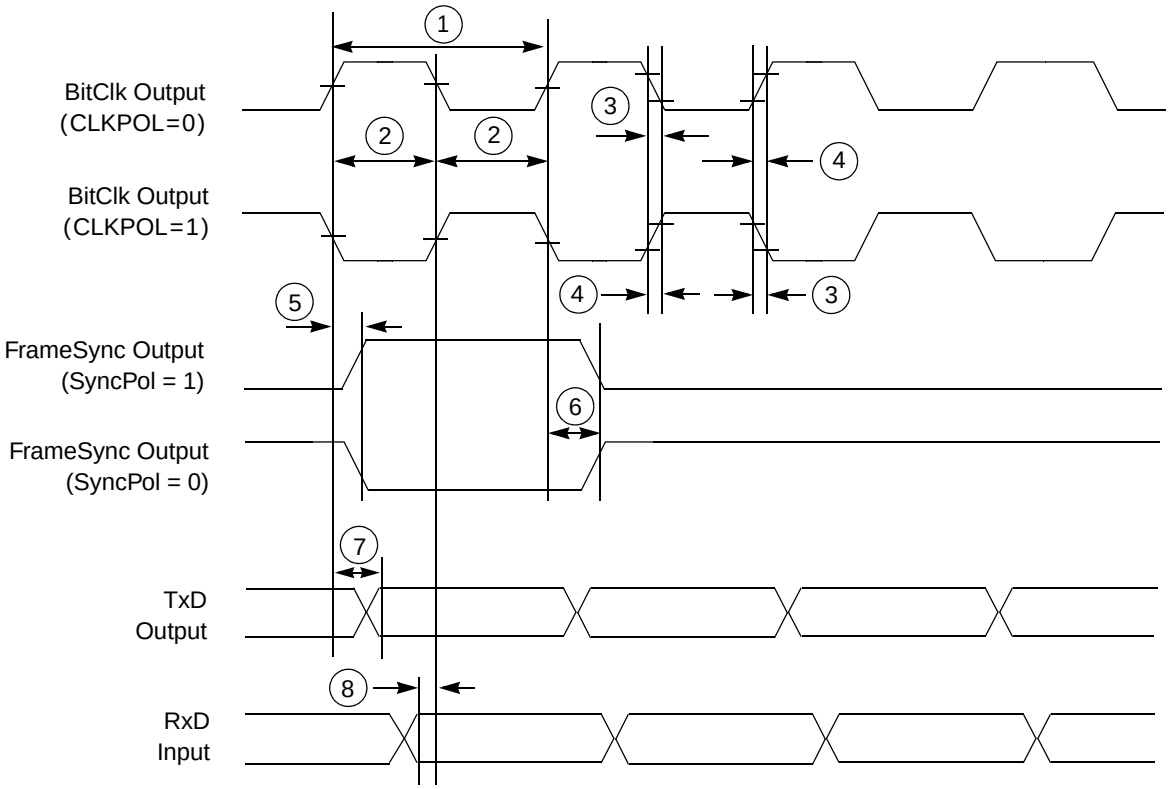

Figure 47. Timing Diagram – 8, 16, 24, and 32-bit CODEC/I^{2}S Master Mode

Table 43. Timing Specifications – 8, 16, 24, and 32-bit CODEC/I^{2}S Slave Mode

Symbol	Description	Min	Typ	Max	Units	SpecID
1	Bit Clock cycle time	40.0	—	—	ns	A20.9
2	Clock duty cycle	—	50	—	%[1]	A20.10
3	FrameSync setup time	1.0	—	—	ns	A20.11
4	Output Data valid after clock edge	—	—	14.0	ns	A20.12
5	Input Data setup time	1.0	—	—	ns	A20.13
6	Input Data hold time	1.0	—	—	ns	A20.14

1 Bit Clock cycle time

NOTE

Output timing is specified at a nominal 50 pF load.

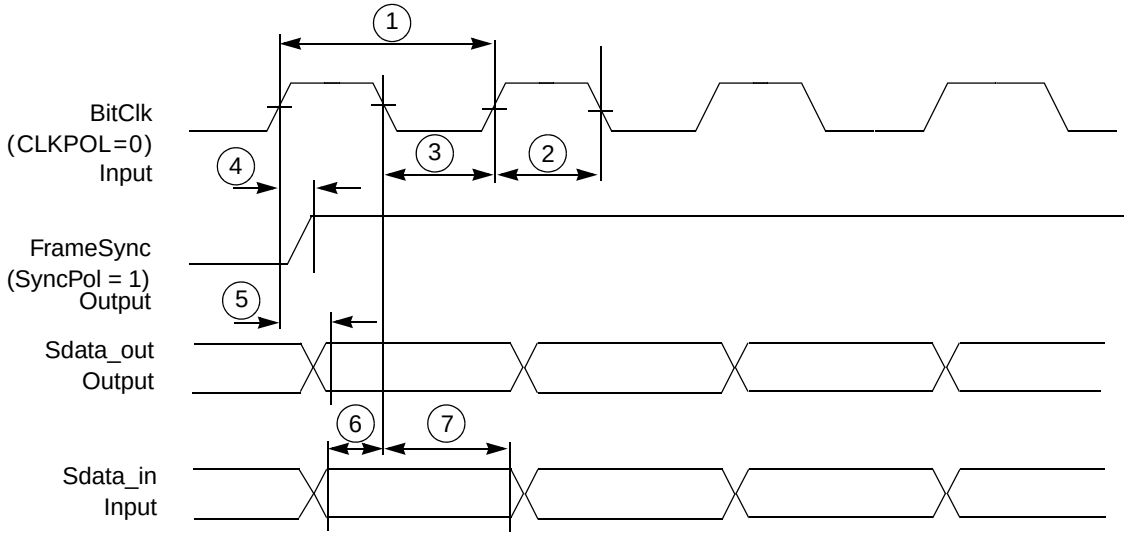

Figure 49. Timing Diagram – AC97 Mode

3.3.20.3 SPI Mode

Table 45. Timing Specifications – SPI Master Mode, Format 0 (CPHA = 0)

Symbol	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A20.26
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A20.27
3	Slave select clock delay, programable in the PSC CCS register	30.0	—	ns	A20.28
4	Output Data valid after Slave Select ($\overline{SS}$)	—	8.9	ns	A20.29
5	Output Data valid after SCK	—	8.9	ns	A20.30
6	Input Data setup time	6.0	—	ns	A20.31
7	Input Data hold time	1.0	—	ns	A20.32
8	Slave disable lag time	—	TSCK	ns	A20.33
9	Sequential Transfer delay, programmable in the PSC CTUR / CTLR register	15.0	—	ns	A20.34
10	Clock falling time	—	7.9	ns	A20.35
11	Clock rising time	—	7.9	ns	A20.36

NOTE

Output timing is specified at a nominal 50 pF load.

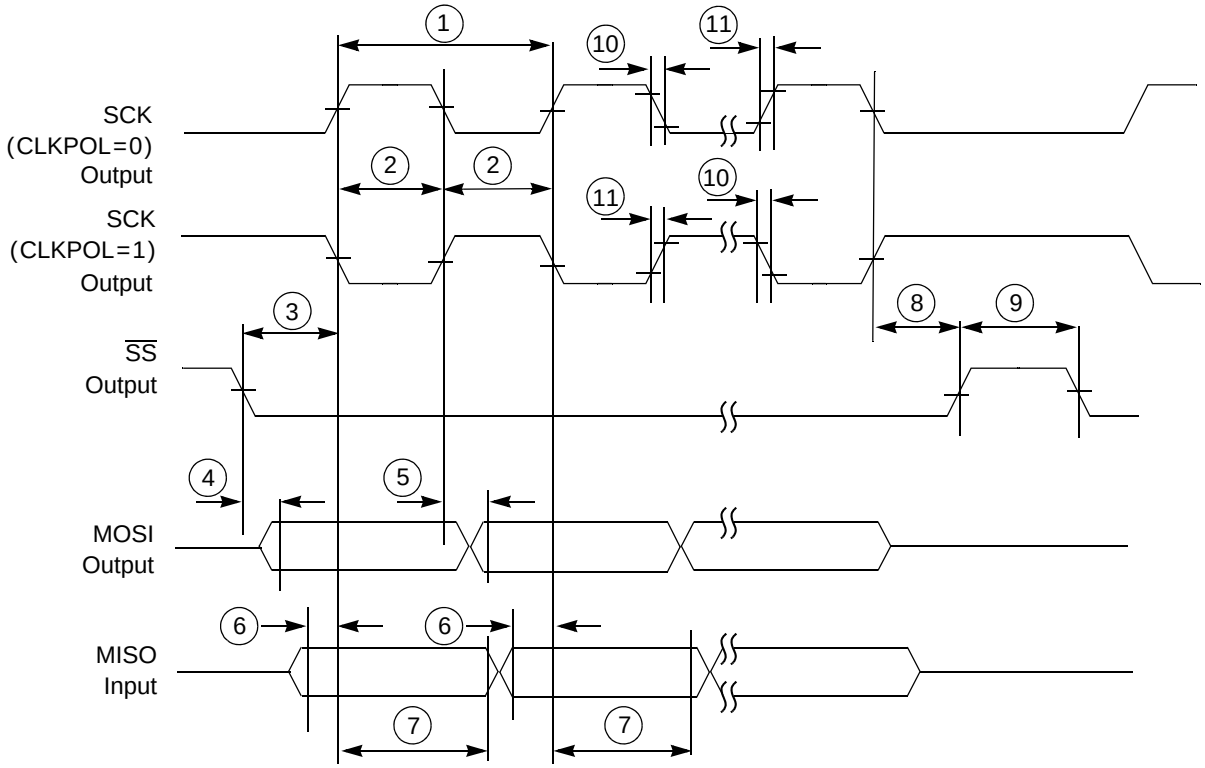

Figure 50. Timing Diagram – SPI Master Mode, Format 0 (CPHA = 0)

Table 46. Timing Specifications – SPI Slave Mode, Format 0 (CPHA = 0)

Symbol	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A20.37
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A20.38
3	Slave select clock delay	1.0	—	ns	A20.39
4	Input Data setup time	1.0	—	ns	A20.40
5	Input Data hold time	1.0	—	ns	A20.41
6	Output data valid after $\overline{SS}$	—	14.0	ns	A20.42
7	Output data valid after SCK	—	14.0	ns	A20.43
8	Slave disable lag time	0.0	—	ns	A20.44
9	Minimum Sequential Transfer delay = 2 × IP Bus clock cycle time	30.0	—	—	A20.45

NOTE

Output timing is specified at a nominal 50 pF load.

3.3.24 VIU

The Video Input Unit (VIU) is an interface which accepts the ITU656 format compatible video stream.

Figure 58 shows the VIU interface timing and Table 52 lists the timing parameters.

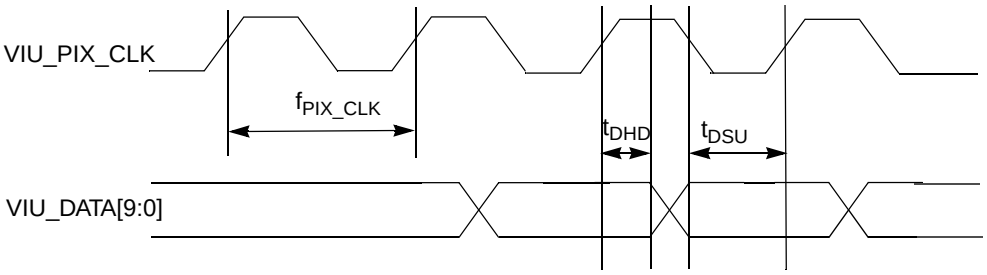

Figure 58. VIU Interface Timing Diagram

Table 52. VIU Interface Timing Parameters

Parameter	Description	Min	Typ	Max	Unit	SpecID
f_{PIX_CK}	VIU Pixel Clock Frequency	—	—	83	MHz	A24.1
t_{DSU}	VIU Data Setup Time	2.5	—	—	ns	A24.2
t_{DHD}	VIU Data Hold Time	2.5	—	—	ns	A24.3

4 System Design Information

4.1 Power Up/Down Sequencing

Power sequencing between the 1.4 V power supply V_{DD_CORE} and the remaining supplies is required to prevent excessive current during power up phase.

The required power sequence is as follows:

- Use 12 V/millisecond or slower time for all supplies.
- Power up V_{DD_IO}, PLL_AV_{DD}, V_{BAT_RTC} (if not applied permanently), $V_{DD\_MEM\_IO}$, USB PHY, and SATA PHY supplies first in any order and then power up V_{DD_CORE}. If required, AV_{DD_FUSEWR} should be powered up afterwards.
- All the supplies must reach the specified operating conditions before the $\overline{\text{PORESET}}$ can be released.
- For power down, drop AV_{DD_FUSEWR} to 0 V first, drop V_{DD_CORE} to 0 V, and then drop all other supplies.
- V_{DD_CORE} should not exceed V_{DD_IO}, $V_{DD\_MEM\_IO}$, V_{BAT_RTC}, or PLL_AV_{DD}s by more than 0.4 V at any time, including power-up.

4.2 System and CPU Core AVDD Power Supply Filtering

Each of the independent PLL power supplies require filtering external to the device. The following drawing Figure 59 is a recommendation for the required filter circuit.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits.

All traces should be as low impedance as possible, especially ground pins to the ground plane.

The filter for System/Core $PLLV_{DD}$ to V_{SS} should be connected to the power and ground planes, respectively, not fingers of the planes.

In addition to keeping the filter components for System/Core $PLLV_{DD}$ as close as practical to the body of the MPC5121e as previously mentioned, special care should be taken to avoid coupling switching power supply noise or digital switching noise onto the portion of that supply between the filter and the MPC5121e.

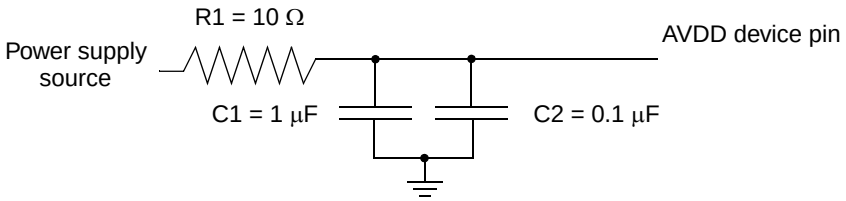

Figure 59. Power Supply Filtering

The capacitors for C2 in Figure 59 should be rated X5R or better due to temperature performance. It is recommended to add a bypass capacitance of at least 1 µF for the V_{BAT_RTC} pin.

4.3 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to V_{DD_IO}. Unused active high inputs should be connected to V_{SS}. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} and V_{SS} pins of the MPC5121e/MPC5123.

The unused AV_{DD_FUSEWR} power should be connected to V_{SS} directly or via a resistor.

For DDR or LPDDR modes the unused pins MVTT[3:0] for DDR2 Termination voltage can be unconnected.

6 Product Documentation

This Data Sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com.

Table 55 provides a revision history for this document.

Table 55. Document Revision History

Revision	Substantive Change(s)
Rev. 0, DraftA	First Draft (5/2008)
Rev. 0, DraftB	Second Draft (5/2008)
Rev. 0, DraftC	Third Draft (7/2008)
Rev. 1	Advance Information (10/2008)
Rev. 2	Technical Data (2/2009)
Rev. 3	Technical Data (2/2009). Corrected Table 5, Footnote 3.
Rev. 3.1	Technical Data (12/2009). Interim release for removing AVDD_FUSERD throughout document, changing pin D9 to VDD_IO, and adding D9 to list of pins for VDD_IO.
Rev. 4	Technical Data (1/2010). Minor editorial and graphical updates. No technical updates.
Rev 5	— Updated table “DDR and DDR2 SDRAM Timing Specification”, removed the row of ‘MCK AC differential crosspoint voltage' . — Updated table “Thermal Resistance Data”. — Added table “NFC Timing Characteristics in Symmetric Mode ”and added figure “Read data latch timing in Symmetric Mode”. —Published as Rev. 5