Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	e300
Core Size	32-Bit Single-Core
Speed	400MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, USB OTG
Peripherals	DMA, WDT
Number of I/O	147
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc5123yvy400b

Table of Contents

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 9 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
TDI	Y23	General IO	V_{DD_IO}	3
TDO	W22	General IO	V_{DD_IO}	—
TMS	Y25	General IO	V_{DD_IO}	3
$\overline{\text{TRST}}$	AA26	General IO	V_{DD_IO}	3
Test / Debug (2 Total)				
TEST	W25	General IO	V_{DD_IO}	4, 5
$\overline{\text{CKSTP\_OUT}}$	Y26	General IO	V_{DD_IO}	—
System Control (3 Total)				
$\overline{\text{HRESET}}$	W24	General IO	V_{DD_IO}	6, 2
$\overline{\text{PORESET}}$	W23	General IO	V_{DD_IO}	4, 2
$\overline{\text{SRESET}}$	V22	General IO	V_{DD_IO}	6, 2
System Clock (2 Total)				
SYS_XTALI	V24	Analog Input	SYS_PLL_AVDD	Oscillator Input
SYS_XTALO	W26	Analog Output	SYS_PLL_AVDD	Oscillator Output
RTC (3 Total)				
RTC_XTALI	C20	Analog Input	VBAT_RTC	Oscillator Input
RTC_XTALO	A20	Analog Output	VBAT_RTC	Oscillator Output
$\overline{\text{HIB\_MODE}}$	D18	Analog Output	VBAT_RTC	—
GP Input Only (4 Total)				
GPIO28	A19	Analog Input	VBAT_RTC	—
GPIO29	E17	Analog Input	VBAT_RTC	—
GPIO30	C18	Analog Input	VBAT_RTC	—
GPIO31	B18	Analog Input	VBAT_RTC	—
DDR Reference Voltage				
MVREF	AB11	Analog Input	Voltage Reference for SSTL input pads	
USB – PHY without Power and Ground Supplies (7 Total)				
USB_XTALI	C24	Analog Input	USB_PLL_PWR3	Oscillator Input
USB_XTALO	B24	Analog Output	USB_PLL_PWR3	Oscillator Output
USB_DP	A23	Analog IO	USB_VDDA	—
USB_DM	A22	Analog IO	USB_VDDA	—
USB_TPA	A24	Analog Output	—	USB PHY debug output
USB_VBUS	D21	Analog IO	—	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 11 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
V_{SS}	A2, A3, A25, B1,B2, B3, B5, B7, B12, B17, B20, B22, B26, C1, C4, C23, C25, D2, D12, D17, D24, D25, E18, F2, F3, F4, F5, F6, F8, F10, F16, F17, F21, G5, H6, H23, H25, K6, K21, L6, L11, L12, L13, L14, L15, L16, L21, M2, M4, M11, M12, M13, M14, M15, M16, N5, N11, N12, N13, N14, N15, N16,	Ground	—	—
V_{SS}	N23, N25, P11, P12, P13, P14, P15, P16, R11, R12, R13, R14, R15, R16, T6, T11, T12, T13, T14, T15, T16, T21, U2, U4, U6, U21, V23, V25, Y24, AA6, AA10, AA11, AA16, AA17, AA21, AB2, AB4, AB10, AB24, AC8, AC12, AC17, AC22, AD3, AD25, AE7, AE12, AE17, AE23, AE26	Ground	—	—
SYS_PLL_AVDD	T22	Analog Power	—	—
SYS_PLL_AVSS	U22	Analog Ground	—	—
CORE_PLL_AVDD	AA19	Analog Power	—	—
CORE_PLL_AVSS	AD23	Analog Ground	—	—
VBAT_RTC	D19	Power	—	—
AVDD_FUSEWR	C9	Power	—	—
MVTT0	AB7	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
MVTT1	AF9	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
MVTT2	AE11	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
MVTT3	AE14	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
Power and Ground Supplies (USB PHY)				
USB_PLL_GND	E23	Analog Ground	—	—
USB_PLL_PWR3	D23	Analog Power	—	—
USB_RREF	E22	Analog Power	—	—
USB_VSSA_BIAS	B23	Analog Ground	—	—

3 Electrical and Thermal Characteristics

3.1 DC Electrical Characteristics

3.1.1 Absolute Maximum Ratings

The tables in this section describe the MPC5121e/MPC5123 DC Electrical characteristics. Table 4 gives the absolute maximum ratings.

Table 4. Absolute Maximum Ratings[1]

Characteristic	Symbol	Min	Max	Unit	SpecID
Supply voltage – e300 core and peripheral logic	V_{DD_CORE}	–0.3	1.47	V	D1.1
Supply voltage – I/O buffers	V_{DD_IO}, $V_{DD\_MEM\_IO}$	–0.3	3.6	V	D1.2
Input reference voltage (DDR/DDR2)	MVREF	–0.3	3.6	V	
Termination Voltage (DDR2)	MVTT	–0.3	3.6	V	
Supply voltage – System APLL, System Oscillator	SYS_PLL_AVDD	–0.3	3.6	V	D1.3
Supply voltage – e300 APLL	CORE_PLL_AVDD	–0.3	3.6	V	D1.4
Supply voltage – RTC (Hibernation)	VBAT_RTC	–0.3	3.6	V	D1.5
Supply voltage – FUSE Programming	AVDD_FUSEWR	–0.3	3.6	V	D1.6
Supply voltage – SATA PHY analog	SATA_VDDA_3P3	–0.3	3.6	V	D1.8
Supply voltage – SATA PHY voltage regulator	SATA_VDDA_VREG	–0.3	2.6	V	D1.9
Supply voltage – SATA PHY Tx/Rx	SATA_VDDA_1P2	–0.3	1.47	V	D1.10
Supply voltage – SATA PHY PLL	SATA_PLL_VDDA1P2	–0.3	1.47	V	D1.11
Supply voltage – USB PHY PLL and OSC	USB_PLL_PWR3	–0.3	3.6	V	D1.12
Supply voltage – USB PHY transceiver	USB_VDDA	–0.3	3.6	V	D1.13
Supply voltage – USB PHY bandgap bias	USB_VDDA_BIAS	–0.3	3.6	V	D1.14
Input voltage – USB PHY cable	USB_VBUS	–0.3	3.6	V	D1.15
Input voltage (V_{DD_IO})	Vin	–0.3	V_{DD_IO} + 0.3	V	D1.16
Input voltage ($V_{DD\_MEM\_IO}$)	Vin	–0.3	$V_{DD\_MEM\_IO}$ + 0.3	V	D1.17
Input voltage (VBAT_RTC)	Vin	–0.3	VBAT_RTC + 0.3	V	D1.18
Input voltage overshoot	Vinos	—	1	V	D1.19
Input voltage undershoot	Vinus	—	1	V	D1.20
Storage temperature range	Tstg	–55	150	^{o}C	D1.21

1 Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage.

Table 9. Power Dissipation (continued)

Core Power Supply (V_{DD_CORE})			SpecID
Mode	High-Performance	Unit	
	e300 = 300 MHz, CSB = 200 MHz		
Typical	300	mW	D5.5
PHY Power Supplies (USB_VDDA, SATA_VDDA)			
Typical	200	mW	D5.6

1 Typical core power is measured at V_{DD_CORE} = 1.4 V, T_j = 25 °C.

NOTE

The maximum power depends on the supply voltage, process corner, junction temperature, and the concrete application and clock configurations.
The worst case power consumption could reach a maximum of 2000 mW.

3.1.6 Thermal Characteristics

Table 10. Thermal Resistance Data

Rating	Board Layers	Symbol	TEPBGA	TEPBGA 2	Value	Unit	SpecID
Junction to Ambient Natural Convection[1,2]	Single layer board (1s)	$R_{\theta JA}$	31	24	30	°C/W	D6.1
Junction to Ambient Natural Convection[1,3]	Four layer board (2s2p)	$R_{\theta JMA}$	22	17	22	°C/W	D6.2
Junction to Ambient (@200 ft/min)[1,3]	Single layer board (1s)	$R_{\theta JMA}$	25	19	24	°C/W	D6.3
Junction to Ambient (@200 ft/min)[1,3]	Four layer board (2s2p)	$R_{\theta JMA}$	19	14	19	°C/W	D6.4
Junction to Board[4]	—	$R_{\theta JB}$	14	9	14	°C/W	D6.5
Junction to Case[5]	—	$R_{\theta JC}$	9	7	8	°C/W	D6.6
Junction to Package Top[6]	Natural Convection	Ψ_{JT}	2	7	2	°C/W	D6.7

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4 Fall time is measured from 20% of vdd to 80% of V_{DD}.
5 SYS_XTALI duty cycle is measured at V_M.

3.2.2 RTC Oscillator Electrical Characteristics

Table 13. RTC Oscillator Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit	SpecID
RTC_XTALI frequency	f_{rtc_xtal}	—	32.768	—	kHz	O2.1

3.2.3 System PLL Electrical Characteristics

Table 14. System PLL Specifications

Characteristic	Symbol	Min	Typical	Max	Unit	SpecID
Sys PLL input clock frequency[1]	f_{sys_xtal}	16	33.3	67	MHz	O3.1
Sys PLL input clock jitter[2]	t_{jitter}	—	—	10	ps	O3.2
Sys PLL VCO frequency[1]	f_{VCOsys}	400	—	800	MHz	O3.3
Sys PLL VCO output jitter (Dj), peak to peak / cycle	$f_{VCOjitterDj}$	—	—	40	ps	O3.4
Sys PLL VCO output jitter (Rj), RMS 1 sigma	$f_{VCOjitterRj}$	—	—	12	ps	O3.5
Sys PLL relock time—after power up[3]	t_{lock1}	—	—	200	µs	O3.6
Sys PLL relock time—when power was on[4]	t_{lock2}	—	—	170	µs	O3.7

1 The SYS_XTALI frequency and PLL Configuration bits must be chosen such that the resulting system frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
2 This represents total input jitter—short term and long term combined. Two different types of jitter can exist on the input to CORE_SYSCLK, systemic and true random jitter. True random jitter is rejected. Systemic jitter is passed into and through the PLL to the internal clock circuitry.
3 PLL relock time is the maximum amount of time required for the PLL lock after a stable VDD and CORE_SYSCLK are reached during the power-on reset sequence.
4 PLL relock time is the maximum amount of time required for the PLL lock after the PLL has been disabled and subsequently re-enabled during sleep modes.

3.2.4 e300 Core PLL Electrical Characteristics

The internal clocking of the e300 core is generated from and synchronized to the system clock by means of a voltage-controlled core PLL.

Table 15. e300 PLL Specifications

Characteristic	Symbol	Min	Typical	Max	Unit	SpecID
e300 frequency[1]	f_{core}	200	—	400	MHz	O4.1
e300 PLL VCO frequency[1]	$f_{VCOcore}$	400	—	800	MHz	O4.3
e300 PLL input clock frequency	f_{CSB_CLK}	50	—	200	MHz	O4.4
e300 PLL input clock cycle time	t_{CSB_CLK}	5	—	20	ns	O4.5
e300 PLL relock time[2]	t_{lock}	—	—	200	µs	O4.6

[4] See the timing measurement conditions in the PCI Local Bus Specification.

For Measurement and Test Conditions, see the PCI Local Bus Specification.

3.3.7 LPC

The Local Plus Bus is the external bus interface of the MPC5121e/MPC5123. A maximum of eight configurable chip selects (CS) are provided. There are two main modes of operation: non-MUXed and MUXED. The reference clock is the LPC CLK. The maximum bus frequency is 83 MHz.

Definition of Acronyms and Terms:

WS = Wait State
DC = Dead Cycle
HC = Hold Cycle
DS = Data Size in Bytes
BBT = Burst Bytes per Transfer
AL = Address latch enable Length
ALT = Chip select/Address Latch Timing
t_{LPCck} = LPC clock period

Table 23. LPC Timing

Sym	Description	Min	Max	Units	SpecID
t_{OD}	$\overline{CS}$[x], ADDR, R/$\overline{W}$, TSIZ, DATA (wr), $\overline{TS}$, $\overline{OE}$ valid after LPC CLK (Output Delay related to LPC CLK)	0	5	ns	A7.1
t_1	Non-MUXed non-Burst $\overline{CS}$[x] pulse width	(2 + WS) × t_{LPCck}	(2 + WS) × t_{LPCck}	ns	A7.2
t_2	ADDR, R/$\overline{W}$, TSIZ, DATA (wr) valid before $\overline{CS}$[x] assertion	$t_{LPCck} - t_{OD}$	$t_{LPCck} + t_{OD}$	ns	A7.3
t_3	$\overline{OE}$ assertion after $\overline{CS}$[x] assertion	$t_{LPCck} - t_{OD}$	$t_{LPCck} + t_{OD}$	ns	A7.4
t_4	ADDR, R/$\overline{W}$, TSIZ, Data (wr) hold after $\overline{CS}$[x] negation	$t_{LPCck} - t_{OD}$	(HC + 1) × t_{LPCck} + t_{OD}	ns	A7.5
t_5	$\overline{TS}$ pulse width	t_{LPCck}	t_{LPCck}	ns	A7.6
t_6	DATA (rd) setup before LPC CLK	4	—	ns	A7.7
t_7	DATA (rd) input hold	0	(DC + 1) × t_{LPCck}	ns	A7.8
t_8	Non-MUXed read Burst $\overline{CS}$[x] pulse width	(2 + WS + BBT/DS) × t_{LPCck}	(2 + WS + BBT/DS) × t_{LPCck}	ns	A7.9
t_9	Burst $\overline{ACK}$ pulse width	(BBT/DS) × t_{LPCck}	(BBT/DS) × t_{LPCck}	ns	A7.10
t_{10}	Burst DATA (rd) input hold	0	—	ns	A7.11
t_{11}	Read Burst $\overline{ACK}$ assertion after $\overline{CS}$[x] assertion	(2 + WS) × t_{LPCck}	(2 + WS) × t_{LPCck}	ns	A7.12
t_{12}	Non-muxed write Burst $\overline{CS}$[x] pulse width	(2.5 + WS + BBT/DS) × t_{LPCck}	(2.5 + WS + BBT/DS) × t_{LPCck}	ns	A7.13
t_{13}	Write Burst ADDR, R/$\overline{W}$, TSIZ, DATA (wr) hold after $\overline{CS}$[x] negation	0.5 × t_{LPCck} – t_{OD}	(HC + 0.5) × t_{LPCck} + t_{OD}	ns	A7.14

3.3.7.1.4 Non-MUXed Asynchronous Read Burst Mode (Page Mode)

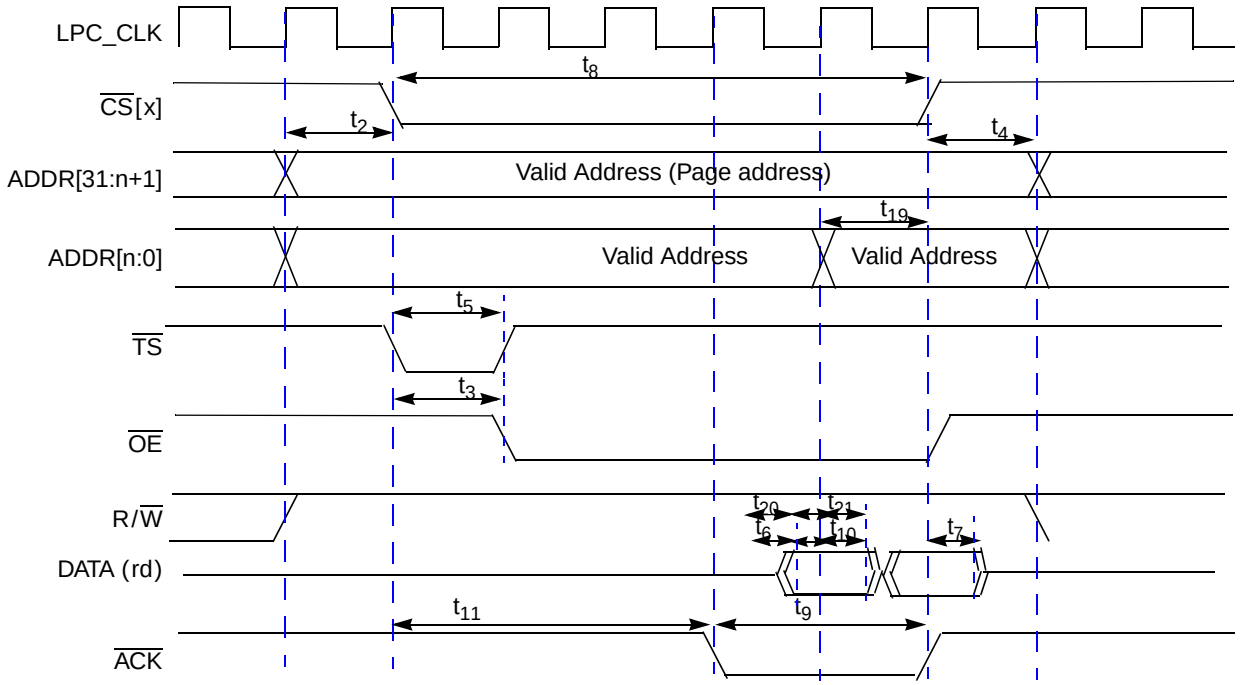

Figure 16. Timing Diagram – Non-MUXed Asynchronous Read Burst

3.3.7.1.5 Non-MUXed Aynchronous Write Burst Mode

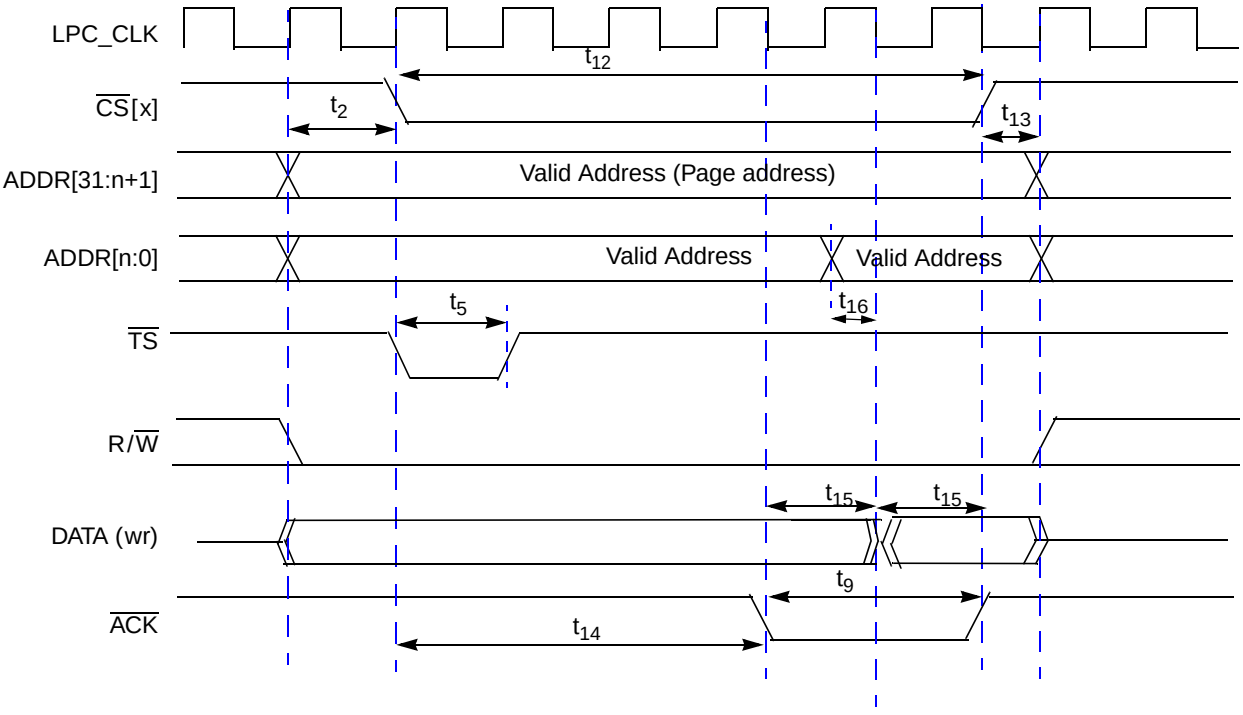

Figure 17. Timing Diagram – Non-MUXed Aynchronous Write Burst

3.3.7.2.2 MUXed Synchronous Read Burst Mode

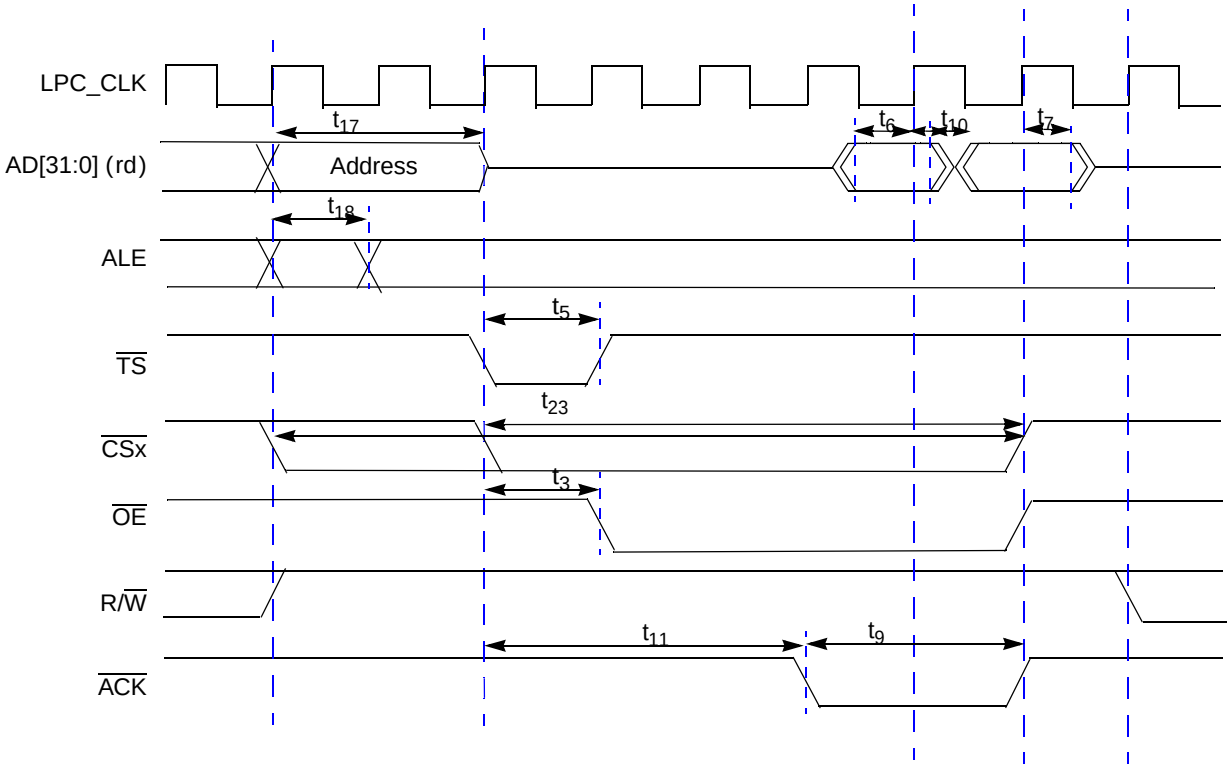

Figure 19. Timing Diagram – MUXed Synchronous Read Burst

3.3.7.2.3 MUXed Synchronous Write Burst Mode

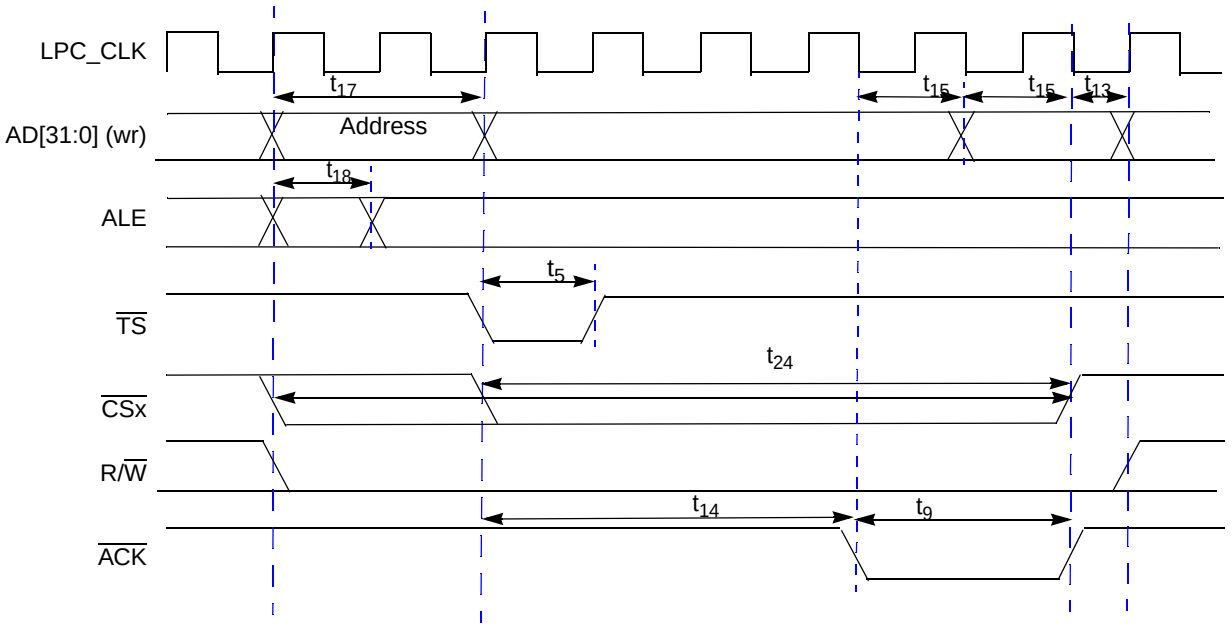

Figure 20. Timing Diagram – MUXed Synchronous Write Burst

3.3.8 NFC

The NAND flash controller (NFC) implements the interface to standard NAND Flash memory devices. This section describes the timing parameters of the NFC.

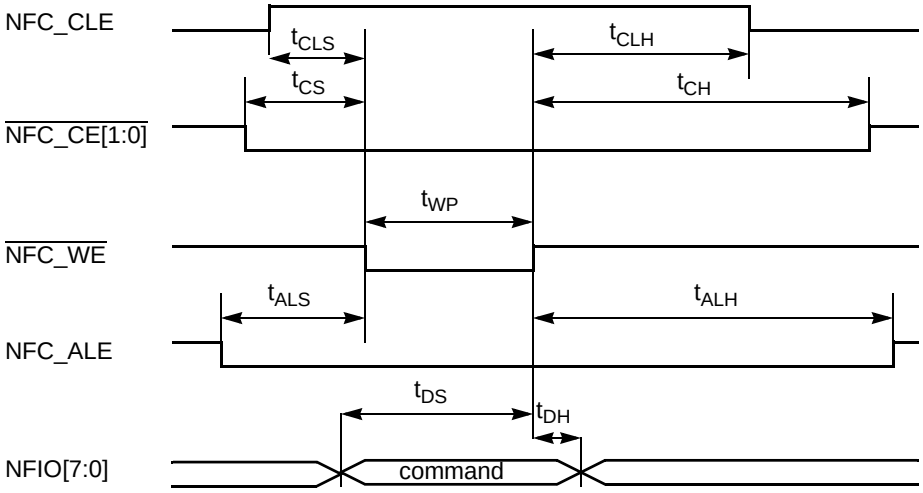

Figure 21. Command Latch Cycle Timing

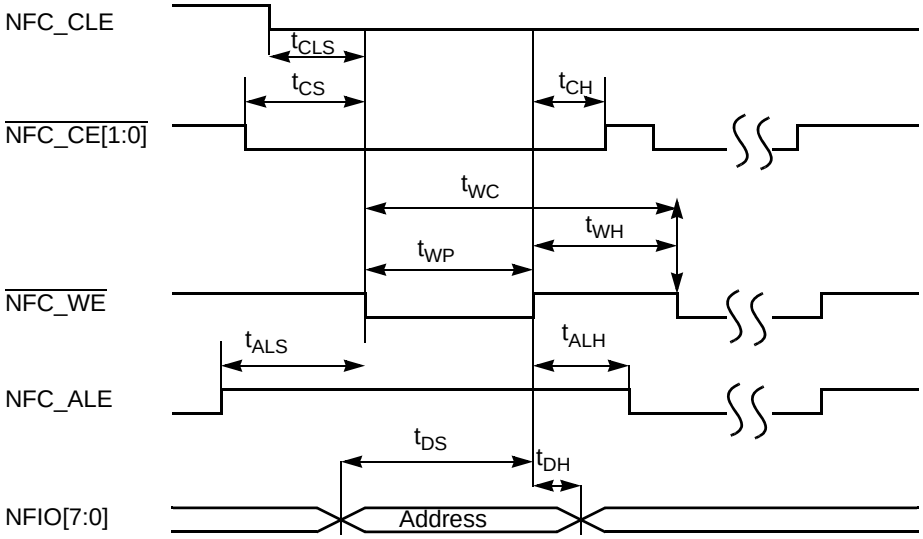

Figure 22. Address Latch Cycle Timing

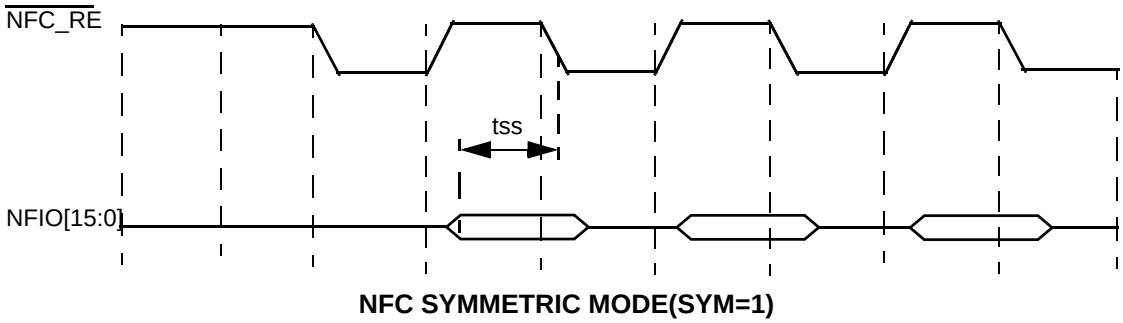

Figure 25. Read Data Latch Timing in Symmetric Mode

Table 24. NFC Timing Characteristics in asymmetric mode(SYM=0)[1]

Timing parameter	Description	Min. value	Max. value	Unit	SpecID
t_{CLS}	NFC_CLE setup Time	T + 1	—	ns	A8.1
t_{CLH}	NFC_CLE Hold Time	T – 1	—	ns	A8.2
t_{CS}	$\overline{\text{NFC\_CE}}$[1:0] Setup Time	2T – 1	—	ns	A8.3
t_{CH}	$\overline{\text{NFC\_CE}}$[1:0] Hold Time	3T	—	ns	A8.4
t_{WP}	$\overline{\text{NFC\_WP}}$ Pulse Width	T – 1	—	ns	A8.5
t_{ALS}	NFC_ALE Setup Time	T – 1	—	ns	A8.6
t_{ALH}	NFC_ALE Hold Time	T – 1	—	ns	A8.7
t_{DS}	Data Setup Time	T – 2	—	ns	A8.8
t_{DH}	Data Hold Time	T – 1	—	ns	A8.9
t_{WC}	Write Cycle Time	2T	—	ns	A8.10
t_{WH}	$\overline{\text{NFC\_WE}}$ Hold Time	T – 1	—	ns	A8.11
t_{RR}	Ready to $\overline{\text{NFC\_RE}}$ Low	5T + 2	—	ns	A8.12
t_{RP}	$\overline{\text{NFC\_RE}}$ Pulse Width	1.5T – 1	—	ns	A8.13
t_{RC}	READ Cycle Time	2T	—	ns	A8.14
t_{REH}	$\overline{\text{NFC\_RE}}$ High Hold Time	0.5T	—	ns	A8.15

1 T is the flash clock cycle.
T = 45 ns, frequency = 22 MHz (boot configuration, IP bus = 66 MHz)
T = 36 ns, frequency = 27 MHz (maximum configurable frequency, IP bus = 83 MHz)

Table 25. NFC Timing Characteristics in Symmetric mode(SYM=1)[1]

Timing Parameter	Description	Min. value	Max. value	Unit	SpecID
t_{CLS}	NFC_CLE Setup time	T	—	ns	A8.21
t_{CLH}	NFC_CLE Hold time	T	—	ns	A8.22
t_{CS}	NFC_CE[1:0] Setup time	T-2	—	ns	A8.23
t_{CH}	NFC_CE[1:0] Hold time	1.5T-1	—	ns	A8.24
t_{WP}	NFC_WE Pulse width	0.5T+1	—	ns	A8.25
t_{ALS}	NFC_ALE Setup time	T	—	ns	A8.26
t_{ALH}	NFC_ALE Hold time	T	—	ns	A8.27
t_{DS}	Data Setup time	0.5T-3	—	ns	A8.28
t_{DH}	Data Hold time	0.5T	—	ns	A8.29
t_{WC}	Write Cycle time	T	—	ns	A8.30
t_{WH}	NFC_WE Hold time	0.5T-1	—	ns	A8.31
t_{RR}	Ready to NFC_RE low	5T+2	—	ns	A8.32
t_{RP}	NFC_RE pulse width	0.5T	—	ns	A8.33
t_{RC}	Read Cycle time	T	—	ns	A8.34
t_{REH}	NFC_RE High hold time	0.5T	—	ns	A8.35
t_{SS}	NFC Read Data setup time	9.6	—	ns	A8.36

1 T is the flash clock cycle.
T = 45 ns, frequency = 22 MHz (boot configuration, IP bus = 66 MHz)
T = 36 ns, frequency = 27 MHz (maximum configurable frequency, IP bus = 83 MHz)

3.3.9 PATA

The MPC5121e/MPC5123 ATA Controller (PATA) is completely software programmable. It can be programmed to operate with ATA protocols using their respective timing, as described in the ANSI ATA-4 specification. The ATA interface is completely asynchronous in nature. Signal relationships are based on specific fixed timing in terms of timing units (nanoseconds).

ATA data setup and hold times, with respect to Read/Write strobes, are software programmable inside the ATA Controller. Data setup and hold times are implemented using counters. The counters count the number of ATA clock cycles needed to meet the ANSI ATA-4 timing specifications. For details, see the ANSI ATA-4 specification and how to program an ATA Controller and ATA drive for different ATA protocols and their respective timing. See the *MPC5121e Microcontroller Reference Manual*.

The MPC5121e/MPC5123 ATA Host Controller design makes data available coincidentally with the active edge of the WRITE strobe in PIO and Multiword DMA modes.

- Write data is latched by the drive at the inactive edge of the WRITE strobe. This gives ample setup-time beyond that required by the ATA-4 specification.
- Data is held unchanged until the next active edge of the WRITE strobe. This gives ample hold-time beyond that required by the ATA-4 specification.

Table 3-26. PATA Timing Parameters (continued)

Name	Meaning	Controlled by	Value	SpecID
t_{skew4}	Max difference in cable propagation delay between: ATA_IORDY and ATA_DATA (read)	Cable		A9.14
t_{skew5}	Max difference in cable propagation delay between: ATA_DIOR, ATA_DIOW, ATA_DMACK and ATA_CS0, ATA_CS1, ATA_DA2, ATA_DA1, ATA_DA0, ATA_DATA (write)	Cable		A9.15
tskew6	Max difference in cable propagation delay without accounting for ground bounce	Cable		A9.16

3.3.9.2 PIO Mode Timing

A timing diagram for the PIO read mode is given in Figure 26.

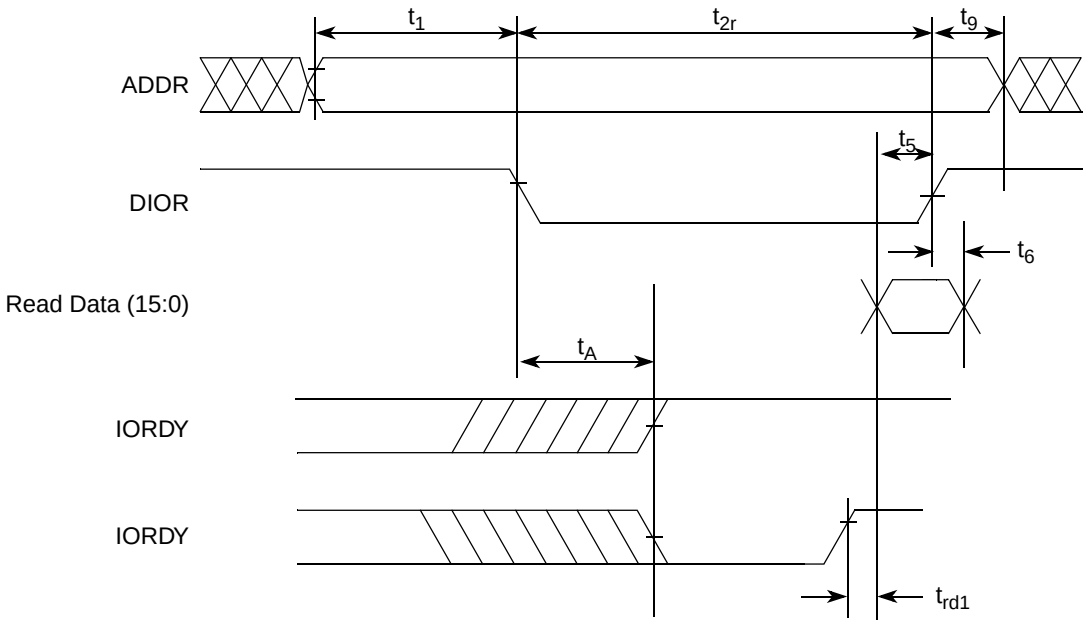

Figure 26. PIO Read Mode Timing

To fulfill read mode timing, the different timing parameters given in Table 3-27 must be observed.

Table 3-27. Timing Parameters PIO Read

ATA Parameter	PIO Read Mode Timing Parameter	Value	How to meet	SpecID
t_1	t_1	$t_1(min) = (time\_1 \times T) - (t_{skew1} + t_{skew2} + t_{skew5})$	calculate and programming time_1. [1]	A9.20
t_2	t_2r	$t_2(min) = (time\_2r \times T) - (t_{skew1} + t_{skew2} + t_{skew5})$	calculate and programming time_2r. [1]	A9.21
t_9	t_9	$t_9(min) = (time\_9 \times T) - (t_{skew1} + t_{skew2} + t_{skew6})$	calculate and programming time_9. [1]	A9.22

Table 3-27. Timing Parameters PIO Read (continued)

ATA Parameter	PIO Read Mode Timing Parameter	Value	How to meet	SpecID
t_5	t_5	$t_5(min) = t_{co} + t_{su} + t_{buf} + t_{buf} + t_{cable1} + t_{cable2}$	If not met, increase time_2r	A9.23
t_6	t_6	0	—	A9.24
t_A	t_A	$t_{A(min)} = (1.5 + time\_ax) \times T - (t_{co} + t_{sui} + t_{cable2} + t_{cable2} + 2 \times t_{buf})$	calculate and programming time_ax. [1]	A9.25
t_{rd}	t_{rd1}	$t_{rd1(max)} = (-t_{rd}) + (t_{skew3} + t_{skew4})$ $t_{rd1(min)} = (time\_pio\_rdx - 0.5) \times T - (t_{su} + t_{hi})$ $(time\_pio\_rdx - 0.5) \times T > t_{su} + t_{hi} + t_{skew3} + t_{skew4}$	calculate and programming time_pio_rdx. [1]	A9.26
t_0	—	$t_{0(min)} = (time\_1 + time\_2 + time\_9) \times T$	time_1, time_2r, time_9	A9.27

1 See the *MPC5121e Microcontroller Reference Manual.*

In PIO write mode, timing waveforms are somewhat different as shown in Figure 27.

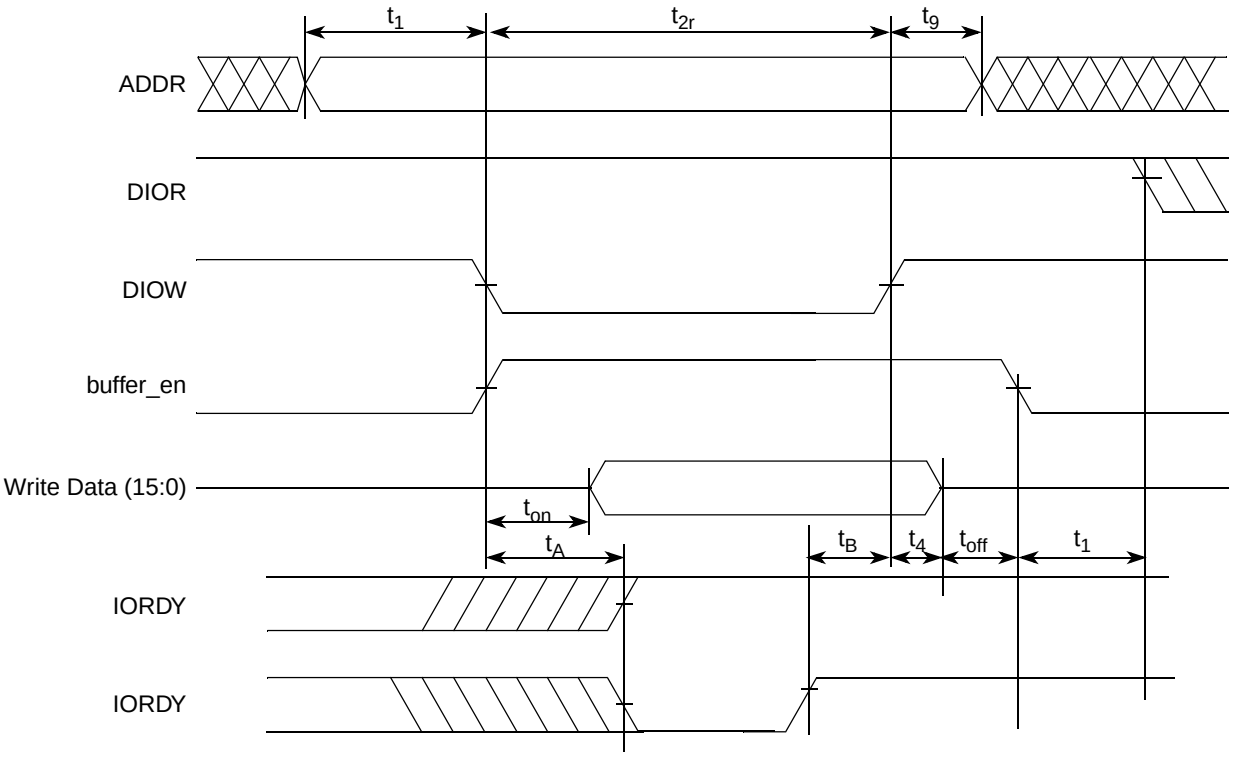

Figure 27. PIO Write Mode Timing

To fulfill this timing, several parameters need to be observed as shown in Table 3-28.

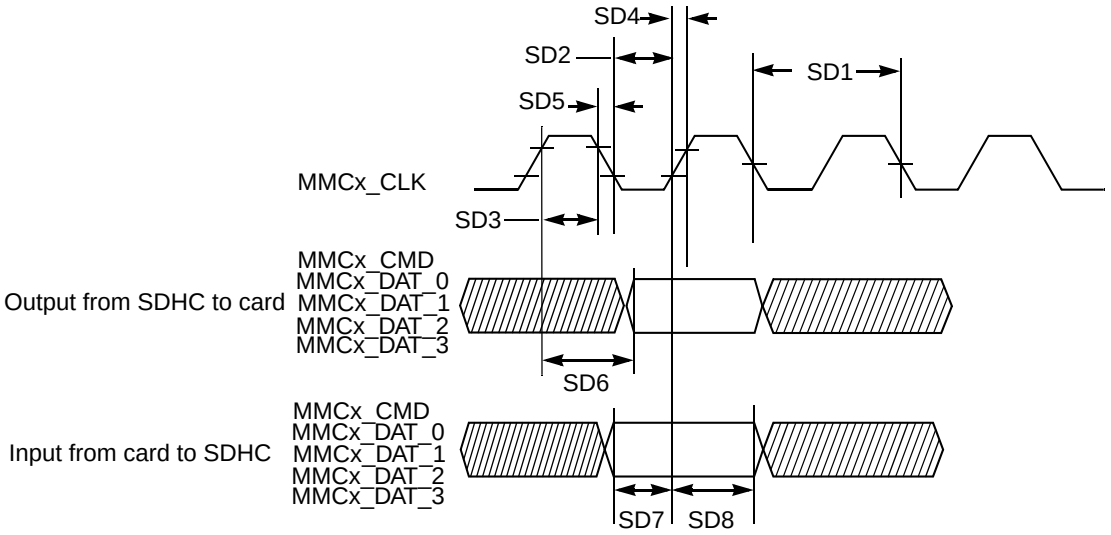

Figure 41. SDHC Timing Diagram

Table 37 lists the timing parameters.

Table 37. MMC/SD Interface Timing Parameters

ID	Parameter	Symbols	Min	Max	Unit	SpecID
Card Input Clock						
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz	A14.1
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz	A14.2
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz	A14.3
	Clock Frequency (Identification Mode)	f_{OD}[4]	100	400	kHz	A14.4
SD2	Clock Low Time (Full Speed/High Speed)	t_{WL}	10/7		ns	A14.5
SD3	Clock High Time (Full Speed/High Speed)	t_{WH}	10/7		ns	A14.6
SD4	Clock Rise Time (Full Speed/High Speed)	t_{TLH}		10/3	ns	A14.7
SD5	Clock Fall Time (Full Speed/High Speed)	t_{THL}		10/3	ns	A14.8
SDHC Output / Card Inputs CMD, DAT (Reference to CLK)						
SD6	SDHC Output Delay	t_{OD}	TH[5] – 3	TH+3	ns	A14.9
SDHC Input / Card Outputs CMD, DAT (Reference to CLK)						
SD7	SDHC Input Setup Time	t_{ISU}	2.5		ns	A14.10
SD8	SDHC Input Hold Time	t_{IH}	2.5		ns	A14.11

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal data transfer mode for SD/SDIO card, clock frequency can be any value between 0 ~ 25 MHz.

3 In normal data transfer mode for MMC card, clock frequency can be any value between 0 ~ 20 MHz.

4 In card identification mode, card clock must be 100 kHz ~ 400 kHz, voltage ranges from 2.7 to 3.6 V.

5 Suggested ClockPeriod = T, CLK_DIVIDER (in SDHC Clock Rate Register) = D, then TH = [(D + 1)/2]/(D + 1) × T where the value is rounded.

3.3.15 DIU

The DIU is a display controller designed to manage the TFT LCD display.

3.3.15.1 Interface to TFT LCD Panels, Functional Description

Figure 42 shows the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with positive polarity. The sequence of events for active matrix interface timing is:

- DIU_CLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, DIU_CLK runs continuously. This signal frequency could be from 5 to 100 MHz depending on the panel type.
- DIU_HSYNC causes the panel to start a new line. It always encompasses at least one DIU_CLK pulse.
- DIU_VSYNC causes the panel to start a new frame. It always encompasses at least one DIU_HSYNC pulse.
- DIU_DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

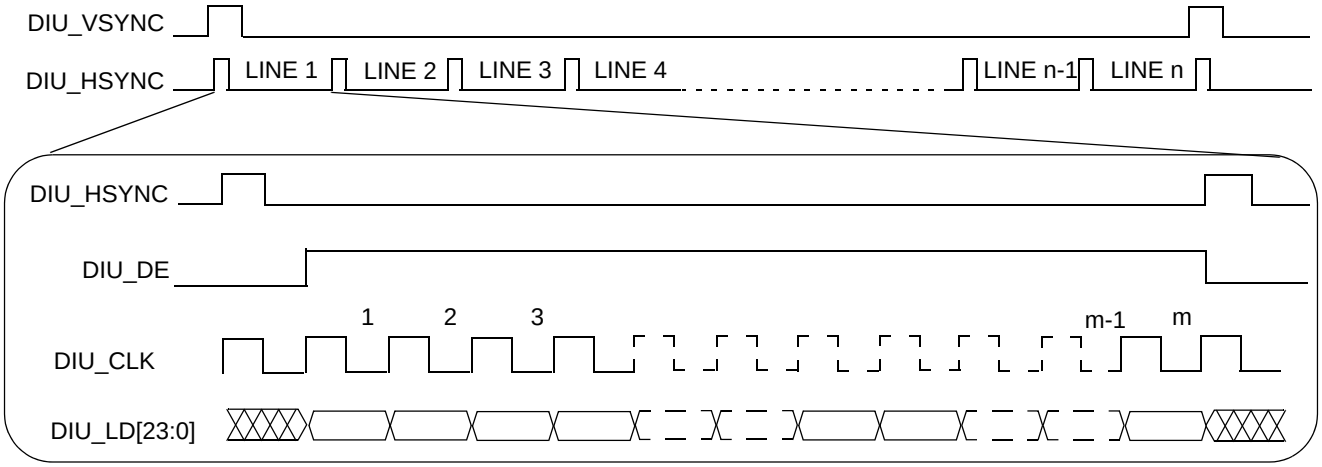

Figure 42. Interface Timing Diagram for TFT LCD Panels

3.3.15.2 Interface to TFT LCD Panels, Electrical Characteristics

Figure 43 shows the horizontal timing (timing of one line), including the horizontal sync pulse and the data. All parameters shown in the diagram are programmable. This timing diagram corresponds to positive polarity of the DIU_CLK signal (meaning the data and sync. signals change at the rising edge of it) and active-high polarity of the DIU_HSYNC, DIU_VSYNC and DIU_DE signal. You can select the polarity of the DIU_HSYNC and DIU_VSYNC signal via the SYN_POL register, whether active-high or active-low, the default is active-high. The DIU_DE signal is always active-high. And, pixel clock inversion and a flexible programmable pixel clock delay is also supported, programed via the DIU Clock Config Register (DCCR) in the system clock module.

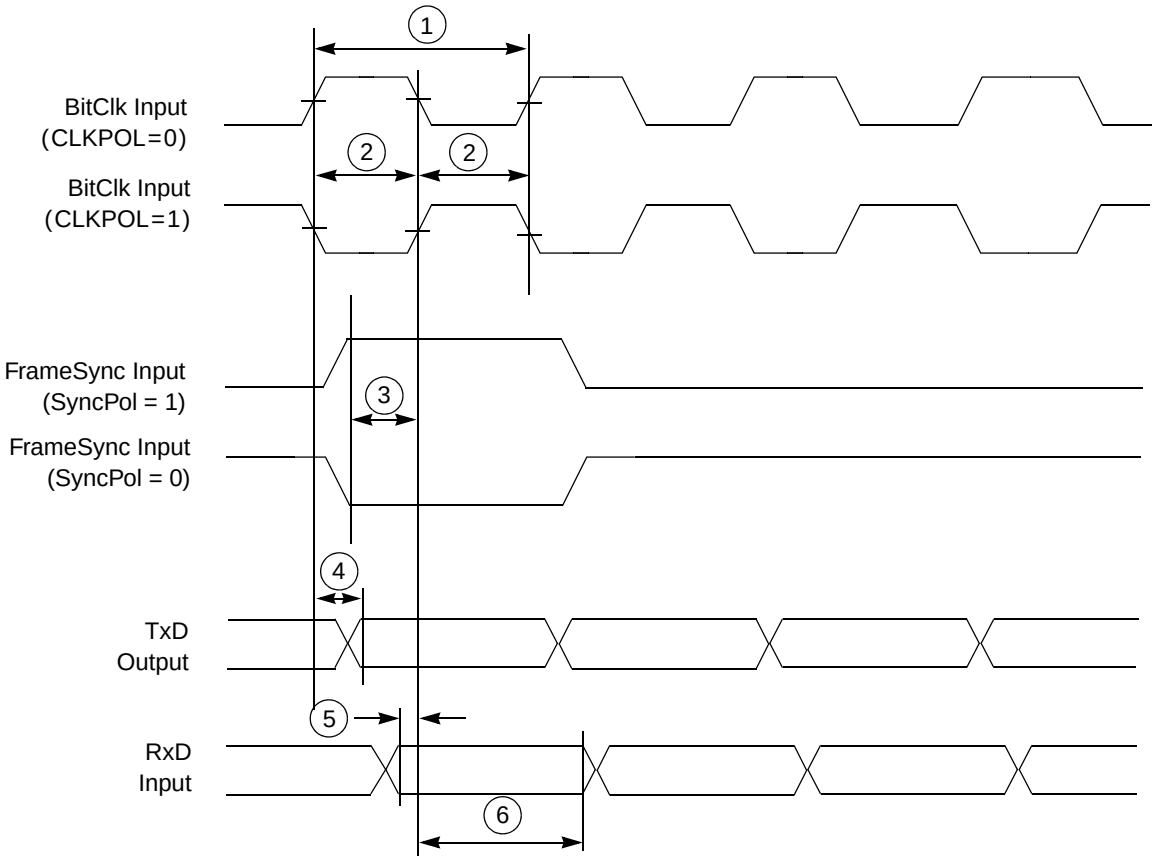

Figure 48. Timing Diagram – 8,16, 24, and 32-bit CODEC/I^{2}S Slave Mode

3.3.20.2 AC97 Mode

Table 44. Timing Specifications – AC97 Mode

Symbol	Description	Min	Typ	Max	Units	SpecID
1	Bit Clock cycle time	—	81.4	—	ns	A20.15
2	Clock pulse high time	—	40.7	—	ns	A20.16
3	Clock pulse low time	—	40.7	—	ns	A20.17
4	FrameSync valid after rising clock edge	—	—	13.0	ns	A20.18
5	Output Data valid after rising clock edge	—	—	14.0	ns	A20.19
6	Input Data setup time	1.0	—	—	ns	A20.20
7	Input Data hold time	1.0	—	—	ns	A20.21

NOTE

Output timing is specified at a nominal 50 pF load.

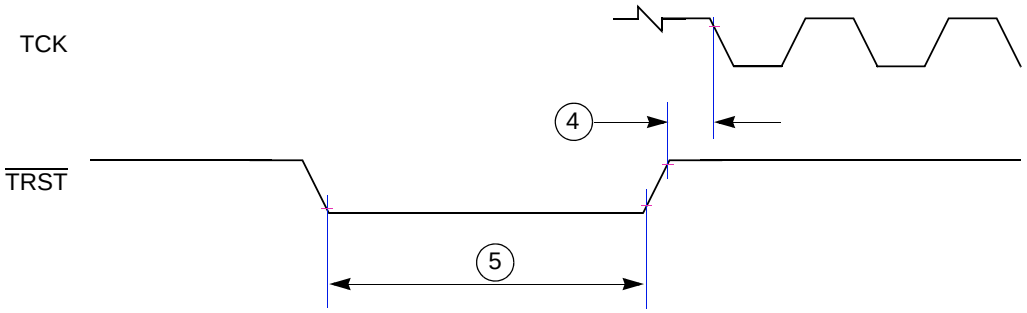

Figure 55. Timing Diagram – JTAG TRST

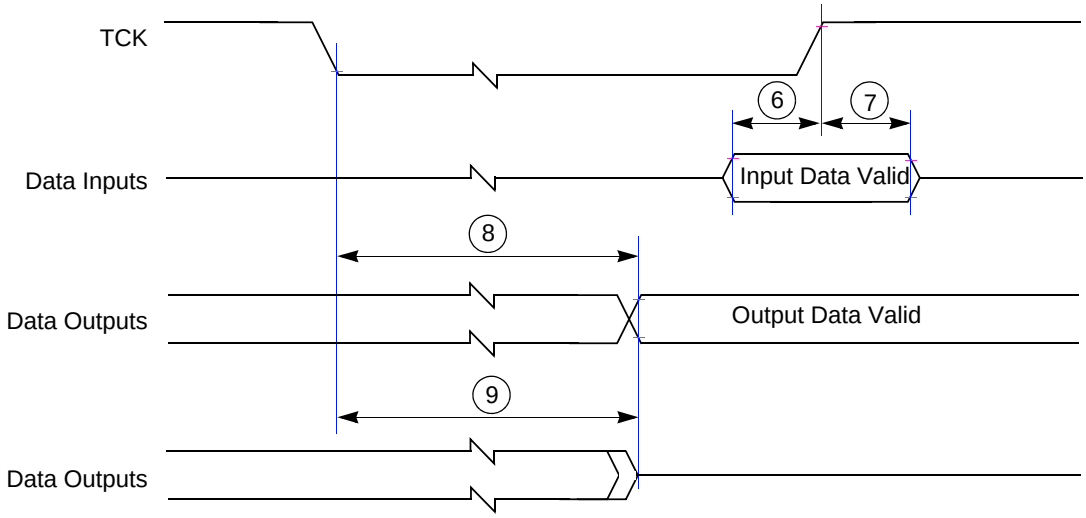

Figure 56. Timing Diagram – JTAG Boundary Scan

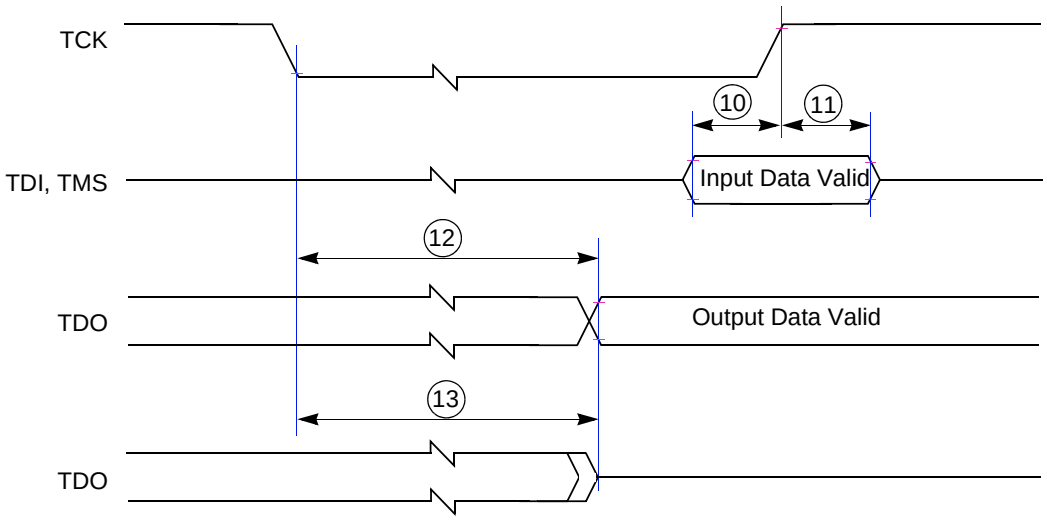

Figure 57. Timing Diagram – Test Access Port

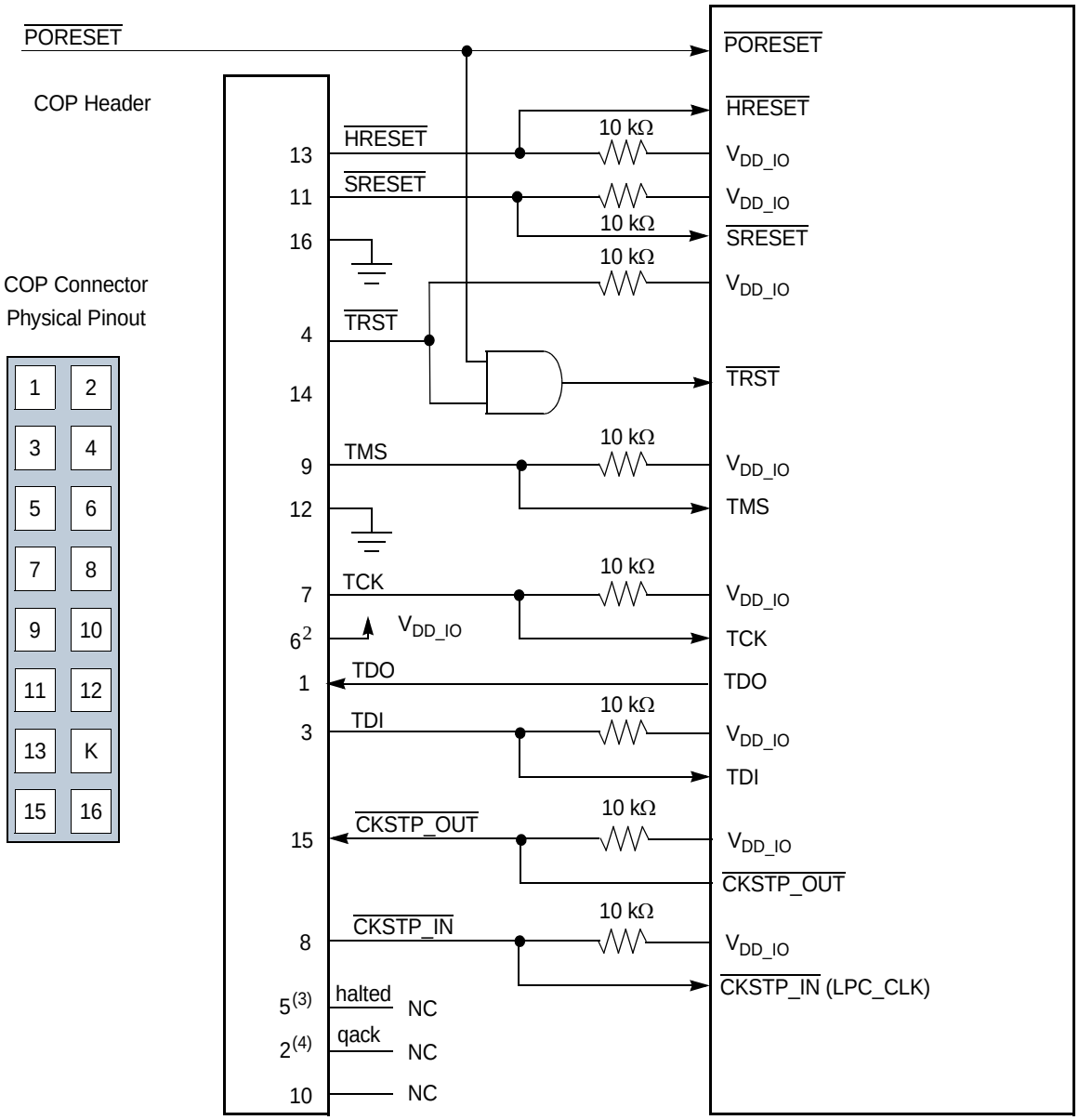

Figure 63. COP Connector Diagram

4.5.2.2 Boards Without COP Connector

If the JTAG interface is not used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{PORESET}}$, so that it is asserted when the system reset signal ($\overline{\text{PORESET}}$) is asserted. This ensures that the JTAG scan chain is initialized during power on. Figure 64 shows the connection of the JTAG interface without COP connector.

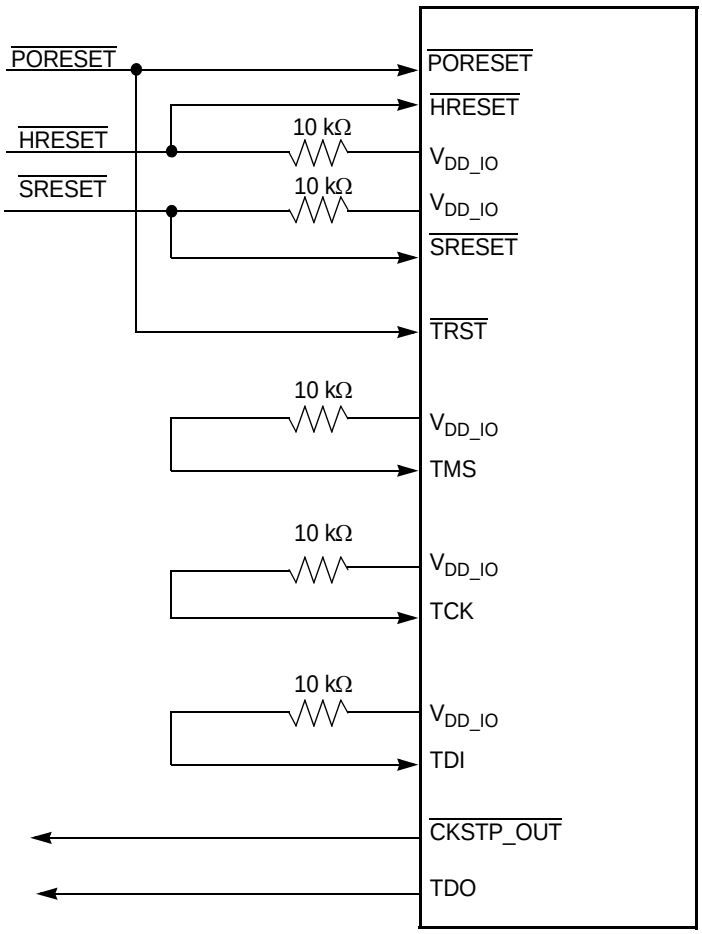

Figure 64. $\overline{\text{TRST}}$ Wiring for Boards without COP Connector