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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e300
Core Size	32-Bit Single-Core
Speed	400MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, USB OTG
Peripherals	DMA, WDT
Number of I/O	147
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/ppc5121vy400

Figure 1 shows a simplified MPC5121e/MPC5123 block diagram.

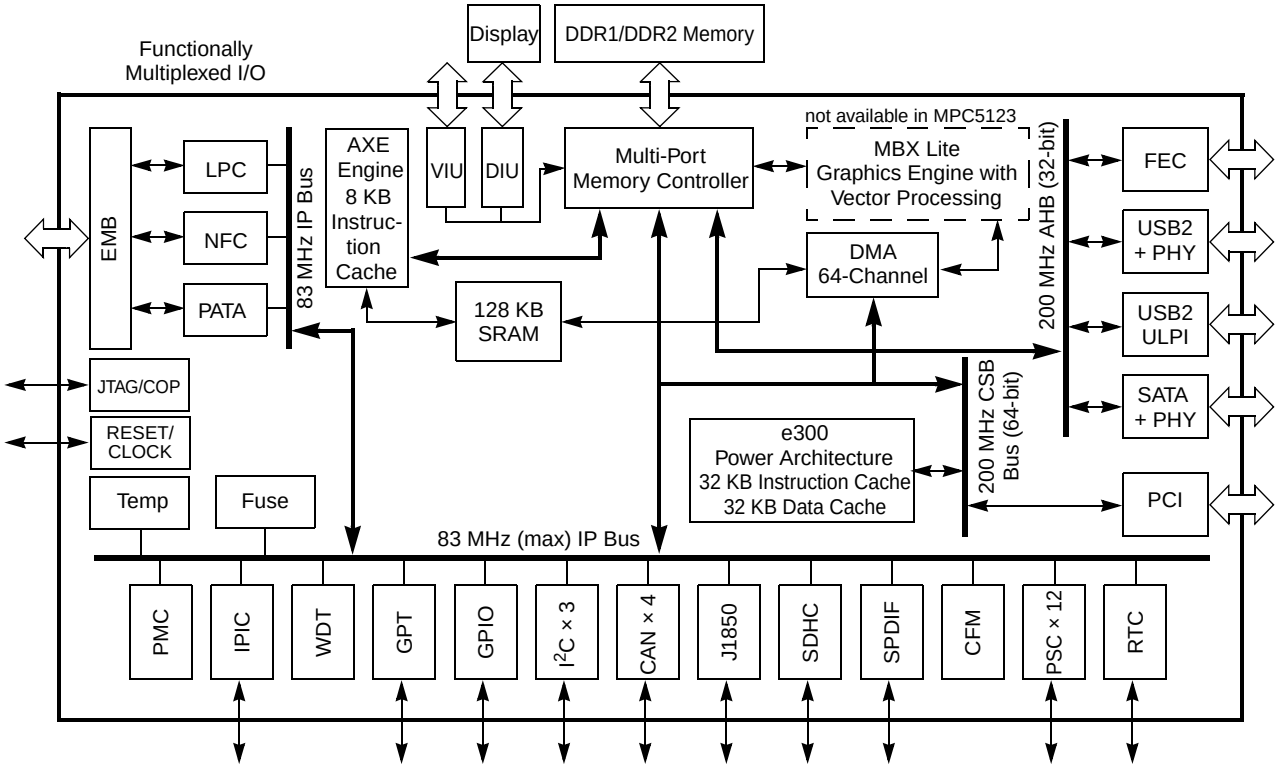

Figure 1. Simplified MPC5121e/MPC5123 Block Diagram

1 Ordering Information

Table 1. MPC5121e Orderable Part Numbers

Freescale Part Number	Speed (MHz)	Temperature (ambient)	Qualification	Package	Availability
MPC5121VY400B	400	0 °C to 70 °C	Consumer	RoHS and Pb-free	Tray
MPC5121VY400BR	400	0 °C to 70 °C	Consumer	RoHS and Pb-free	Tape and Reel
MPC5121YVY400B	400	–40 °C to 85 °C	Industrial	RoHS and Pb-free	Tray
MPC5121YVY400BR	400	–40 °C to 85 °C	Industrial	RoHS and Pb-free	Tape and Reel
SPC5121YVY400B	400	–40 °C to 85 °C	Automotive—AEC	RoHS and Pb-free	Tray
SPC5121YVY400BR	400	–40 °C to 85 °C	Automotive—AEC	RoHS and Pb-free	Tape and Reel

Table 2. MPC5123 Orderable Part Numbers

Freescale Part Number	Speed (MHz)	Temperature (ambient)	Qualification	Package	Availability
MPC5123VY400B	400	0 °C to 70 °C	Consumer	RoHS and Pb-free	Tray
MPC5123VY400BR	400	0 °C to 70 °C	Consumer	RoHS and Pb-free	Tape and Reel
MPC5123YVY400B	400	–40 °C to 85 °C	Industrial	RoHS and Pb-free	Tray

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 4 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
EMB_AD11	P3	General IO	V_{DD_IO}	—
EMB_AD10	N1	General IO	V_{DD_IO}	—
EMB_AD09	N2	General IO	V_{DD_IO}	—
EMB_AD08	N3	General IO	V_{DD_IO}	—
EMB_AD07	N4	General IO	V_{DD_IO}	—
EMB_AD06	M1	General IO	V_{DD_IO}	—
EMB_AD05	M3	General IO	V_{DD_IO}	—
EMB_AD04	M5	General IO	V_{DD_IO}	—
EMB_AD03	L1	General IO	V_{DD_IO}	—
EMB_AD02	L2	General IO	V_{DD_IO}	—
EMB_AD01	L3	General IO	V_{DD_IO}	—
EMB_AD00	L4	General IO	V_{DD_IO}	—
PATA Interface (9 Total)				
$\overline{\text{PATA\_CE1}}$	K1	General IO	V_{DD_IO}	ATA name: CS0
$\overline{\text{PATA\_CE2}}$	L5	General IO	V_{DD_IO}	ATA name: CS1
PATA_ISOLATE	K3	General IO	V_{DD_IO}	—
$\overline{\text{PATA\_IOR}}$	J1	General IO	V_{DD_IO}	ATA name: DIOR
$\overline{\text{PATA\_IOW}}$	K5	General IO	V_{DD_IO}	ATA name: DIOW
PATA_IOCHRDY	J2	General IO	V_{DD_IO}	ATA name: IORDY
PATA_INTRQ	J3	General IO	V_{DD_IO}	—
PATA_DRQ	J4	General IO	V_{DD_IO}	ATA name: DMARQ
$\overline{\text{PATA\_DACK}}$	H2	General IO	V_{DD_IO}	ATA name: DMACK
NFC Interface (7 Total)				
$\overline{\text{NFC\_WP}}$	G4	General IO	V_{DD_IO}	—
NFC_R/$\overline{\text{B}}$	H1	General IO	V_{DD_IO}	—
$\overline{\text{NFC\_WE}}$	G3	General IO	V_{DD_IO}	—
$\overline{\text{NFC\_RE}}$	G2	General IO	V_{DD_IO}	—
NFC_ALE	H4	General IO	V_{DD_IO}	—
NFC_CLE	H5	General IO	V_{DD_IO}	—
$\overline{\text{NFC\_CE0}}$	H3	General IO	V_{DD_IO}	—
I2C Interface (6 Total)				
I2C0_SCL	AC23	General IO	V_{DD_IO}	—
I2C0_SDA	AD26	General IO	V_{DD_IO}	—
I2C1_SCL	AB22	General IO	V_{DD_IO}	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 5 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
I2C1_SDA	AB23	General IO	V_{DD_IO}	—
I2C2_SCL	AC25	General IO	V_{DD_IO}	—
I2C2_SDA	AA22	General IO	V_{DD_IO}	—
IRQ Interface (2 Total)				
$\overline{IRQ0}$	AC26	General IO	V_{DD_IO}	—
$\overline{IRQ1}$	AB25	General IO	V_{DD_IO}	—
CAN Interface (4 Total)				
CAN1_RX	C19	Analog Input	VBAT_RTC	—
CAN1_TX	A18	General IO	V_{DD_IO}	—
CAN2_RX	B19	Analog Input	VBAT_RTC	—
CAN2_TX	E16	General IO	V_{DD_IO}	—
J1850 Interface (2 Total)				
J1850_TX	Y22	General IO	V_{DD_IO}	—
J1850_RX	AA24	General IO	V_{DD_IO}	—
SPDIF Interface (3 Total)				
SPDIF_TXCLK	AB21	General IO	V_{DD_IO}	—
SPDIF_TX	AD24	General IO	V_{DD_IO}	—
SPDIF_RX	AC24	General IO	V_{DD_IO}	—
PCI (54 Total)				
$\overline{PCI\_INTA}$	U23	PCI	V_{DD_IO}	—
$\overline{PCI\_RST\_OUT}$	F22	PCI	V_{DD_IO}	—
PCI_AD00	U24	PCI	V_{DD_IO}	—
PCI_AD01	V26	PCI	V_{DD_IO}	—
PCI_AD02	U25	PCI	V_{DD_IO}	—
PCI_AD03	R22	PCI	V_{DD_IO}	—
PCI_AD04	U26	PCI	V_{DD_IO}	—
PCI_AD05	T24	PCI	V_{DD_IO}	—
PCI_AD06	R23	PCI	V_{DD_IO}	—
PCI_AD07	T26	PCI	V_{DD_IO}	—
PCI_AD08	R26	PCI	V_{DD_IO}	—
PCI_AD09	P23	PCI	V_{DD_IO}	—
PCI_AD10	R24	PCI	V_{DD_IO}	—
PCI_AD11	R25	PCI	V_{DD_IO}	—
PCI_AD12	P26	PCI	V_{DD_IO}	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 7 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
$\overline{\text{PCI\_GNT0}}$	E25	PCI	V_{DD_IO}	—
$\overline{\text{PCI\_GNT1}}$	G22	PCI	V_{DD_IO}	—
$\overline{\text{PCI\_GNT2}}$	E24	PCI	V_{DD_IO}	—
PCI_CLK	C26	PCI	V_{DD_IO}	—
PSC Interface (61 Total)				
PSC_MCLK_IN	C17	General IO	V_{DD_IO}	—
PSC0_0	D16	General IO	V_{DD_IO}	—
PSC0_1	A17	General IO	V_{DD_IO}	—
PSC0_2	E15	General IO	V_{DD_IO}	—
PSC0_3	C16	General IO	V_{DD_IO}	—
PSC0_4	B16	General IO	V_{DD_IO}	—
PSC1_0	C15	General IO	V_{DD_IO}	—
PSC1_1	A16	General IO	V_{DD_IO}	—
PSC1_2	E14	General IO	V_{DD_IO}	—
PSC1_3	A15	General IO	V_{DD_IO}	—
PSC1_4	D14	General IO	V_{DD_IO}	—
PSC2_0	C14	General IO	V_{DD_IO}	—
PSC2_1	B14	General IO	V_{DD_IO}	—
PSC2_2	E13	General IO	V_{DD_IO}	—
PSC2_3	A14	General IO	V_{DD_IO}	—
PSC2_4	D13	General IO	V_{DD_IO}	—
PSC3_0	AF3	General IO	V_{DD_IO}	—
PSC3_1	AB5	General IO	V_{DD_IO}	—
PSC3_2	AC4	General IO	V_{DD_IO}	—
PSC3_3	AD4	General IO	V_{DD_IO}	—
PSC3_4	AF4	General IO	V_{DD_IO}	—
PSC4_0	AB1	General IO	V_{DD_IO}	—
PSC4_1	AA3	General IO	V_{DD_IO}	—
PSC4_2	AB3	General IO	V_{DD_IO}	—
PSC4_3	AA5	General IO	V_{DD_IO}	—
PSC4_4	AC2	General IO	V_{DD_IO}	—
PSC5_0	AC1	General IO	V_{DD_IO}	—
PSC5_1	AC3	General IO	V_{DD_IO}	—
PSC5_2	AD1	General IO	V_{DD_IO}	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 11 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
V_{SS}	A2, A3, A25, B1,B2, B3, B5, B7, B12, B17, B20, B22, B26, C1, C4, C23, C25, D2, D12, D17, D24, D25, E18, F2, F3, F4, F5, F6, F8, F10, F16, F17, F21, G5, H6, H23, H25, K6, K21, L6, L11, L12, L13, L14, L15, L16, L21, M2, M4, M11, M12, M13, M14, M15, M16, N5, N11, N12, N13, N14, N15, N16,	Ground	—	—
V_{SS}	N23, N25, P11, P12, P13, P14, P15, P16, R11, R12, R13, R14, R15, R16, T6, T11, T12, T13, T14, T15, T16, T21, U2, U4, U6, U21, V23, V25, Y24, AA6, AA10, AA11, AA16, AA17, AA21, AB2, AB4, AB10, AB24, AC8, AC12, AC17, AC22, AD3, AD25, AE7, AE12, AE17, AE23, AE26	Ground	—	—
SYS_PLL_AVDD	T22	Analog Power	—	—
SYS_PLL_AVSS	U22	Analog Ground	—	—
CORE_PLL_AVDD	AA19	Analog Power	—	—
CORE_PLL_AVSS	AD23	Analog Ground	—	—
VBAT_RTC	D19	Power	—	—
AVDD_FUSEWR	C9	Power	—	—
MVTT0	AB7	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
MVTT1	AF9	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
MVTT2	AE11	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
MVTT3	AE14	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
Power and Ground Supplies (USB PHY)				
USB_PLL_GND	E23	Analog Ground	—	—
USB_PLL_PWR3	D23	Analog Power	—	—
USB_RREF	E22	Analog Power	—	—
USB_VSSA_BIAS	B23	Analog Ground	—	—

3.1.3 DC Electrical Specifications

Table 6 gives the DC Electrical characteristics for the MPC5121e/MPC5123 at recommended operating conditions.

Table 6. DC Electrical Specifications

Characteristic	Condition	Symbol	Min	Max	Unit	SpecID
Input high voltage	Input type = TTL V_{DD_IO}	V_{IH}	0.51 × V_{DD_IO}	—	V	D3.1
Input high voltage	Input type = TTL $V_{DD\_MEM\_IO\_DDR}$	V_{IH}	MVREF + 0.15	—	V	D3.2
Input high voltage	Input type = TTL $V_{DD\_MEM\_IO\_DDR2}$	V_{IH}	MVREF + 0.125	—	V	D3.3
Input high voltage	Input type = TTL $V_{DD\_MEM\_IO\_LPDDR}$	V_{IH}	0.7 × $V_{DD\_MEM\_IO\_LPDDR}$	—	V	D3.4
Input high voltage	Input type = PCI V_{DD_IO}	V_{IH}	0.5 × V_{DD_IO}	—	V	D3.5
Input high voltage	Input type = Schmitt V_{DD_IO}	V_{IH}	0.65 × V_{DD_IO}	—	V	D3.6
Input high voltage	SYS_XTALI crystal mode[1] Bypass mode[2]	CV_{IH}	Vxtal + 0.4V (V_{DD_IO}/2) + 0.4V	—	V	D3.7
Input high voltage	SATA_XTALI crystal mode Bypass mode	SV_{IH}	Vxtal + 0.4V (V_{DD_IO}/2) + 0.4V	—	V	D3.8
Input high voltage	USB_XTALI crystal mode Bypass mode	UV_{IH}	Vxtal + 0.4V (V_{DD_IO}/2) + 0.4V	—	V	D3.9
Input high voltage	RTC_XTALI crystal mode[3] Bypass mode[4]	RV_{IH}	(VBAT_RTC/5) + 0.5V (VBAT_RTC/2) + 0.4V	—	V	D3.10
Input low voltage	Input type = TTL V_{DD_IO}	V_{IL}	—	0.42 × V_{DD_IO}	V	D3.11
Input low voltage	Input type = TTL $V_{DD\_MEM\_IO\_DDR}$	V_{IL}	—	MVREF – 0.15	V	D3.12
Input low voltage	Input type = TTL $V_{DD\_MEM\_IO\_DDR2}$	V_{IL}	—	MVREF – 0.125	V	D3.13
Input low voltage	Input type = TTL $V_{DD\_MEM\_IO\_LPDDR}$	V_{IL}	—	0.3 × $V_{DD\_MEM\_IO\_LPDDR}$	V	D3.14
Input low voltage	Input type = PCI V_{DD_IO}	V_{IL}	—	0.3 × V_{DD_IO}	V	D3.15
Input low voltage	Input type = Schmitt V_{DD_IO}	V_{IL}	—	0.35 × V_{DD_IO}	V	D3.16
Input low voltage	SYS_XTALI crystal mode Bypass mode	CV_{IL}	—	Vxtal – 0.4 (V_{DD_IO}/2) – 0.4	V	D3.17
Input low voltage	SATA_XTALI crystal mode Bypass mode	SV_{IL}	—	Vxtal – 0.4 V (V_{DD_IO}/2) – 0.4	V	D3.18
Input low voltage	USB_XTALI crystal mode Bypass mode	UV_{IL}	—	Vxtal – 0.4 (V_{DD_IO}/2) – 0.4	V	D3.19
Input low voltage	RTC_XTALI crystal mode Bypass mode	RV_{IL}	—	(VBAT_RTC/5) – 0.5 (VBAT_RTC/2) – 0.4	V	D3.20
Input leakage current	Vin = 0 or V_{DD_IO}/$V_{DD\_MEM\_IO\_DDR/2}$ (depending on input type)[5]	I_{IN}	–2.5	2.5	µA	D3.21
Input leakage current	SYS_XTALI Vin = 0 or V_{DD_IO}	I_{IN}	—	20	µA	D3.22

3.1.6.1 Heat Dissipation

An estimation of the chip-junction temperature, T_J, can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \text{Eqn. 3}$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
P_D = power dissipation in package (W)

The junction to ambient thermal resistance is an industry standard value, which provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board, and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is correct depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 4}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction to case thermal resistance (°C/W)
$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. You control the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, you can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for ceramic packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \text{Eqn. 5}$$

where:

T_T = thermocouple temperature on top of package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned, so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over approximately one mm of wire extending

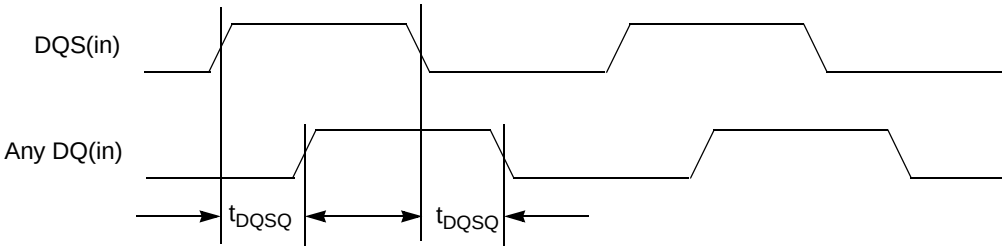

Figure 9. DDR Read Timing, DQ vs DQS

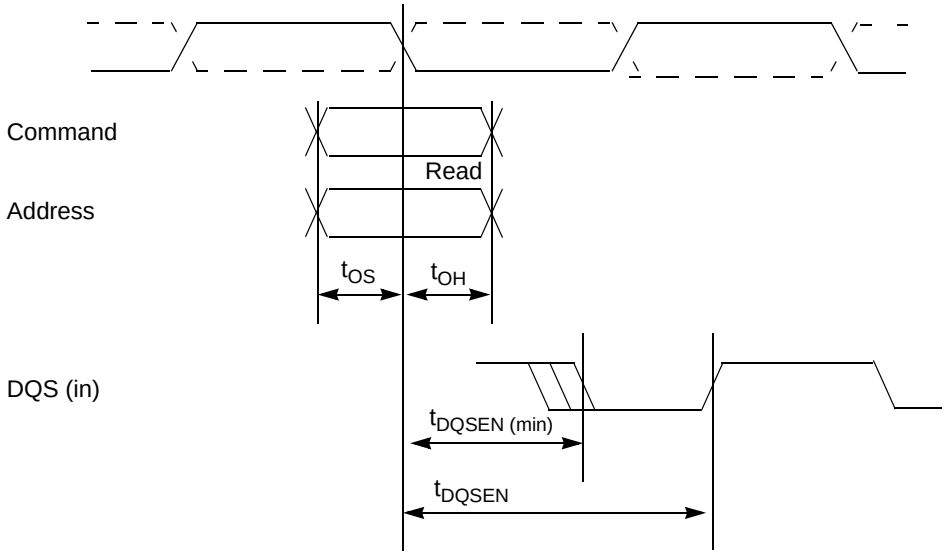

Figure 10. DDR Read Timing, DQSEN

Figure 11 provides the AC test load for the DDR bus.

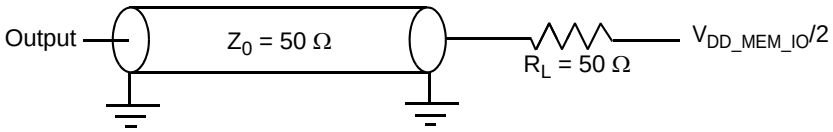

Figure 11. DDR AC Test Load

3.3.6 PCI

The PCI interface on the MPC5121e/MPC5123 is designed to PCI Version 2.3 and supports 33 and 66 MHz PCI operations. See the PCI Local Bus Specification; the component section specifies the electrical and timing parameters for PCI components with the intent that components connect directly together whether on the planar or an expansion board, without any external buffers or other glue logic. Parameters apply at the package pins, not at expansion board edge connectors.

The PCI_CLK is used as output clock, the MPC5121e/MPC5123 is a PCI host device only.

Figure 12 shows the clock waveform and required measurement points for 3.3 V signaling environments. Table 21 summarizes the clock specifications.

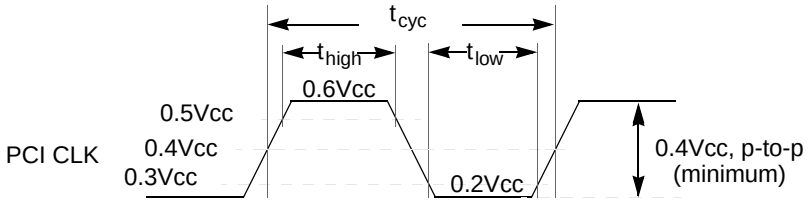

Figure 12. PCI CLK Waveform

Table 21. PCI CLK Specifications

Sym	Description	66 MHz[1]		33 MHz		Units	SpecID
		Min[2]	Max	Min	Max		
t_{cyc}	PCI CLK Cycle Time[1,3]	15	30	30	—	ns	A6.1
t_{high}	PCI CLK High Time	6	—	11	—	ns	A6.2
t_{low}	PCI CLK Low Time	6	—	11	—	ns	A6.3
—	PCI CLK Slew Rate[2]	1.5	4	1	4	V/ns	A6.4

1 In general, all 66 MHz PCI components must work with any clock frequency up to 66 MHz. CLK requirements vary depending upon whether the clock frequency is above 33 MHz.

2 Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in Figure 12.

3 The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.

Table 22. PCI Timing Parameters[1]

Sym	Description	66 MHz		33 MHz		Units	SpecID
		Min[2]	Max	Min	Max		
t_{val}	CLK to Signal Valid Delay – bused signals[1,2,3]	2	6	2	11	ns	A6.5
$t_{val}(ptp)$	CLK to Signal Valid Delay – point to point[1,2,3]	2	6	2	12	ns	A6.6
t_{on}	Float to Active Delay[1]	2	—	2	—	ns	A6.7
t_{off}	Active to Float Delay[1]		14		28	ns	A6.8
t_{su}	Input Setup Time to CLK – bused signals[3,4]	3	—	7	—	ns	A6.9
$t_{su}(ptp)$	Input Setup Time to CLK – point to point[3,4]	5	—	10,12	—	ns	A6.10
t_h	Input Hold Time from CLK[4]	0	—	0	—	ns	A6.11

1 See the timing measurement conditions in the PCI Local Bus Specification. It is important that all driven signal transitions drive to their Voh or Vol level within one Tcyc.

2 Minimum times are measured at the package pin with the load circuit, and maximum times are measured with the load circuit as shown in the PCI Local Bus Specification.

3 REQ# and GNT# are point-to-point signals and have different input setup times than do bused signals. GNT# and REQ# have a setup of 5 ns at 66 MHz. All other signals are bused.

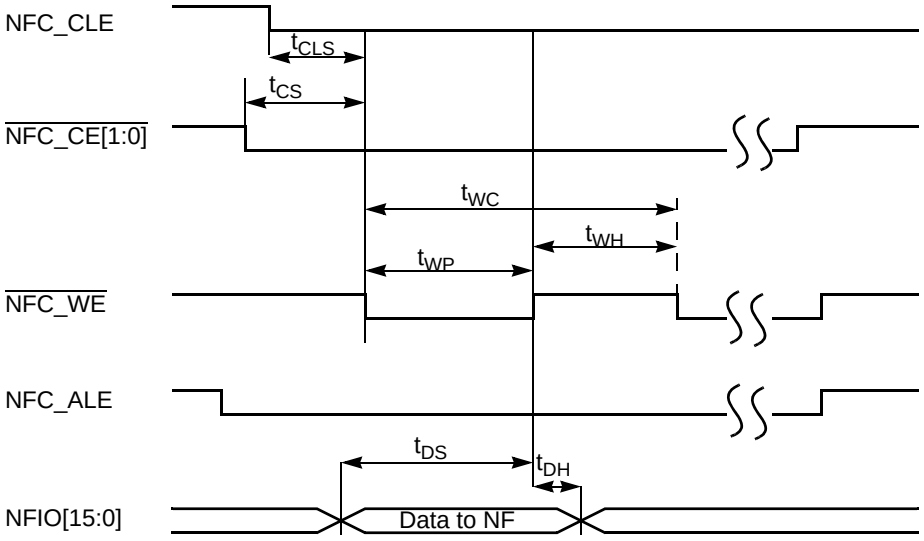

Figure 23. Write Data Latch Timing

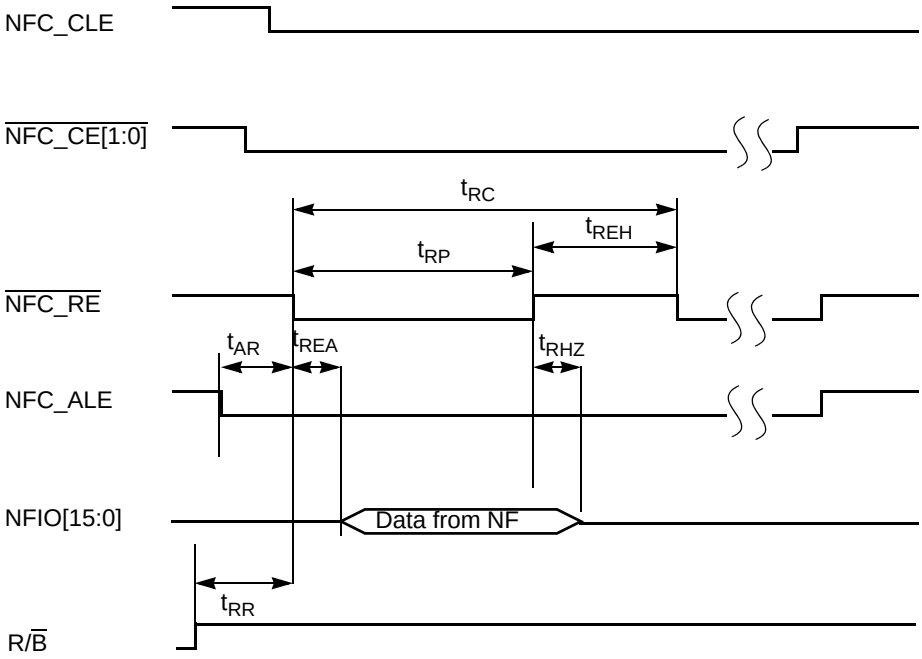

Figure 24. Read Data Latch Timing

Table 3-26. PATA Timing Parameters (continued)

Name	Meaning	Controlled by	Value	SpecID
t_{skew4}	Max difference in cable propagation delay between: ATA_IORDY and ATA_DATA (read)	Cable		A9.14
t_{skew5}	Max difference in cable propagation delay between: ATA_DIOR, ATA_DIOW, ATA_DMACK and ATA_CS0, ATA_CS1, ATA_DA2, ATA_DA1, ATA_DA0, ATA_DATA (write)	Cable		A9.15
tskew6	Max difference in cable propagation delay without accounting for ground bounce	Cable		A9.16

3.3.9.2 PIO Mode Timing

A timing diagram for the PIO read mode is given in Figure 26.

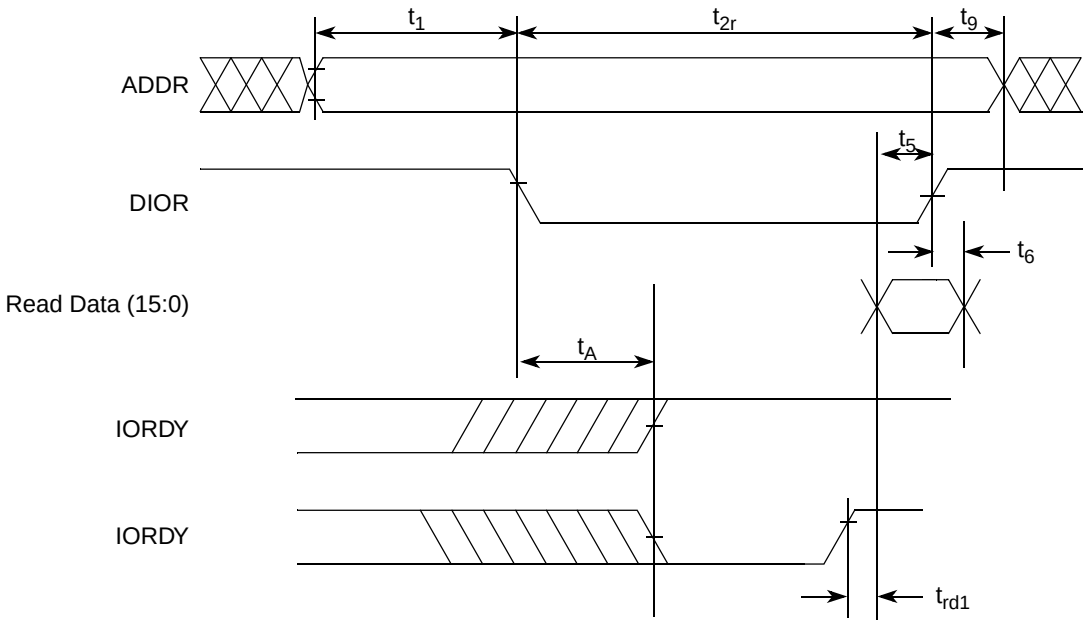

Figure 26. PIO Read Mode Timing

To fulfill read mode timing, the different timing parameters given in Table 3-27 must be observed.

Table 3-27. Timing Parameters PIO Read

ATA Parameter	PIO Read Mode Timing Parameter	Value	How to meet	SpecID
t_1	t_1	$t_1(min) = (time\_1 \times T) - (t_{skew1} + t_{skew2} + t_{skew5})$	calculate and programming time_1. [1]	A9.20
t_2	t_2r	$t_2(min) = (time\_2r \times T) - (t_{skew1} + t_{skew2} + t_{skew5})$	calculate and programming time_2r. [1]	A9.21
t_9	t_9	$t_9(min) = (time\_9 \times T) - (t_{skew1} + t_{skew2} + t_{skew6})$	calculate and programming time_9. [1]	A9.22

Table 30. Timing Parameters UDMA in Burst

ATA Parameter	UDMA In Timing Parameter	Value	How to Meet	SpecID
t_{ack}	t_{ack}	$t_{ack(min)} = (time\_ack \times T) - (t_{skew1} + t_{skew2})$	calculate and programming time_ack. [1]	A9.51
t_{env}	t_{env}	$t_{env(min)} = (time\_env \times T) - (t_{skew1} + t_{skew2})$ $t_{env(max)} = (time\_env \times T) + (t_{skew1} + t_{skew2})$	calculate and programming time_env. [1]	A9.52
t_{ds}	t_{ds1}	$t_{ds} - (t_{skew3}) - ti\_ds > 0$	t_{skew3}, ti_ds, ti_dh should be low enough	A9.53
t_{dh}	t_{dh1}	$t_{dh} - (t_{skew3}) - ti\_dh > 0$		A9.54
t_{cyc}	t_{c1}	$(t_{cyc} - t_{skew}) > T$	Bus clock period T big enough	A9.55
t_{rp}	t_{rp}	$t_{rp(min)} = time\_rp \times T - (t_{skew1} + t_{skew2} + t_{skew6})$	calculate and programming time_rp. [1]	A9.56
—	t_{x1} [2]	$(time\_rp \times T) - [tco + tsu + 3T + (2 \times t_{buf}) + (2 \times tcable2)] >$ trfs (drive)	calculate and programming time_rp. [1]	A9.57
t_{mli}	t_{mli1}	$t_{mli1(min)} = (time\_mlix + 0.4) \times T$	calculate and programming time_mlix. [1]	A9.58
t_{zah}	t_{zah}	$t_{zah(min)} = (time\_zah + 0.4) \times T$	calculate and programming time_zah. [1]	A9.59
t_{dzfs}	t_{dzfs}	$t_{dzfs} = (time\_dzfs \times T) - (t_{skew1} + t_{skew2})$	calculate and programming time_dzfs. [1]	A9.60
t_{cvh}	t_{cvh}	$t_{cvh} = (time\_cvh \times T) - (t_{skew1} + t_{skew2})$	calculate and programming time_cvh. [1]	A9.61
—	t_{on} t_{off} [3]	$t_{on} = (time\_on \times T) - t_{skew1}$ $t_{off} = (time\_off \times T) - t_{skew1}$	—	A9.62

1 See the *MPC5121e Microcontroller Reference Manual.*

2 A special timing requirement in the ATA host requires the internal DIOW to go only high three clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

3 Make t_{on} and t_{off} large enough to avoid bus contention.

3.3.9.5 UDMA Out Timing Diagrams

UDMA mode timing is more complicated than PIO mode or MDMA mode. In this section, timing diagrams for UDMA out are given:

- Figure 33 gives timing for UDMA out transfer start
- Figure 34 gives timing for host terminating UDMA out transfer
- Figure 35 gives timing for device terminating UDMA out transfer

Table 31. Timing Parameters UDMA Out Burst (continued)

ATA Parameter	UDMA Out Timing Parameter	Value	How to meet	SpecID
t_{li}	t_{li2}	$t_{li2} > 0$	—	A9.74
t_{li}	t_{li3}	$t_{li3} > 0$	—	A9.75
t_{cvh}	t_{cvh}	$t_{cvh} = (time\_cvh \times T) - (t_{skew1} + t_{skew2})$	calculate and program time_cvh. [1]	A9.76
—	t_{on} t_{off}	$t_{on} = time\_on \times T - t_{skew1}$ $t_{off} = time\_off \times T - t_{skew1}$	—	A9.77

1 See the *MPC5121e Microcontroller Reference Manual.*

3.3.10 SATA PHY

1.5 Gbps SATA PHY Layer

See “Serial ATA: High Speed Serialized AT Attachment” Revision 1.0a, 7-January-2003.

3.3.11 FEC

AC Test Timing Conditions:

- Output Loading
  All Outputs: 25 pF

Table 32. MII Rx Signal Timing

Symbol	Description	Min	Max	Unit	SpecID
1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns	A11.1
2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns	A11.2
3	RX_CLK pulse width high	35%	65%	RX_CLK Period[1]	A11.3
4	RX_CLK pulse width low	35%	65%	RX_CLK Period[1]	A11.4

1 RX_CLK shall have a frequency of 25% of data rate of the received signal. See the IEEE 802.3 Specification.

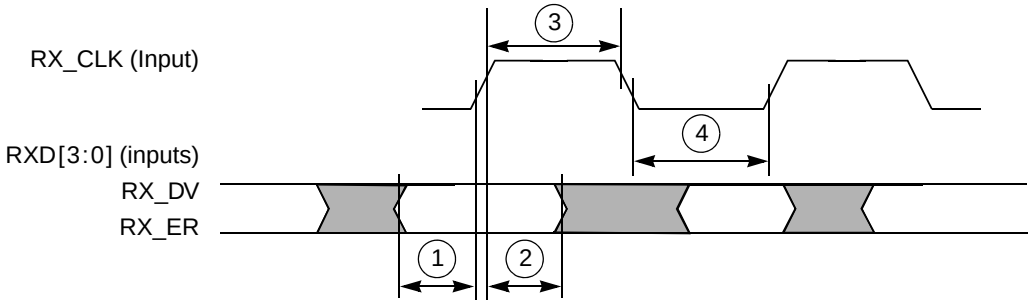

Figure 36. Ethernet Timing Diagram – MII Rx Signal

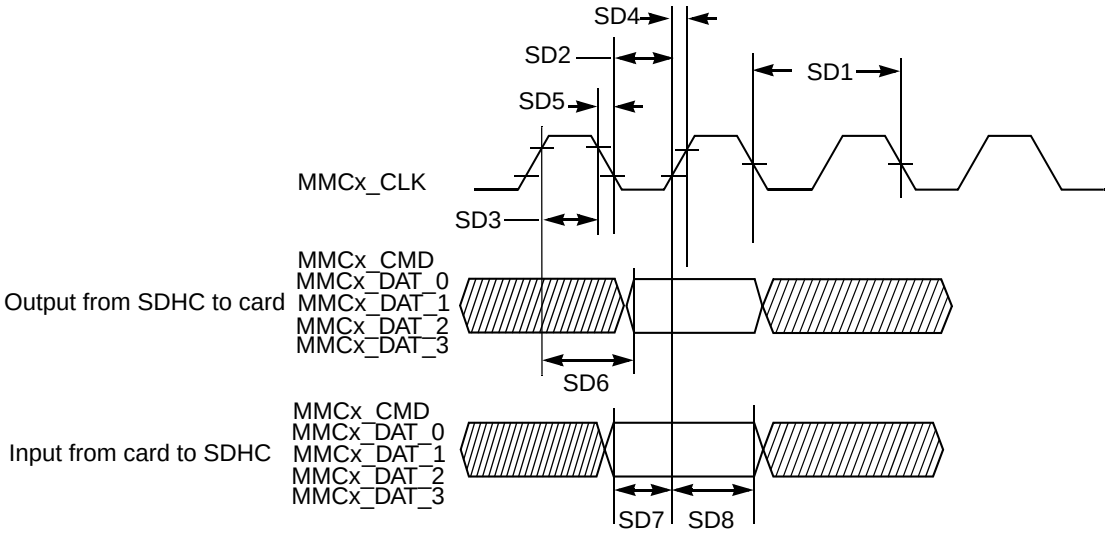

Figure 41. SDHC Timing Diagram

Table 37 lists the timing parameters.

Table 37. MMC/SD Interface Timing Parameters

ID	Parameter	Symbols	Min	Max	Unit	SpecID
Card Input Clock						
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz	A14.1
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz	A14.2
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz	A14.3
	Clock Frequency (Identification Mode)	f_{OD}[4]	100	400	kHz	A14.4
SD2	Clock Low Time (Full Speed/High Speed)	t_{WL}	10/7		ns	A14.5
SD3	Clock High Time (Full Speed/High Speed)	t_{WH}	10/7		ns	A14.6
SD4	Clock Rise Time (Full Speed/High Speed)	t_{TLH}		10/3	ns	A14.7
SD5	Clock Fall Time (Full Speed/High Speed)	t_{THL}		10/3	ns	A14.8
SDHC Output / Card Inputs CMD, DAT (Reference to CLK)						
SD6	SDHC Output Delay	t_{OD}	TH[5] – 3	TH+3	ns	A14.9
SDHC Input / Card Outputs CMD, DAT (Reference to CLK)						
SD7	SDHC Input Setup Time	t_{ISU}	2.5		ns	A14.10
SD8	SDHC Input Hold Time	t_{IH}	2.5		ns	A14.11

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal data transfer mode for SD/SDIO card, clock frequency can be any value between 0 ~ 25 MHz.

3 In normal data transfer mode for MMC card, clock frequency can be any value between 0 ~ 20 MHz.

4 In card identification mode, card clock must be 100 kHz ~ 400 kHz, voltage ranges from 2.7 to 3.6 V.

5 Suggested ClockPeriod = T, CLK_DIVIDER (in SDHC Clock Rate Register) = D, then TH = [(D + 1)/2]/(D + 1) × T where the value is rounded.

3.3.15 DIU

The DIU is a display controller designed to manage the TFT LCD display.

3.3.15.1 Interface to TFT LCD Panels, Functional Description

Figure 42 shows the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with positive polarity. The sequence of events for active matrix interface timing is:

- DIU_CLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, DIU_CLK runs continuously. This signal frequency could be from 5 to 100 MHz depending on the panel type.
- DIU_HSYNC causes the panel to start a new line. It always encompasses at least one DIU_CLK pulse.
- DIU_VSYNC causes the panel to start a new frame. It always encompasses at least one DIU_HSYNC pulse.
- DIU_DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

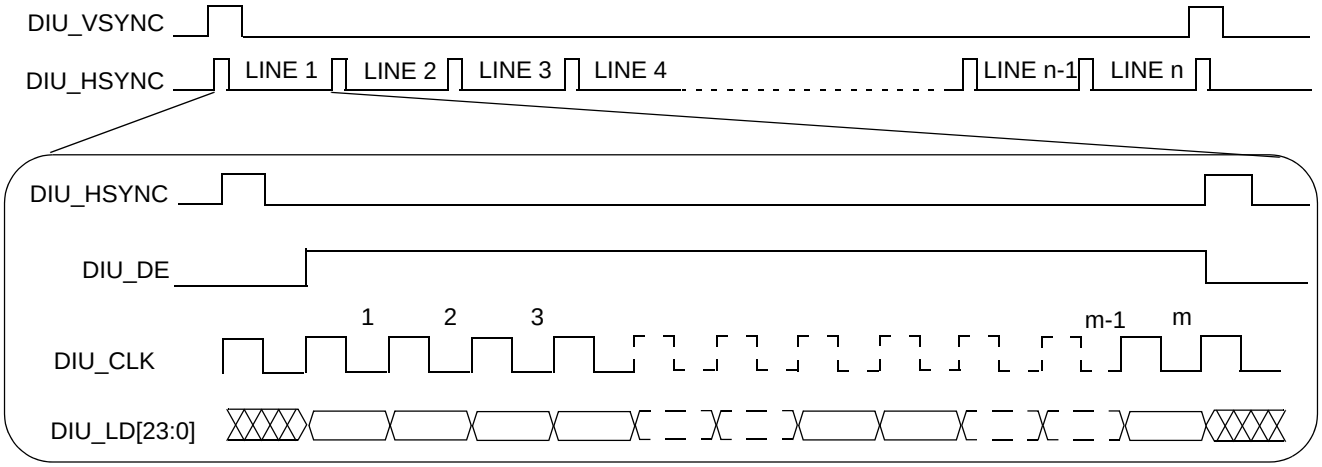

Figure 42. Interface Timing Diagram for TFT LCD Panels

3.3.15.2 Interface to TFT LCD Panels, Electrical Characteristics

Figure 43 shows the horizontal timing (timing of one line), including the horizontal sync pulse and the data. All parameters shown in the diagram are programmable. This timing diagram corresponds to positive polarity of the DIU_CLK signal (meaning the data and sync. signals change at the rising edge of it) and active-high polarity of the DIU_HSYNC, DIU_VSYNC and DIU_DE signal. You can select the polarity of the DIU_HSYNC and DIU_VSYNC signal via the SYN_POL register, whether active-high or active-low, the default is active-high. The DIU_DE signal is always active-high. And, pixel clock inversion and a flexible programmable pixel clock delay is also supported, programed via the DIU Clock Config Register (DCCR) in the system clock module.

Table 38. LCD Interface Timing Parameters – Pixel Level (continued)

Name	Description	Value	Unit	SpecID
t_{FPH}	HSYNC Front Porch Width	FP_H × t_{PCP}	ns	A15.4
t_{SW}	Screen Width	DELTA_X × t_{PCP}	ns	A15.5
t_{HSP}	HSYNC (Line) Period	(PW_H + BP_H + DELTA_X + FP_H) × t_{PCP}	ns	A15.6
t_{PWV}	VSYNC Pulse Width	PW_V × t_{HSP}	ns	A15.7
t_{BPV}	VSYNC Back Porch Width	BP_V × t_{HSP}	ns	A15.8
t_{FPV}	VSYNC Front Porch Width	FP_V × t_{HSP}	ns	A15.9
t_{SH}	Screen Height	DELTA_Y × t_{HSP}	ns	A15.10
t_{VSP}	VSYNC (Frame) Period	(PW_V + BP_V + DELTA_Y + FP_H) × t_{HSP}	ns	A15.11

1 Display interface pixel clock period immediate value (in nanosecond).

The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register; The PW_H, BP_H, and FP_H parameters are programmed via the HSYN_PARA register; And the PW_V, BP_V and FP_V parameters are programmed via the VSYN_PARA register. See appropriate section in the reference manual for detailed descriptions on these parameters.

Figure 45 shows the synchronous display interface timing for access level, and Table 39 lists the timing parameters.

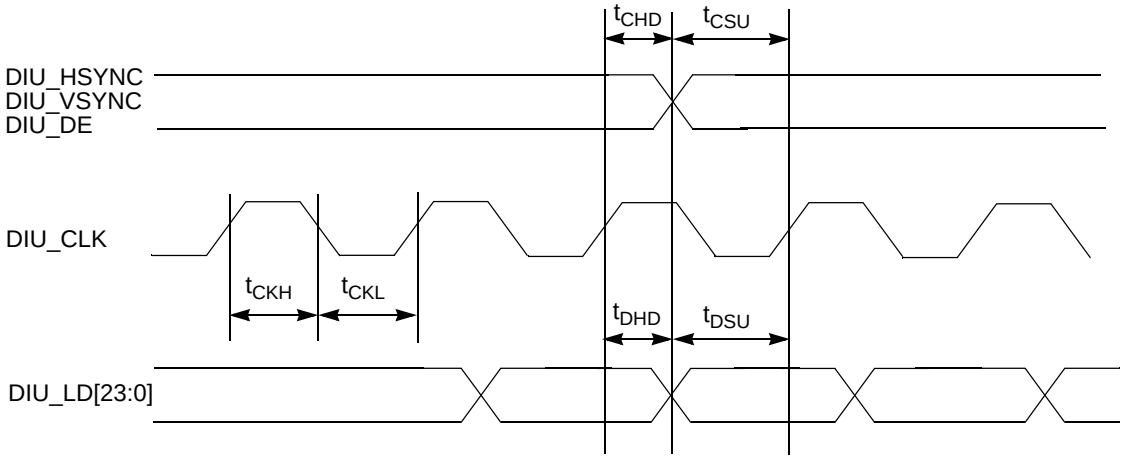

Figure 45. LCD Interface Timing Diagram – Access Level

Table 39. LCD Interface Timing Parameters – Access Level

Parameter	Description	Min	Typ	Max	Unit	SpecID
t_{CKH}	LCD Interface Pixel Clock High Time	t_{PCP} × 0.4	t_{PCP} × 0.5	t_{PCP} × 0.6	ns	A15.12
t_{CKL}	LCD Interface Pixel Clock Low Time	t_{PCP} × 0.4	t_{PCP} × 0.5	t_{PCP} × 0.6	ns	A15.13
t_{DSU}	LCD Interface Data Setup Time	5.0	—	—	ns	A15.14
t_{DHD}	LCD Interface Data Hold Time	6.0	—	—	ns	A15.15
t_{CSU}	LCD Interface Control Signal Setup Time	5.0	—	—	ns	A15.16
t_{CHD}	LCD Interface Control Signal Hold Time	6.0	—	—	ns	A15.17

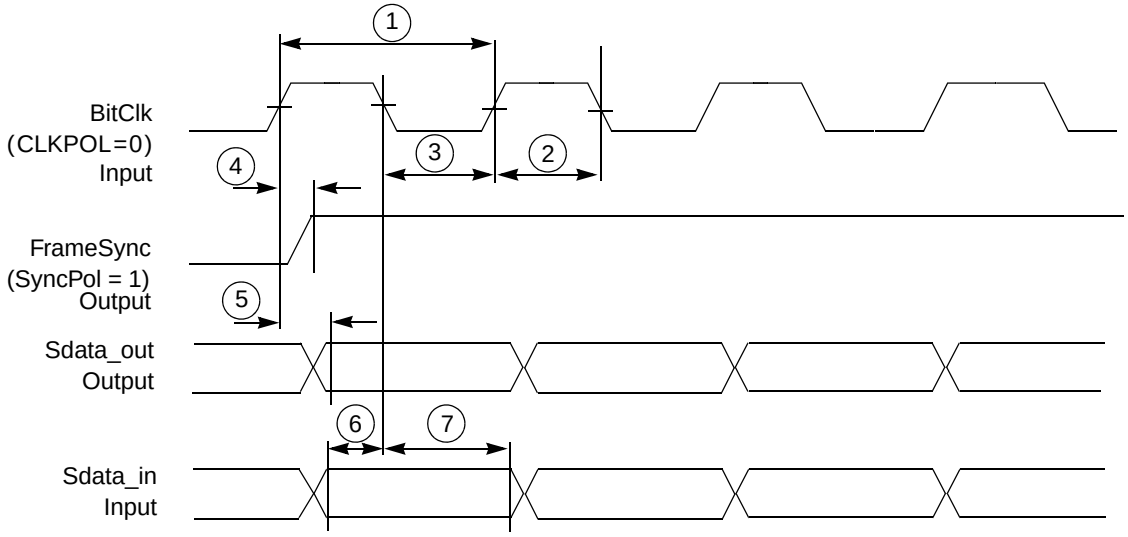

Figure 49. Timing Diagram – AC97 Mode

3.3.20.3 SPI Mode

Table 45. Timing Specifications – SPI Master Mode, Format 0 (CPHA = 0)

Symbol	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A20.26
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A20.27
3	Slave select clock delay, programable in the PSC CCS register	30.0	—	ns	A20.28
4	Output Data valid after Slave Select ($\overline{SS}$)	—	8.9	ns	A20.29
5	Output Data valid after SCK	—	8.9	ns	A20.30
6	Input Data setup time	6.0	—	ns	A20.31
7	Input Data hold time	1.0	—	ns	A20.32
8	Slave disable lag time	—	TSCK	ns	A20.33
9	Sequential Transfer delay, programmable in the PSC CTUR / CTLR register	15.0	—	ns	A20.34
10	Clock falling time	—	7.9	ns	A20.35
11	Clock rising time	—	7.9	ns	A20.36

NOTE

Output timing is specified at a nominal 50 pF load.

Table 53. COP/BDM Interface Signals

BDM Pin #	MPC5121e/MPC5123 I/O Pin	BDM Connector	Internal Pull Up/Down	External Pull Up/Down	I/O[1]
16	—	GND	—	—	—
15	$\overline{\text{CKSTP\_OUT}}$	ckstp_out	—	10 kΩ Pull-up	I
14	—	KEY	—	—	—
13	$\overline{\text{HRESET}}$	hreset	Pull-up	10 kΩ Pull-up	O
12	—	GND	—	—	—
11	$\overline{\text{SRESET}}$	sreset	Pull-up	10 kΩ Pull-up	O
10	—	N/C	—	—	—
9	TMS	tms	Pull-up	10 kΩ Pull-up	O
8	$\overline{\text{CKSTP\_IN}}$	ckstp_in	—	10 kΩ Pull-up	O
7	TCK	tck	Pull-up	10 kΩ Pull-up	O
6	—	VDD[2]	—	—	—
5	See Note[3]	halted[3]	—	—	I
4	$\overline{\text{TRST}}$	trst	Pull-up	10 kΩ Pull-up	O
3	TDI	tdi	Pull-up	10 kΩ Pull-up	O
2	See Note[4]	qack[4]	—	—	O
1	TDO	tdo	—	—	I

1 With respect to the emulator tool's perspective:
Input is really an output from the embedded e300 core.
Output is really an input to the core.

2 From the board under test, power sense for chip power.

3 HALTED is not available from e300 core.

4 Input to the e300 core to enable/disable soft-stop condition during breakpoints. MPC5121e/MPC5123 internally ties CORE_QACK to GND in its normal/functional mode (always asserted).

For a board with a COP (common on-chip processor) connector that accesses the JTAG interface and needs to reset the JTAG module, only wiring $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ is not recommended.

To reset the MPC5121e/MPC5123 via the COP connector, the $\overline{\text{HRESET}}$ pin of the COP should be connected to the $\overline{\text{HRESET}}$ pin of the MPC5121e/MPC5123. The circuitry shown in Figure 63 allows the COP to assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ separately, while any other board sources can drive $\overline{\text{PORESET}}$.

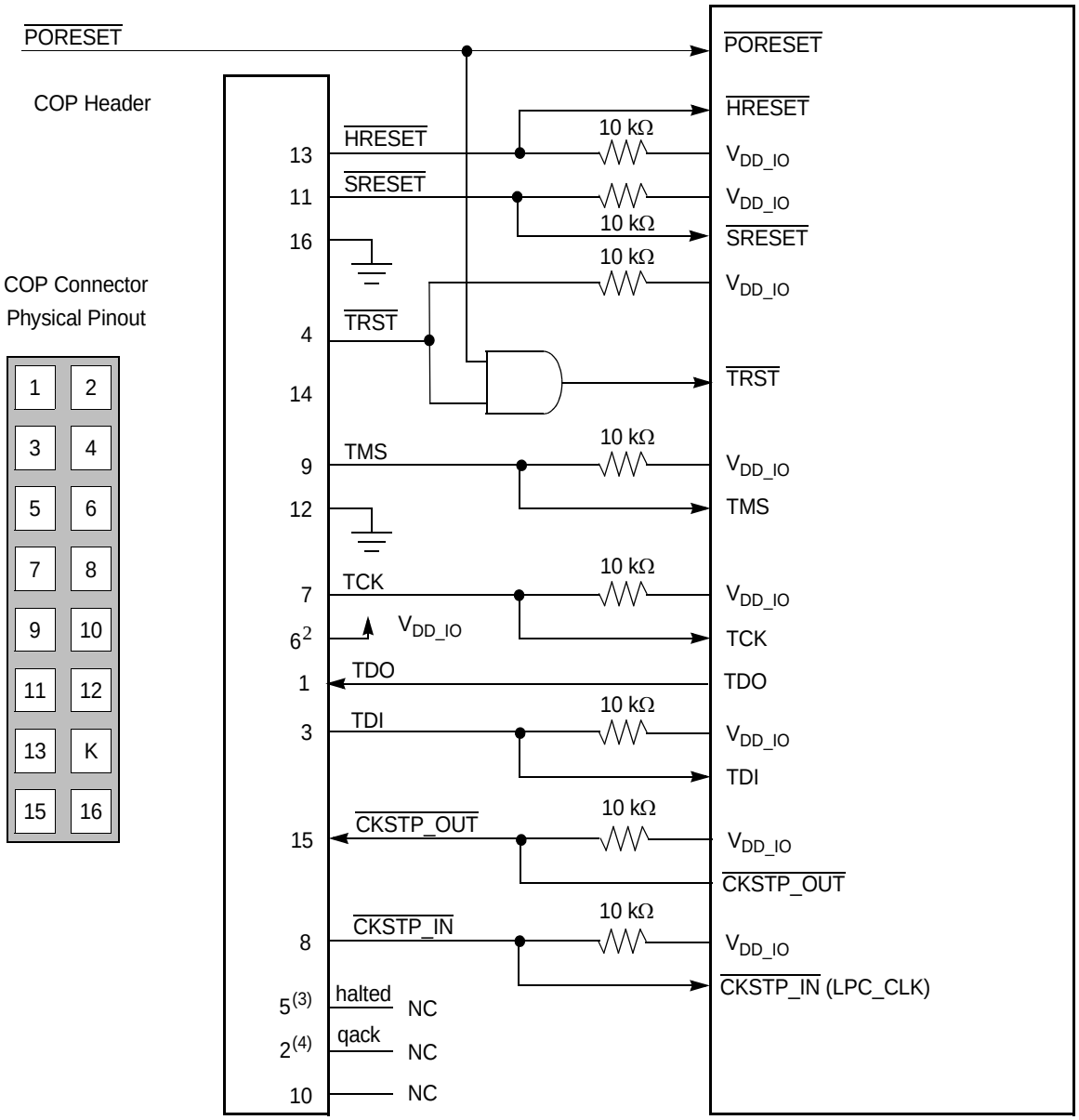

Figure 63. COP Connector Diagram

4.5.2.2 Boards Without COP Connector

If the JTAG interface is not used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{PORESET}}$, so that it is asserted when the system reset signal ($\overline{\text{PORESET}}$) is asserted. This ensures that the JTAG scan chain is initialized during power on. Figure 64 shows the connection of the JTAG interface without COP connector.

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