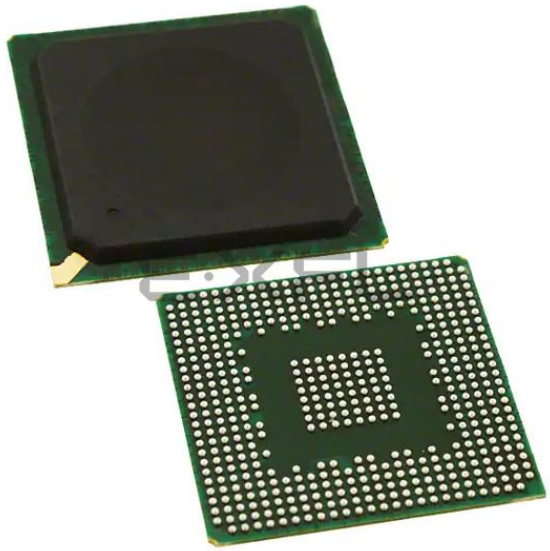

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Details	
Product Status	Active
Core Processor	e300
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Connectivity	CANbus, EBI/EMI, Ethernet, I²C, USB OTG
Peripherals	DMA, WDT
Number of I/O	147
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5121yvy400b

Table of Contents

2.2 Pinout Listings

Table 3 provides the pin-out listing for the MPC5121e/MPC5123.

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 1 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
DDR Memory Interface (67 Total)				
MDQ0	AF5	DDR	$V_{DD\_MEM\_IO}$	—
MDQ1	AB6	DDR	$V_{DD\_MEM\_IO}$	—
MDQ2	AE4	DDR	$V_{DD\_MEM\_IO}$	—
MDQ3	AF6	DDR	$V_{DD\_MEM\_IO}$	—
MDQ4	AF7	DDR	$V_{DD\_MEM\_IO}$	—
MDQ5	AB8	DDR	$V_{DD\_MEM\_IO}$	—
MDQ6	AD6	DDR	$V_{DD\_MEM\_IO}$	—
MDQ7	AE6	DDR	$V_{DD\_MEM\_IO}$	—
MDQ8	AC7	DDR	$V_{DD\_MEM\_IO}$	—
MDQ9	AF8	DDR	$V_{DD\_MEM\_IO}$	—
MDQ10	AB9	DDR	$V_{DD\_MEM\_IO}$	—
MDQ11	AD7	DDR	$V_{DD\_MEM\_IO}$	—
MDQ12	AE9	DDR	$V_{DD\_MEM\_IO}$	—
MDQ13	AF10	DDR	$V_{DD\_MEM\_IO}$	—
MDQ14	AC9	DDR	$V_{DD\_MEM\_IO}$	—
MDQ15	AF11	DDR	$V_{DD\_MEM\_IO}$	—
MDQ16	AD10	DDR	$V_{DD\_MEM\_IO}$	—
MDQ17	AF12	DDR	$V_{DD\_MEM\_IO}$	—
MDQ18	AD11	DDR	$V_{DD\_MEM\_IO}$	—
MDQ19	AB12	DDR	$V_{DD\_MEM\_IO}$	—
MDQ20	AD12	DDR	$V_{DD\_MEM\_IO}$	—
MDQ21	AB13	DDR	$V_{DD\_MEM\_IO}$	—
MDQ22	AF14	DDR	$V_{DD\_MEM\_IO}$	—
MDQ23	AD13	DDR	$V_{DD\_MEM\_IO}$	—
MDQ24	AE13	DDR	$V_{DD\_MEM\_IO}$	—
MDQ25	AC13	DDR	$V_{DD\_MEM\_IO}$	—
MDQ26	AF15	DDR	$V_{DD\_MEM\_IO}$	—
MDQ27	AB14	DDR	$V_{DD\_MEM\_IO}$	—
MDQ28	AE16	DDR	$V_{DD\_MEM\_IO}$	—
MDQ29	AD15	DDR	$V_{DD\_MEM\_IO}$	—
MDQ30	AC15	DDR	$V_{DD\_MEM\_IO}$	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 8 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
PSC5_3	AD2	General IO	V_{DD_IO}	—
PSC5_4	AE3	General IO	V_{DD_IO}	—
PSC6_0	A11	General IO	V_{DD_IO}	—
PSC6_1	C10	General IO	V_{DD_IO}	—
PSC6_2	A10	General IO	V_{DD_IO}	—
PSC6_3	B9	General IO	V_{DD_IO}	—
PSC6_4	A9	General IO	V_{DD_IO}	—
PSC7_0	B8	General IO	V_{DD_IO}	—
PSC7_1	E10	General IO	V_{DD_IO}	—
PSC7_2	C8	General IO	V_{DD_IO}	—
PSC7_3	A8	General IO	V_{DD_IO}	—
PSC7_4	A7	General IO	V_{DD_IO}	—
PSC8_0	E9	General IO	V_{DD_IO}	—
PSC8_1	D8	General IO	V_{DD_IO}	—
PSC8_2	C7	General IO	V_{DD_IO}	—
PSC8_3	B6	General IO	V_{DD_IO}	—
PSC8_4	E8	General IO	V_{DD_IO}	—
PSC9_0	C6	General IO	V_{DD_IO}	—
PSC9_1	D7	General IO	V_{DD_IO}	—
PSC9_2	E7	General IO	V_{DD_IO}	—
PSC9_3	D6	General IO	V_{DD_IO}	—
PSC9_4	E6	General IO	V_{DD_IO}	—
PSC10_0	C13	General IO	V_{DD_IO}	—
PSC10_1	B13	General IO	V_{DD_IO}	—
PSC10_2	A13	General IO	V_{DD_IO}	—
PSC10_3	C12	General IO	V_{DD_IO}	—
PSC10_4	E12	General IO	V_{DD_IO}	—
PSC11_0	A12	General IO	V_{DD_IO}	—
PSC11_1	B11	General IO	V_{DD_IO}	—
PSC11_2	C11	General IO	V_{DD_IO}	—
PSC11_3	E11	General IO	V_{DD_IO}	—
PSC11_4	D11	General IO	V_{DD_IO}	—
JTAG (5 Total)				
TCK	AB26	General IO	V_{DD_IO}	2

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 12 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
USB_VDDA_BIAS	D22	Analog Power	—	—
USB_VSSA	C22, E20, E21	Analog Ground	—	—
USB_VDDA	C21, D20	Analog Power	—	—
Power and Ground Supplies (SATA PHY)				
SATA_RESREF	E4	Analog Power	—	—
SATA_VDDA_3P3	D4	Analog Power	—	—
SATA_VDDA_1P2	C5, D1, E2	Analog Power	—	—
SATA_VDDA_VREG	D5	Analog Power	—	—
SATA_PLL_VDDA1P2	E3	Analog Power	—	—
SATA_PLL_VSSA	D3	Analog Ground	—	—
SATA_RX_VSSA	A6, B4	Analog Ground	—	—
SATA_TX_VSSA	G1	Analog Ground	—	—

1 This pins should have an external pull-up resistor. Follow PCI specification and see System Design Information.

2 This pin contains an enabled internal Schmitt trigger.

3 These JTAG pins have internal pull-up P-FETs. This pin can not be configured.

4 This pin is an input only. This pin can not be configured.

5 This test pin must be tied to V_{SS}.

6 This pin is an input or open-drain output. This pin can not be configured. There is an internal pull-up resistor implemented.

NOTE

This table indicates only the pins with permananently enabled internal pull-up, pull-down, or Schmitt trigger. Most of the digital I/O pins can be configured to enable internal pull-up, pull-down, or Schmitt trigger. See the *MPC5121e Microcontroller Reference Manual*, IO Control chapter.

3.1.2 Recommended Operating Conditions

Table 5 gives the recommended operating conditions.

Table 5. Recommended Operating Conditions

Characteristic	Symbol	Min[1]	Typ	Max[1]	Unit	SpecID
Supply voltage – e300 core and peripheral logic	V_{DD_CORE}	1.33	1.4	1.47	V	D2.1
State Retention voltage – e300 core and peripheral logic [2]		1.08	—	—	V	D2.2
Supply voltage – standard I/O buffers	V_{DD_IO}	3.0	3.3	3.6	V	D2.3
Supply voltage – memory I/O buffers (DDR)	$V_{DD\_MEM\_IO\_DDR}$	2.3	2.5	2.7	V	D2.4
Supply voltage – memory I/O buffers (DDR2, LPDDR)	$V_{DD\_MEM\_IO\_DDR2}$ $V_{DD\_MEM\_IO\_LPDDR}$	1.7	1.8	1.9	V	D2.5
Input Reference Voltage (DDR/DDR2)	MVREF	0.49 × $V_{DD\_MEM\_IO}$	0.50 × $V_{DD\_MEM\_IO}$	0.51 × $V_{DD\_MEM\_IO}$	V	D2.6
Termination Voltage (DDR2)	MVTT	MVREF – 0.04	MVREF	MVREF + 0.04	V	D2.7
Supply voltage – System APLL, System Oscillator	SYS_PLL_AVDD	3.0	3.3	3.6	V	D2.8
Supply voltage – e300 APLL	CORE_PLL_AVDD	3.0	3.3	3.6	V	D2.9
Supply voltage – RTC (Hibernation)[3]	VBAT_RTC	3.0	3.3	3.6	V	D2.10
Supply voltage – FUSE Programming	AVDD_FUSEWR	3.3		3.6	V	D2.11
Supply voltage – SATA PHY analog and OSC	SATA_VDDA_3P3	3.0	3.3	3.6	V	D2.13
Supply voltage – SATA PHY voltage regulator	SATA_VDDA_VREG	1.7		2.6	V	D2.14
Supply voltage – SATA PHY Tx/Rx	SATA_VDDA_1P2	1.14	1.2	1.47	V	D2.15
Supply voltage – SATA PHY PLL	SATA_PLL_VDDA1P2	1.33	1.4	1.47	V	D2.16
Supply voltage – USB PHY PLL and OSC	USB_PLL_PWR3	3.0	3.3	3.6	V	D2.17
Supply voltage – USB PHY transceiver	USB_VDDA	3.0	3.3	3.6	V	D2.18
Supply voltage – USB PHY bandgap bias	USB_VDDA_BIAS	3.0	3.3	3.6	V	D2.19
Input voltage – USB PHY cable	USB_VBUS	1.4	—	3.6	V	D2.20
Input voltage – standard I/O buffers	Vin	0	—	V_{DD_IO}	V	D2.21
Input voltage – memory I/O buffers (DDR)	Vin_{DDR}	0	—	$V_{DD\_MEM\_IO\_DDR}$	V	D2.22
Input voltage – memory I/O buffers (DDR2)	Vin_{DDR2}	0	—	$V_{DD\_MEM\_IO\_DDR2}$	V	D2.23
Input voltage – memory I/O buffers (LPDDR)	Vin_{LPDDR}	0	—	$V_{DD\_MEM\_IO\_LPDR}$	V	D2.24
Ambient operating temperature range	TA	–40	—	+85	°C	D2.25
Junction operating temperature range	TJ	–40	—	+125	°C	D2.26

1 These are recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

2 The State Retention voltage can be applied to V_{DD_CORE} after the device is placed in Deep-Sleep mode.

3 VBAT_RTC should not be supplied by a battery of voltage less than 3.0 V.

Table 6. DC Electrical Specifications (continued)

Characteristic	Condition	Symbol	Min	Max	Unit	SpecID
Input leakage current	RTC_XTALI Vin = 0 or V_{DD_IO}	I_{IN}	—	1.0	µA	D3.23
Input current, pullup resistor[6]	Pullup V_{DD_IO} Vin = VIL	I_{INpu}	25	150	µA	D3.24
Input current, pulldown resistor [8]	Pulldown V_{DD_IO} Vin = VIH	I_{INpd}	25	150	µA	D3.25
Output high voltage	IOH is driver dependent[7] V_{DD_IO}	V_{OH}	0.8 × V_{DD_IO}	—	V	D3.26
Output high voltage	IOH is driver dependent[7] $V_{DD\_MEM\_IO\_DDR}$	V_{OHDDR}	1.90	—	V	D3.27
Output high voltage	IOH is driver dependent[7] $V_{DD\_MEM\_IO\_DDR2}$	V_{OHDDR2}	1.396	—	V	D3.28
Output high voltage	IOH is driver dependent[7] $V_{DD\_MEM\_IO\_LPDDR}$	$V_{OHLPDDR}$	$V_{DD\_MEM\_IO}$ – 0.28	—	V	D3.28
Output low voltage	IOL is driver dependent[7] V_{DD_IO}	V_{OL}	—	0.2 × V_{DD_IO}	V	D3.30
Output low voltage	IOL is driver dependent[7] $V_{DD\_MEM\_IO\_DDR}$	V_{OLDDR}	—	0.36	V	D3.31
Output low voltage	IOL is driver dependent[7] $V_{DD\_MEM\_IO\_DDR2}$	V_{OLDDR2}	—	0.28	V	D3.32
Output low voltage	IOL is driver dependent[7] $V_{DD\_MEM\_IO\_LPDDR}$	$V_{OLLPDDR}$	—	0.28	V	D3.33
Differential cross point voltage (DDR MCK/$\overline{\text{MCK}}$)	—	V_{OXMCK}	0.5 × $V_{DD\_MEM\_IO}$ – 0.125	0.5 × $V_{DD\_MEM\_IO}$ + 0.125	V	D3.34
DC Injection Current Per Pin[8]	—	I_{CS}	–1.0	1.0	mA	D3.35
Input Capacitance (digital pins)	—	C_{in}	—	7	pF	D3.36
Input Capacitance (analog pins)	—	C_{in}	—	10	pF	D3.37
On Die Termination (DDR2)	—	R_{ODT}	120	180	Ω	D3.38

1 This parameter is meant for those who do not use quartz crystals or resonators, but CAN osc, in crystal mode. In that case, Vextal – Vxtal - 400mV criteria has to be met for oscillator's comparator to produce output clock.

2 This parameter is meant for those who do not use quartz crystals or resonators, but signal generator clock to drive, in bypass mode. In that case, drive only the EXTAL pin not connecting anything to other pin for the oscillator's comparator to produce output clock.

3 This parameter is meant for those who do not use quartz crystals or resonators, but CAN osc, in crystal mode. In that case, drive one of the XTAL_IN or XTAL_OUT pins not connecting anything to other pin for the oscillator's comparator to produce output clock.

4 This parameter is meant for those who do not use quartz crystals or resonators, but signal generator clock to drive, in bypass mode. In that case, drive only the xtal_in pin not connecting anything to other pin for the oscillator's comparator to produce output clock.

5 Leakage current is measured with output drivers disabled and pull-up/pull-downs inactive.

6 Pullup current is measured at VIL and pulldown current is measured at VIH.

4 Fall time is measured from 20% of vdd to 80% of V_{DD}.
5 SYS_XTALI duty cycle is measured at V_M.

3.2.2 RTC Oscillator Electrical Characteristics

Table 13. RTC Oscillator Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit	SpecID
RTC_XTALI frequency	f_{rtc_xtal}	—	32.768	—	kHz	O2.1

3.2.3 System PLL Electrical Characteristics

Table 14. System PLL Specifications

Characteristic	Symbol	Min	Typical	Max	Unit	SpecID
Sys PLL input clock frequency[1]	f_{sys_xtal}	16	33.3	67	MHz	O3.1
Sys PLL input clock jitter[2]	t_{jitter}	—	—	10	ps	O3.2
Sys PLL VCO frequency[1]	f_{VCOsys}	400	—	800	MHz	O3.3
Sys PLL VCO output jitter (Dj), peak to peak / cycle	$f_{VCOjitterDj}$	—	—	40	ps	O3.4
Sys PLL VCO output jitter (Rj), RMS 1 sigma	$f_{VCOjitterRj}$	—	—	12	ps	O3.5
Sys PLL relock time—after power up[3]	t_{lock1}	—	—	200	µs	O3.6
Sys PLL relock time—when power was on[4]	t_{lock2}	—	—	170	µs	O3.7

1 The SYS_XTALI frequency and PLL Configuration bits must be chosen such that the resulting system frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
2 This represents total input jitter—short term and long term combined. Two different types of jitter can exist on the input to CORE_SYSCLK, systemic and true random jitter. True random jitter is rejected. Systemic jitter is passed into and through the PLL to the internal clock circuitry.
3 PLL relock time is the maximum amount of time required for the PLL lock after a stable VDD and CORE_SYSCLK are reached during the power-on reset sequence.
4 PLL relock time is the maximum amount of time required for the PLL lock after the PLL has been disabled and subsequently re-enabled during sleep modes.

3.2.4 e300 Core PLL Electrical Characteristics

The internal clocking of the e300 core is generated from and synchronized to the system clock by means of a voltage-controlled core PLL.

Table 15. e300 PLL Specifications

Characteristic	Symbol	Min	Typical	Max	Unit	SpecID
e300 frequency[1]	f_{core}	200	—	400	MHz	O4.1
e300 PLL VCO frequency[1]	$f_{VCOcore}$	400	—	800	MHz	O4.3
e300 PLL input clock frequency	f_{CSB_CLK}	50	—	200	MHz	O4.4
e300 PLL input clock cycle time	t_{CSB_CLK}	5	—	20	ns	O4.5
e300 PLL relock time[2]	t_{lock}	—	—	200	µs	O4.6

1 The frequency and e300 PLL Configuration bits must be chosen such that the resulting system frequencies, CPU (core) frequency, and e300 PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies in Table 16. There is a hard coded relationship between f_{core} and $f_{VCOcore}$ ($f_{core} = f_{VCOcore}/2$).

2 PLL relock time is the maximum amount of time required for the PLL lock after a stable VDD and CORE_SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

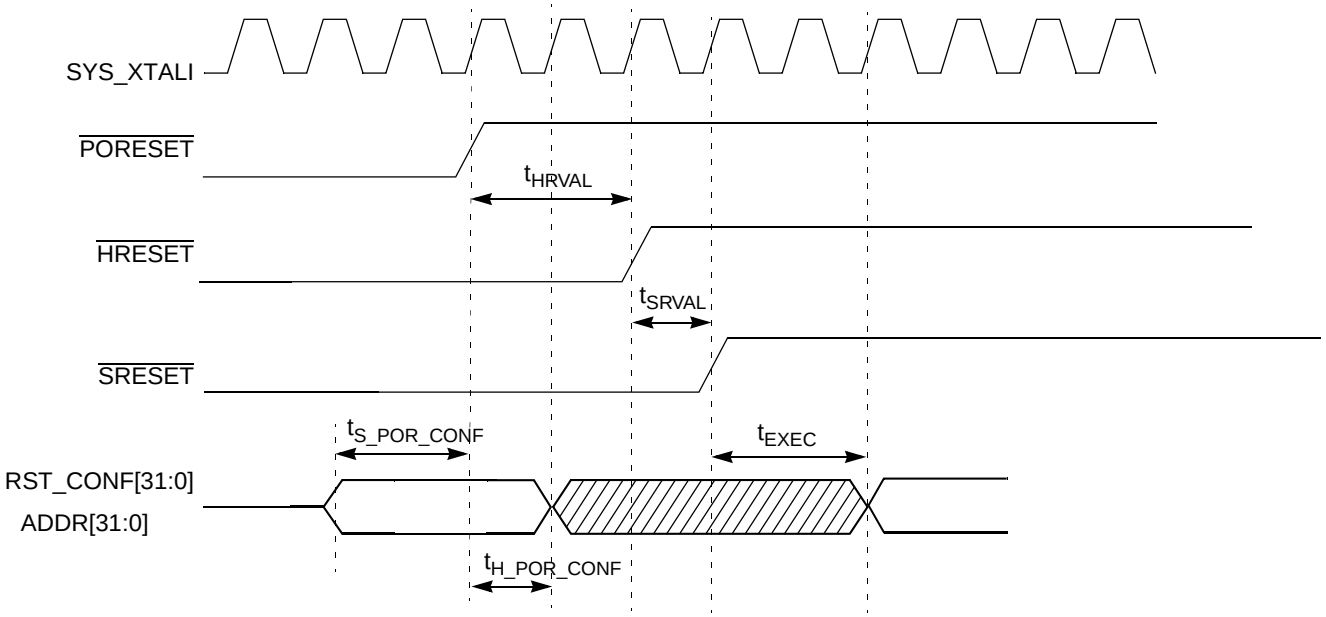

Figure 4. Power-Up Behavior

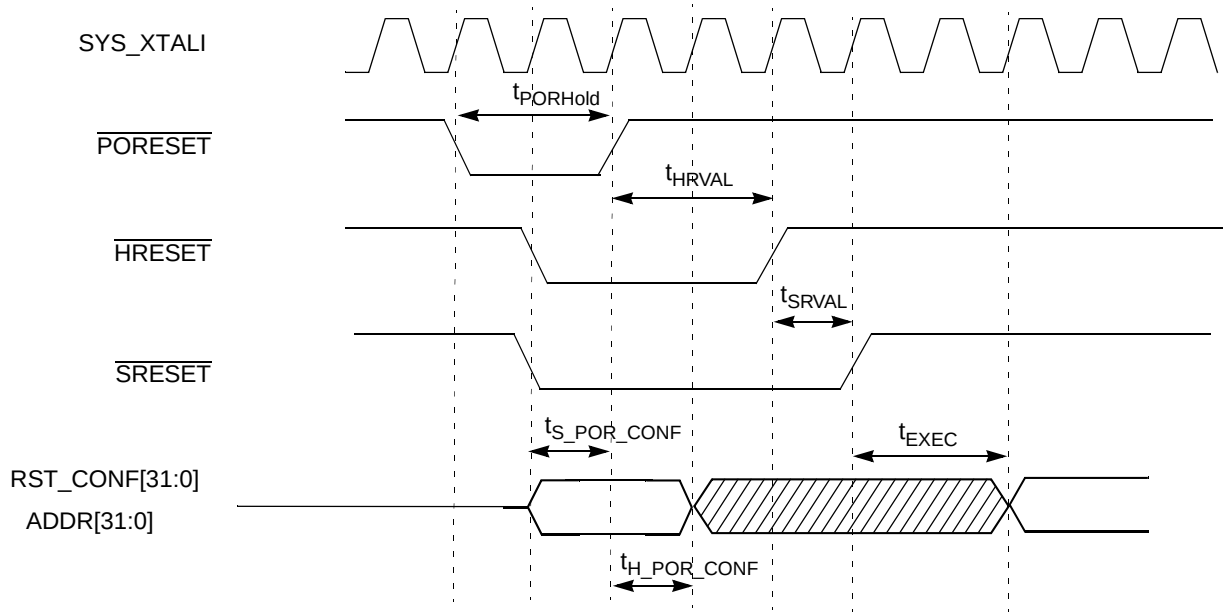

Figure 5. Power-On Reset Behavior

3.3.5.1 DDR and DDR2 SDRAM AC Timing Specifications

Table 20. DDR and DDR2 (DDR2-400) SDRAM Timing Specifications

At recommended operating conditions with $V_{DD\_MEM\_IO}$ of ±5%

Parameter	Symbol	Min	Max	Unit	Notes	SpecID
Clock cycle time, CL=x	t_{CK}	5000	—	ps		A5.1
CK HIGH pulse width	t_{CH}	0.47	0.53	t_{CK}	1,2	A5.3
CK LOW pulse width	t_{CL}	0.47	0.53	t_{CK}	1,2	A5.4
Skew between MCK and DQS transitions	t_{DQSS}	–0.25	0.25	t_{CK}	2, 3	A5.5
Address and control output setup time relative to MCK rising edge	$t_{OS(base)}$	(t_{CK}/2 – 750)	—	ps	2, 3	A5.6
Address and control output hold time relative to MCK rising edge	$t_{OH(base)}$	(t_{CK}/2 – 750)	—	ps	2, 3	A5.7
DQ and DM output setup time relative to DQS	$t_{DS1(base)}$	(t_{CK}/4 – 500)	—	ps	2, 3	A5.8
DQ and DM output hold time relative to DQS	$t_{DH1(base)}$	(t_{CK}/4 – 500)	—	ps	2, 3	A5.9
DQS-DQ skew for DQS and associated DQ inputs	t_{DQSQ}	–(t_{CK}/4 – 600)	(t_{CK}/4 – 600)	ps	2	A5.10
DQS window start position related to CAS read command	t_{DQSEN}	TBD	TBD	ps	1,2,3,4,5	A5.11

1 Measured with clock pin loaded with differential 100 termination resistor.

2 All transitions measured at mid-supply (VDD_MEM_IO/2).

3 Measured with all outputs except the clock loaded with 50 Ω termination resistor to $V_{DD\_MEM\_IO}$/2.

4 In this window, the first rising edge of DQS should occur. From the start of the window to DQS rising edge, DQS should be low.

5 Window position is given for t_{DQSEN} = 2.0 t_{CK}. For other values of t_{DQSEN}, window position is shifted accordingly.

Figure 8 shows the DDR SDRAM write timing.

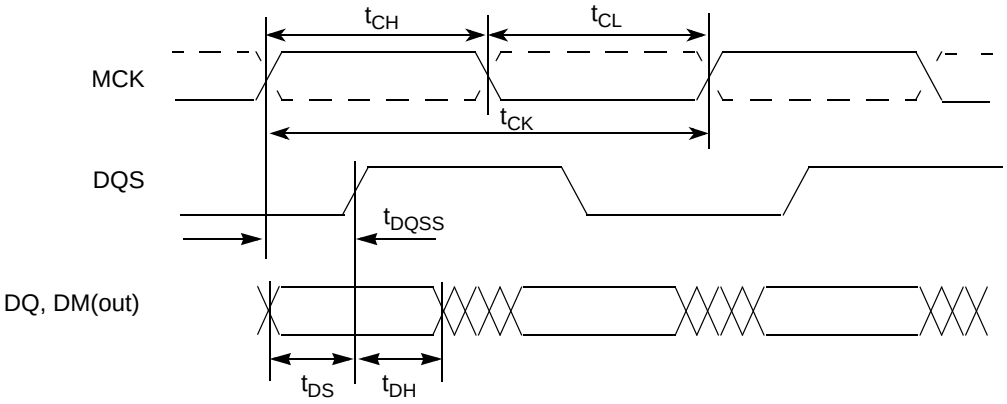

Figure 8. DDR Write Timing

Figure 9 and Figure 10 shows the DDR SDRAM read timing.

Table 25. NFC Timing Characteristics in Symmetric mode(SYM=1)[1]

Timing Parameter	Description	Min. value	Max. value	Unit	SpecID
t_{CLS}	NFC_CLE Setup time	T	—	ns	A8.21
t_{CLH}	NFC_CLE Hold time	T	—	ns	A8.22
t_{CS}	NFC_CE[1:0] Setup time	T-2	—	ns	A8.23
t_{CH}	NFC_CE[1:0] Hold time	1.5T-1	—	ns	A8.24
t_{WP}	NFC_WE Pulse width	0.5T+1	—	ns	A8.25
t_{ALS}	NFC_ALE Setup time	T	—	ns	A8.26
t_{ALH}	NFC_ALE Hold time	T	—	ns	A8.27
t_{DS}	Data Setup time	0.5T-3	—	ns	A8.28
t_{DH}	Data Hold time	0.5T	—	ns	A8.29
t_{WC}	Write Cycle time	T	—	ns	A8.30
t_{WH}	NFC_WE Hold time	0.5T-1	—	ns	A8.31
t_{RR}	Ready to NFC_RE low	5T+2	—	ns	A8.32
t_{RP}	NFC_RE pulse width	0.5T	—	ns	A8.33
t_{RC}	Read Cycle time	T	—	ns	A8.34
t_{REH}	NFC_RE High hold time	0.5T	—	ns	A8.35
t_{SS}	NFC Read Data setup time	9.6	—	ns	A8.36

1 T is the flash clock cycle.
T = 45 ns, frequency = 22 MHz (boot configuration, IP bus = 66 MHz)
T = 36 ns, frequency = 27 MHz (maximum configurable frequency, IP bus = 83 MHz)

3.3.9 PATA

The MPC5121e/MPC5123 ATA Controller (PATA) is completely software programmable. It can be programmed to operate with ATA protocols using their respective timing, as described in the ANSI ATA-4 specification. The ATA interface is completely asynchronous in nature. Signal relationships are based on specific fixed timing in terms of timing units (nanoseconds).

ATA data setup and hold times, with respect to Read/Write strobes, are software programmable inside the ATA Controller. Data setup and hold times are implemented using counters. The counters count the number of ATA clock cycles needed to meet the ANSI ATA-4 timing specifications. For details, see the ANSI ATA-4 specification and how to program an ATA Controller and ATA drive for different ATA protocols and their respective timing. See the *MPC5121e Microcontroller Reference Manual*.

The MPC5121e/MPC5123 ATA Host Controller design makes data available coincidentally with the active edge of the WRITE strobe in PIO and Multiword DMA modes.

- Write data is latched by the drive at the inactive edge of the WRITE strobe. This gives ample setup-time beyond that required by the ATA-4 specification.
- Data is held unchanged until the next active edge of the WRITE strobe. This gives ample hold-time beyond that required by the ATA-4 specification.

Table 3-27. Timing Parameters PIO Read (continued)

ATA Parameter	PIO Read Mode Timing Parameter	Value	How to meet	SpecID
t_5	t_5	$t_5(min) = t_{co} + t_{su} + t_{buf} + t_{buf} + t_{cable1} + t_{cable2}$	If not met, increase time_2r	A9.23
t_6	t_6	0	—	A9.24
t_A	t_A	$t_{A(min)} = (1.5 + time\_ax) \times T - (t_{co} + t_{sui} + t_{cable2} + t_{cable2} + 2 \times t_{buf})$	calculate and programming time_ax. [1]	A9.25
t_{rd}	t_{rd1}	$t_{rd1(max)} = (-t_{rd}) + (t_{skew3} + t_{skew4})$ $t_{rd1(min)} = (time\_pio\_rdx - 0.5) \times T - (t_{su} + t_{hi})$ $(time\_pio\_rdx - 0.5) \times T > t_{su} + t_{hi} + t_{skew3} + t_{skew4}$	calculate and programming time_pio_rdx. [1]	A9.26
t_0	—	$t_{0(min)} = (time\_1 + time\_2 + time\_9) \times T$	time_1, time_2r, time_9	A9.27

1 See the *MPC5121e Microcontroller Reference Manual.*

In PIO write mode, timing waveforms are somewhat different as shown in Figure 27.

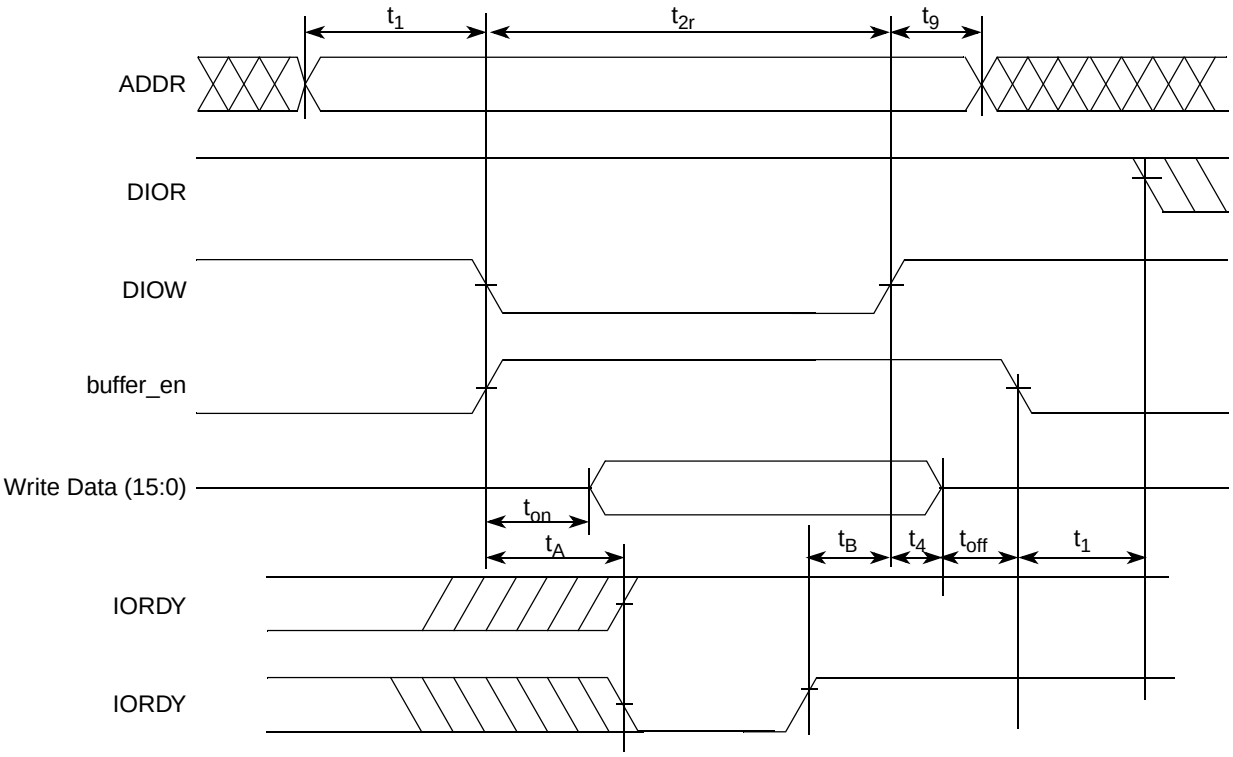

Figure 27. PIO Write Mode Timing

To fulfill this timing, several parameters need to be observed as shown in Table 3-28.

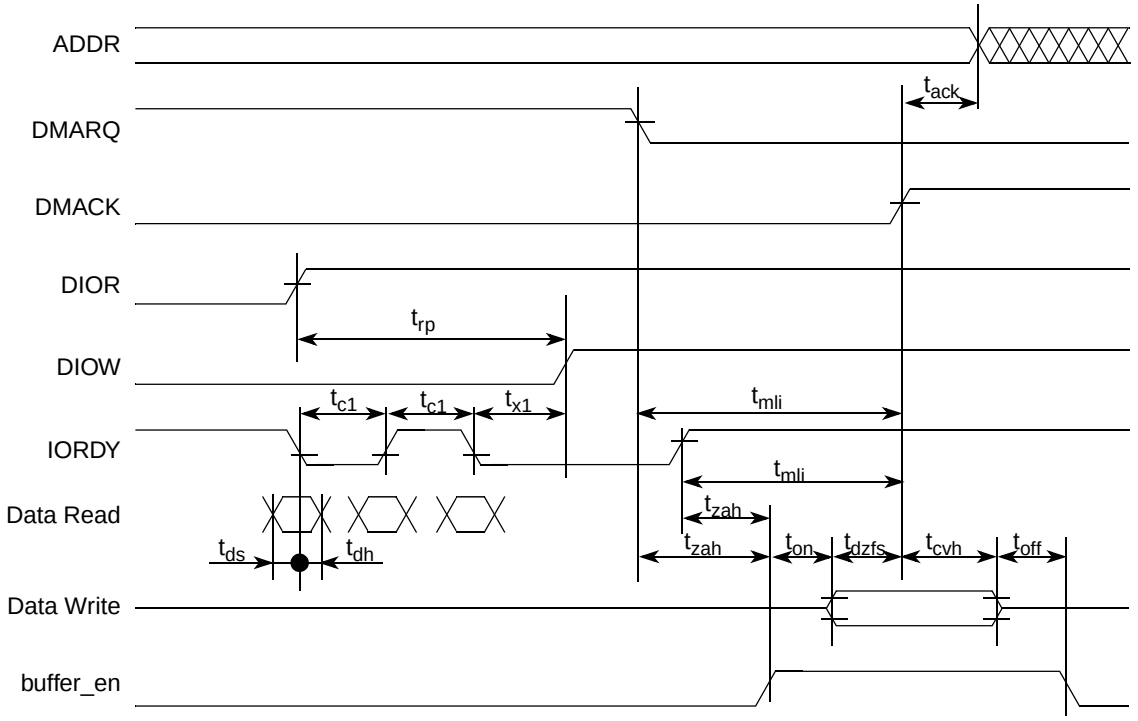

Figure 31. UDMA In Host Terminates Transfer

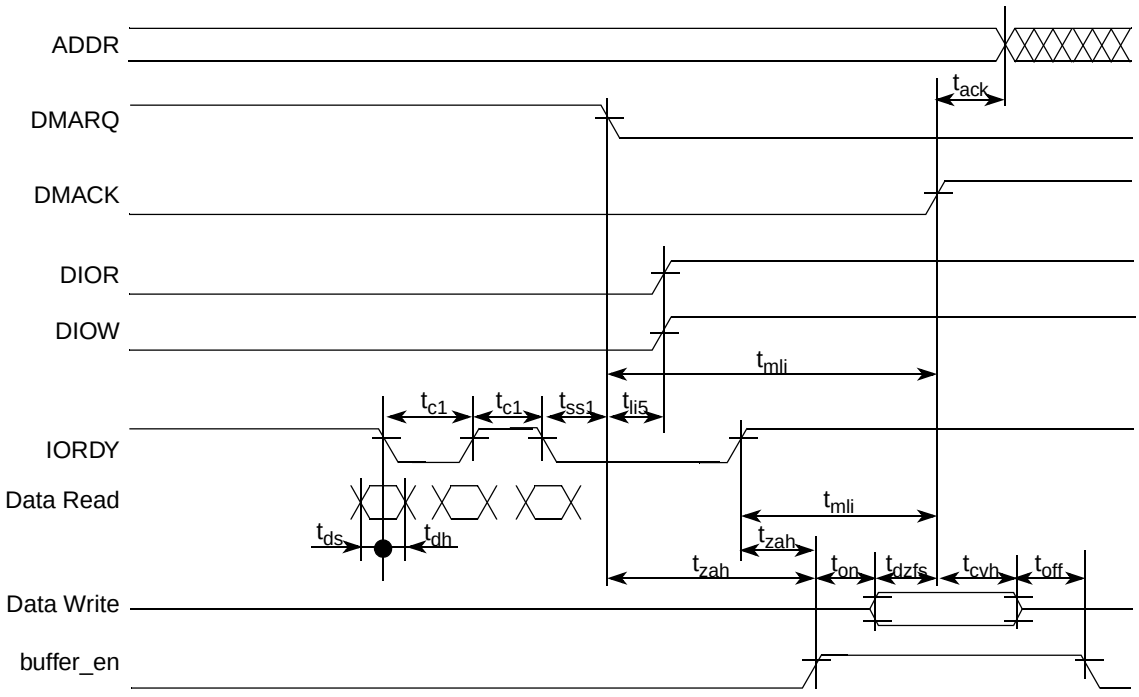

Figure 32. UDMA In Device Terminates Transfer

Timing parameters are explained in Table 30.

3.3.12 USB ULPI

This section specifies the USB ULPI timing.

For more information refer to UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1, October 20, 2004.

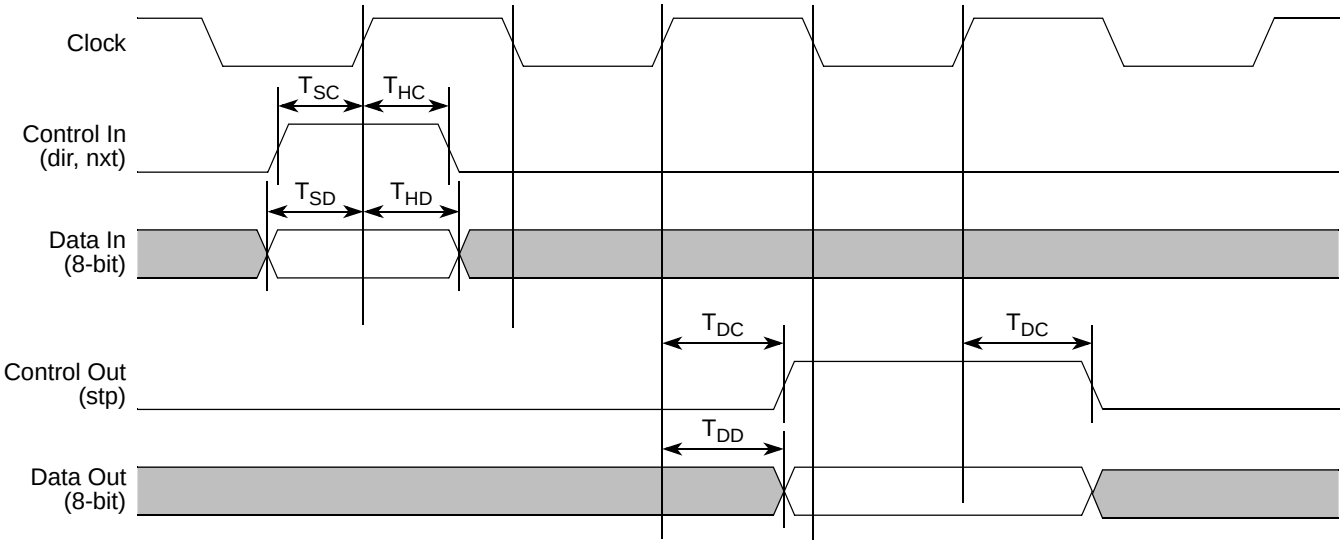

Figure 40. ULPI Timing Diagram

Table 36. Timing Specifications – ULPI

Symbol	Description	Min	Max	Units	SpecID
T_{CK}	Clock Period	15	—	ns	A12.1
T_{SC}, T_{SD}	Setup time (control in, 8-bit data in)	—	6.0	ns	A12.2
T_{HC}, T_{HD}	Hold time (control in, 8-bit data in)	0.0	—	ns	A12.3
T_{DC}, T_{DD}	Output delay (control out, 8-bit data out)	—	9.0	ns	A12.4

NOTE

Output timing is specified at a nominal 50 pF load.

3.3.13 On-Chip USB PHY

The USB PHY is an USB2.0 compatible PHY integrated on-chip. See Chapter 7 in the USB Specification Rev. 2.0 at www.usb.org.

3.3.14 SDHC

Figure 41 shows the timings of the SDHC.

3.3.16 SPDIF

The Sony/Philips Digital Interface (SPDIF) timing is totally asynchronous, therefore there is no need for relationship with the clock.

3.3.17 CAN

The CAN functions are available as TX and CAN3/4_RX pins at normal IO pads and as CAN1/2 RX pins at the VBAT_RTC domain. There is no filter for the WakeUp dominant pulse. Any High-to-Low edge can cause WakeUp, if configured.

3.3.18 I^2C

This section specifies the timing parameters of the Inter-Integrated Circuit (I^2C) interface. Refer to the I^2C Bus Specification.

Table 40. I^2C Input Timing Specifications – SCL and SDA

Symbol	Description	Min	Max	Units	SpecID
1	Start condition hold time	2	—	IP-Bus Cycle[1]	A18.1
2	Clock low time	8	—	IP-Bus Cycle[1]	A18.2
4	Data hold time	0.0	—	ns	A18.3
6	Clock high time	4	—	IP-Bus Cycle[1]	A18.4
7	Data setup time	0.0	—	ns	A18.5
8	Start condition setup time (for repeated start condition only)	2	—	IP-Bus Cycle[1]	A18.6
9	Stop condition setup time	2	—	IP-Bus Cycle[1]	A18.7

1 Inter Peripheral Clock is defined in the MPC5121e/MPC5123 *Reference Manual*.

Table 41. I^2C Output Timing Specifications – SCL and SDA

Symbol	Description	Min	Max	Units	SpecID
1[1]	Start condition hold time	6	—	IP-Bus Cycle[2]	A18.8
2[1]	Clock low time	10	—	IP-Bus Cycle[2]	A18.9
3[3]	SCL/SDA rise time	—	7.9	ns	A18.10
4[1]	Data hold time	7	—	IP-Bus Cycle[2]	A18.11
5[1]	SCL/SDA fall time	—	7.9	ns	A18.12
6[1]	Clock high time	10	—	IP-Bus Cycle[2]	A18.13
7[1]	Data setup time	2	—	IP-Bus Cycle[2]	A18.14
8[1]	Start condition setup time (for repeated start condition only)	20	—	IP-Bus Cycle[2]	A18.15
9[1]	Stop condition setup time	10	—	IP-Bus Cycle[2]	A18.16

1 Programming IFDR with the maximum frequency results in the minimum output timings listed. The I^2C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.

2 Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Inter Peripheral Clock is defined in the *MPC5121e/MPC5123 Reference Manual.*

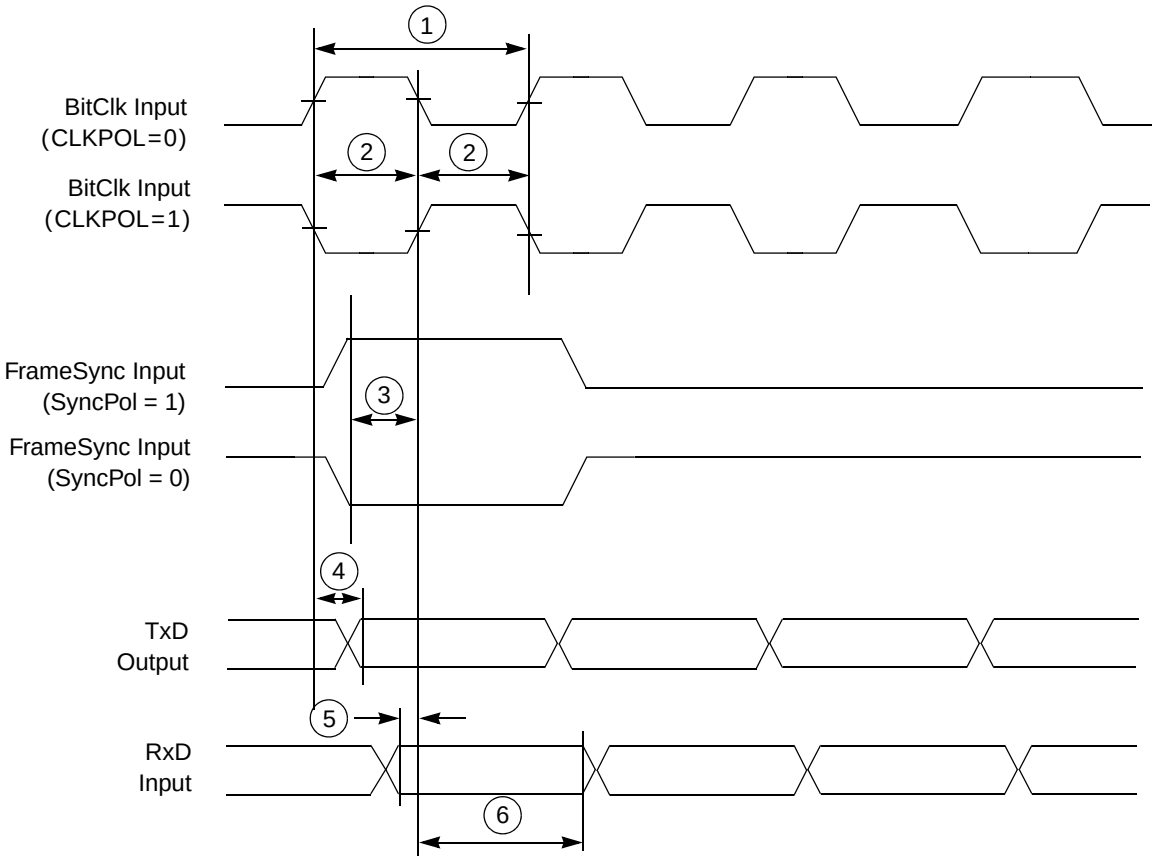

Figure 48. Timing Diagram – 8,16, 24, and 32-bit CODEC/I^{2}S Slave Mode

3.3.20.2 AC97 Mode

Table 44. Timing Specifications – AC97 Mode

Symbol	Description	Min	Typ	Max	Units	SpecID
1	Bit Clock cycle time	—	81.4	—	ns	A20.15
2	Clock pulse high time	—	40.7	—	ns	A20.16
3	Clock pulse low time	—	40.7	—	ns	A20.17
4	FrameSync valid after rising clock edge	—	—	13.0	ns	A20.18
5	Output Data valid after rising clock edge	—	—	14.0	ns	A20.19
6	Input Data setup time	1.0	—	—	ns	A20.20
7	Input Data hold time	1.0	—	—	ns	A20.21

NOTE

Output timing is specified at a nominal 50 pF load.

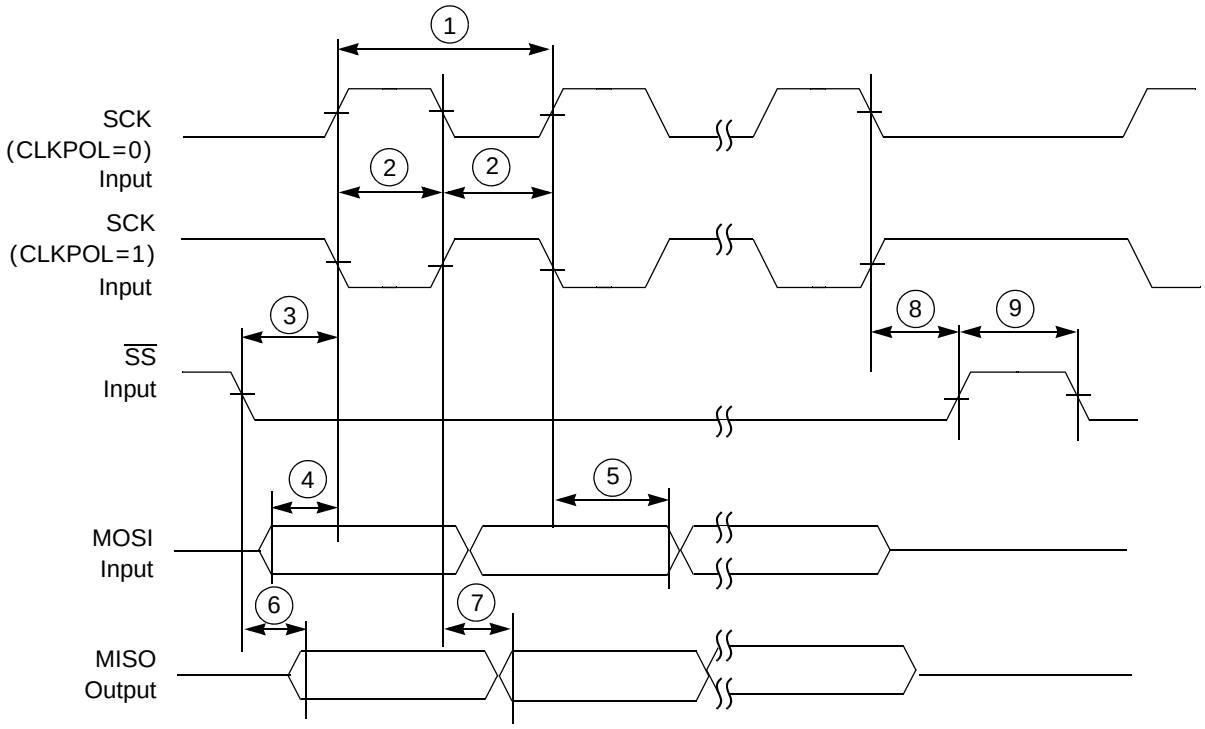

Figure 51. Timing Diagram – SPI Slave Mode, Format 0 (CPHA = 0)

Table 47. Timing Specifications – SPI Master Mode, Format 1 (CPHA = 1)

Symbol	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A20.46
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A20.47
3	Slave select clock delay, programable in the PSC CCS register	30.0	—	ns	A20.48
4	Output data valid	—	8.9	ns	A20.49
5	Input Data setup time	6.0	—	ns	A20.50
6	Input Data hold time	1.0	—	ns	A20.51
7	Slave disable lag time	—	TSCK	ns	A20.52
8	Sequential Transfer delay, programable in the PSC CTUR / CTLR register	15.0	—	ns	A20.53
9	Clock falling time	—	7.9	ns	A20.54
10	Clock rising time	—	7.9	ns	A20.55

NOTE

Output timing is specified at a nominal 50 pF load.

The SATA PHY needs to be powered even if it is not used in an application. In this case, you should not enable the SATA oscillator and the SATA PHY by software.

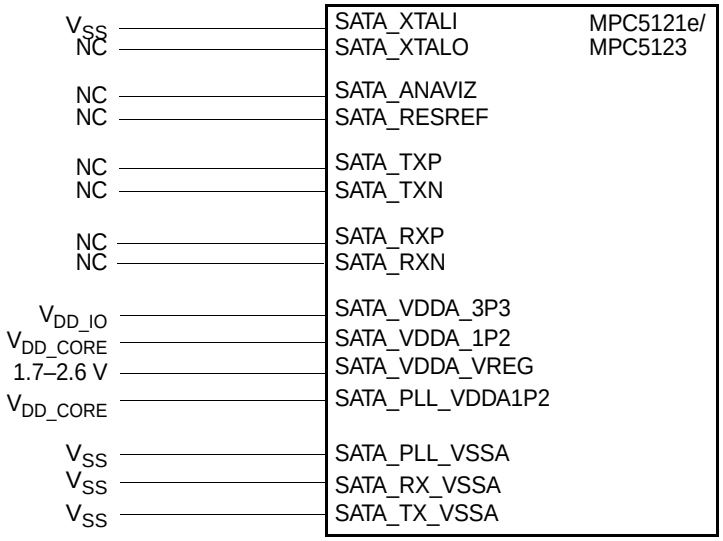

Figure 60. Recommended Connection for Pins of Unused SATA PHY

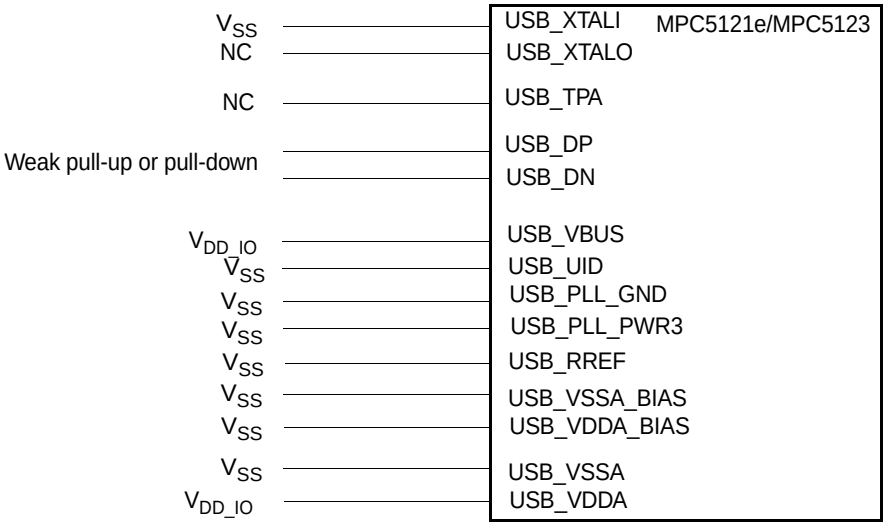

Figure 61. Recommended connection for pins of unused USB PHY

4.4 Pull-Up/Pull-Down Resistor Requirements

The MPC5121e/MPC5123 requires external pull-up or pull-down resistors on certain pins.

4.4.1 Pull-Down Resistor Requirements for TEST pin

The MPC5121e/MPC5123 requires a pull-down resistor on the test pin TEST.

Table 53. COP/BDM Interface Signals

BDM Pin #	MPC5121e/MPC5123 I/O Pin	BDM Connector	Internal Pull Up/Down	External Pull Up/Down	I/O[1]
16	—	GND	—	—	—
15	$\overline{\text{CKSTP\_OUT}}$	ckstp_out	—	10 kΩ Pull-up	I
14	—	KEY	—	—	—
13	$\overline{\text{HRESET}}$	hreset	Pull-up	10 kΩ Pull-up	O
12	—	GND	—	—	—
11	$\overline{\text{SRESET}}$	sreset	Pull-up	10 kΩ Pull-up	O
10	—	N/C	—	—	—
9	TMS	tms	Pull-up	10 kΩ Pull-up	O
8	$\overline{\text{CKSTP\_IN}}$	ckstp_in	—	10 kΩ Pull-up	O
7	TCK	tck	Pull-up	10 kΩ Pull-up	O
6	—	VDD[2]	—	—	—
5	See Note[3]	halted[3]	—	—	I
4	$\overline{\text{TRST}}$	trst	Pull-up	10 kΩ Pull-up	O
3	TDI	tdi	Pull-up	10 kΩ Pull-up	O
2	See Note[4]	qack[4]	—	—	O
1	TDO	tdo	—	—	I

1 With respect to the emulator tool's perspective:
Input is really an output from the embedded e300 core.
Output is really an input to the core.

2 From the board under test, power sense for chip power.

3 HALTED is not available from e300 core.

4 Input to the e300 core to enable/disable soft-stop condition during breakpoints. MPC5121e/MPC5123 internally ties CORE_QACK to GND in its normal/functional mode (always asserted).

For a board with a COP (common on-chip processor) connector that accesses the JTAG interface and needs to reset the JTAG module, only wiring $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ is not recommended.

To reset the MPC5121e/MPC5123 via the COP connector, the $\overline{\text{HRESET}}$ pin of the COP should be connected to the $\overline{\text{HRESET}}$ pin of the MPC5121e/MPC5123. The circuitry shown in Figure 63 allows the COP to assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ separately, while any other board sources can drive $\overline{\text{PORESET}}$.

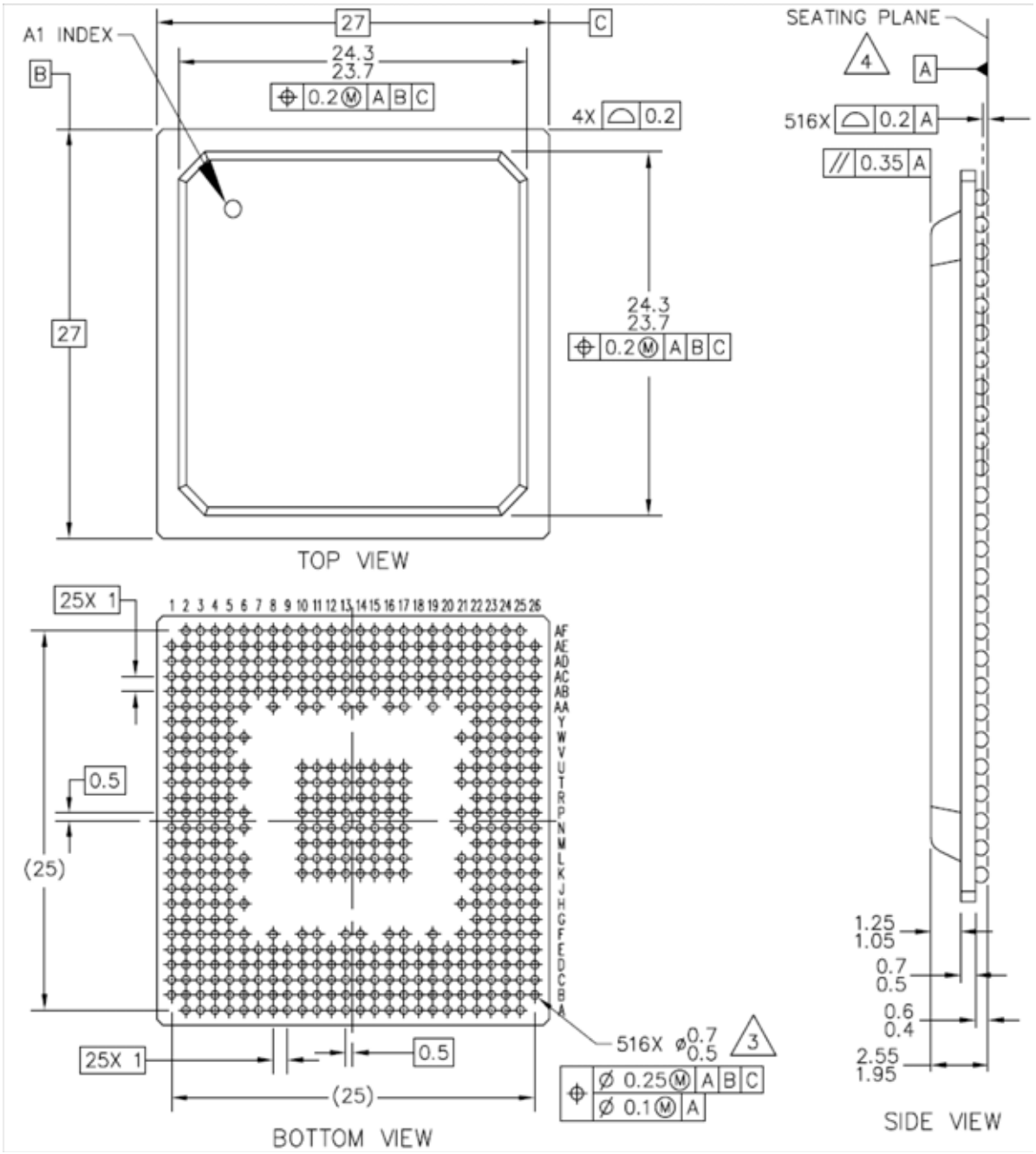

Figure 65. Mechanical Dimension and Bottom Surface Nomenclature of the MPC5121e/MPC5123 TEPBGA

1 All dimensions are in millimeters.
2 Dimensions and tolerances per ASME Y14.5M-1994.
3 Maximum solder ball diameter measured parallel to datum A.
4 Datum A, the seating plane, is determined by the spherical crowns of the solder balls.