## What is "**Embedded - Microcontrollers**"?

"**Embedded - Microcontrollers**" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "**Embedded - Microcontrollers**"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 40 MIPs |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, QEI, WDT |
| Number of I/O | 85 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 24x10/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj64mc710-i-pf |

# dsPIC33FJXXXMCX06/X08/X10

**FIGURE 2-1:** **RECOMMENDED MINIMUM CONNECTION**

**FIGURE 2-1:** RECOMMENDED MINIMUM CONNECTION
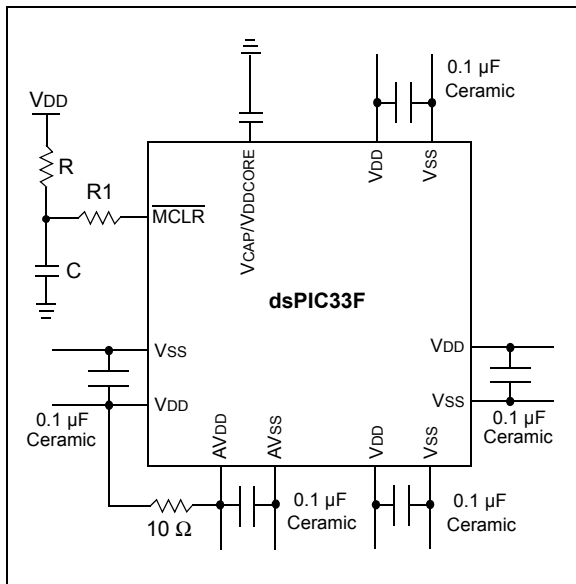
## 2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

## 2.3 Capacitor on Internal Voltage Regulator (VCAP/VDDCORE)

A low-ESR (< 5 Ohms) capacitor is required on the VCAP/VDDCORE pin, which is used to stabilize the voltage regulator output voltage. The VCAP/VDDCORE pin must not be connected to VDD, and must have a capacitor between 4.7 µF and 10 µF, 16V connected to ground. The type can be ceramic or tantalum. Refer to **Section 26.0 "Electrical Characteristics"** for additional information.

The placement of this capacitor should be close to the VCAP/VDDCORE. It is recommended that the trace length not exceed one-quarter inch (6 mm). Refer to **Section 23.2 "On-Chip Voltage Regulator"** for details.

## 2.4 Master Clear ($\overline{\text{MCLR}}$) Pin

The $\overline{\text{MCLR}}$ pin provides for two specific device functions:

- Device Reset
- Device programming and debugging

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{\text{MCLR}}$ pin. Consequently, specific voltage levels ($V_{IH}$ and $V_{IL}$) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor C, be isolated from the $\overline{\text{MCLR}}$ pin during programming and debugging operations.

Place the components shown in Figure 2-2 within one-quarter inch (6 mm) from the $\overline{\text{MCLR}}$ pin.

**FIGURE 2-2:** EXAMPLE OF $\overline{\text{MCLR}}$ PIN CONNECTIONS
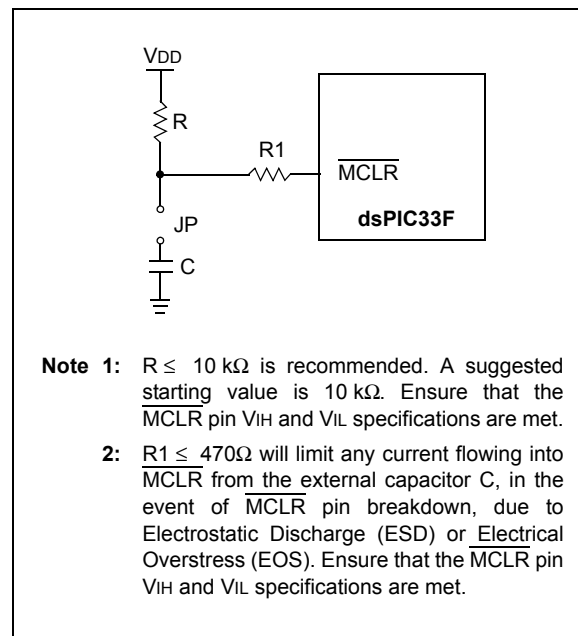


**Note 1:** R $\leq$ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the $\overline{\text{MCLR}}$ pin $V_{IH}$ and $V_{IL}$ specifications are met.

**2:** R1 $\leq$ 470Ω will limit any current flowing into $\overline{\text{MCLR}}$ from the external capacitor C, in the event of $\overline{\text{MCLR}}$ pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the $\overline{\text{MCLR}}$ pin $V_{IH}$ and $V_{IL}$ specifications are met.

**TABLE 4-23:** **ECAN2 REGISTER MAP WHEN C2CTRL1.WIN = 0 OR 1 FOR dsPIC33FJXXXMC708/710 DEVICES**

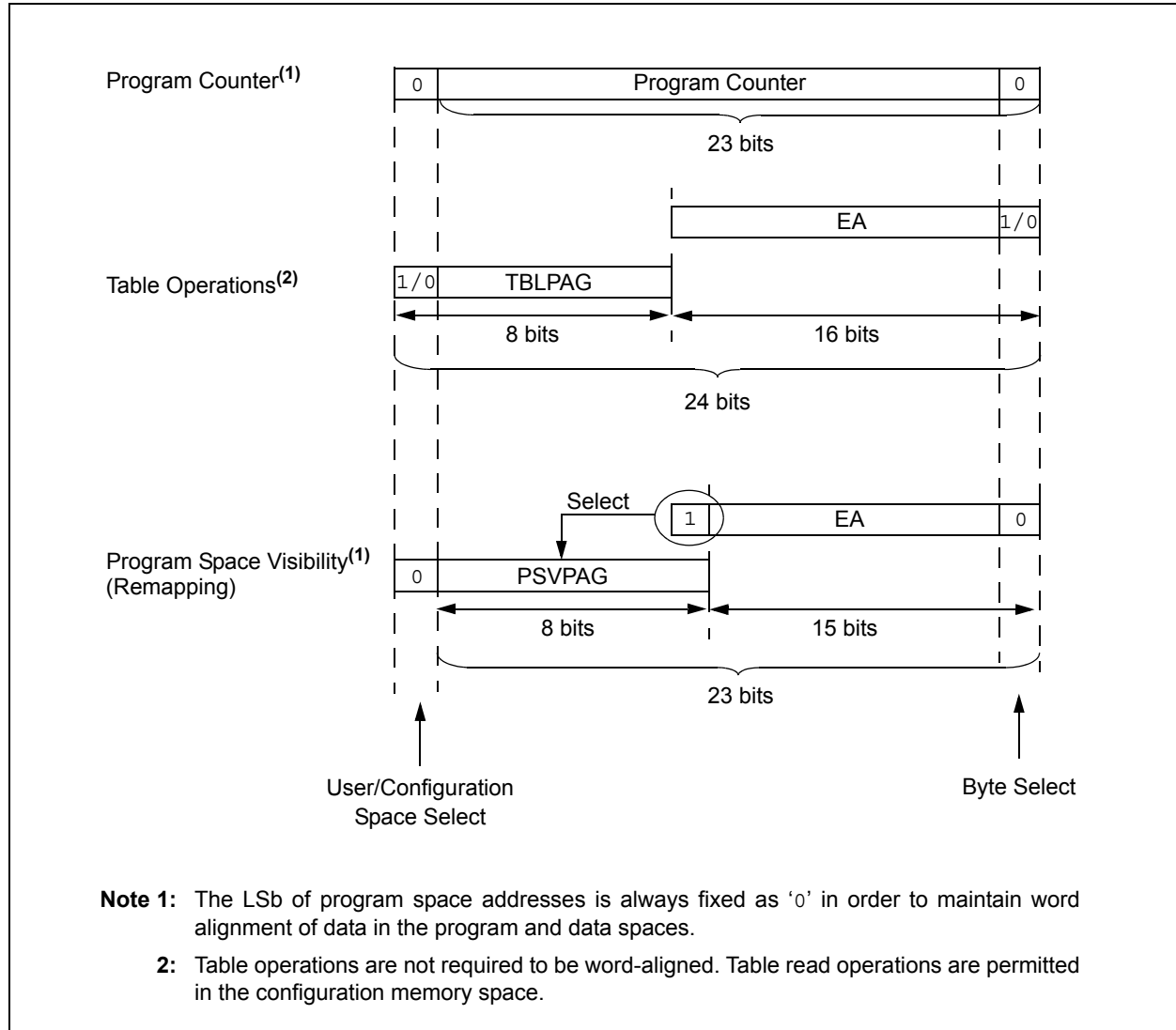| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C2CTRL1 | 0500 | — | — | CSIDL | ABAT | — | REQOP<2:0> | | | OPMODE<2:0> | | | — | CANCAP | — | — | WIN | 0480 |
| C2CTRL2 | 0502 | — | — | — | — | — | — | — | — | — | — | — | DNCNT<4:0> | | | | | 0000 |
| C2VEC | 0504 | — | — | — | FILHIT<4:0> | | | | | — | ICODE<6:0> | | | | | | | 0000 |
| C2FCTRL | 0506 | DMABS<2:0> | | | — | — | — | — | — | — | — | — | FSA<4:0> | | | | | 0000 |
| C2FIFO | 0508 | — | — | FBP<5:0> | | | | | | — | — | FNRB<5:0> | | | | | | 0000 |
| C2INTF | 050A | — | — | TXBO | TXBP | RXBP | TXWAR | RXWAR | EWARN | IVRIF | WAKIF | ERRIF | — | FIFOIF | RBOVIF | RBIF | TBIF | 0000 |
| C2INTE | 050C | — | — | — | — | — | — | — | — | IVRIE | WAKIE | ERRIE | — | FIFOIE | RBOVIE | RBIE | TBIE | 0000 |
| C2EC | 050E | TERRCNT<7:0> | | | | | | | | RERRCNT<7:0> | | | | | | | | 0000 |
| C2CFG1 | 0510 | — | — | — | — | — | — | — | — | SJW<1:0> | | BRP<5:0> | | | | | | 0000 |
| C2CFG2 | 0512 | — | WAKFIL | — | — | — | SEG2PH<2:0> | | | SEG2PHTS | SAM | SEG1PH<2:0> | | | PRSEG<2:0> | | | 0000 |
| C2FEN1 | 0514 | FLTEN15 | FLTEN14 | FLTEN13 | FLTEN12 | FLTEN11 | FLTEN10 | FLTEN9 | FLTEN8 | FLTEN7 | FLTEN6 | FLTEN5 | FLTEN4 | FLTEN3 | FLTEN2 | FLTEN1 | FLTEN0 | FFFF |
| C2FMSKSEL1 | 0518 | F7MSK<1:0> | | F6MSK<1:0> | | F5MSK<1:0> | | F4MSK<1:0> | | F3MSK<1:0> | | F2MSK<1:0> | | F1MSK<1:0> | | F0MSK<1:0> | | 0000 |
| C2FMSKSEL2 | 051A | F15MSK<1:0> | | F14MSK<1:0> | | F13MSK<1:0> | | F12MSK<1:0> | | F11MSK<1:0> | | F10MSK<1:0> | | F9MSK<1:0> | | F8MSK<1:0> | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-24:** **ECAN2 REGISTER MAP WHEN C2CTRL1.WIN = 0 FOR dsPIC33FJXXXMC708/710 DEVICES**

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0500-051E | See definition when WIN = x | | | | | | | | | | | | | | | | |
| C2RXFUL1 | 0520 | RXFUL15 | RXFUL14 | RXFUL13 | RXFUL12 | RXFUL11 | RXFUL10 | RXFUL9 | RXFUL8 | RXFUL7 | RXFUL6 | RXFUL5 | RXFUL4 | RXFUL3 | RXFUL2 | RXFUL1 | RXFUL0 | 0000 |
| C2RXFUL2 | 0522 | RXFUL31 | RXFUL30 | RXFUL29 | RXFUL28 | RXFUL27 | RXFUL26 | RXFUL25 | RXFUL24 | RXFUL23 | RXFUL22 | RXFUL21 | RXFUL20 | RXFUL19 | RXFUL18 | RXFUL17 | RXFUL16 | 0000 |
| C2RXOVF1 | 0528 | RXOVF15 | RXOVF14 | RXOVF13 | RXOVF12 | RXOVF11 | RXOVF10 | RXOVF09 | RXOVF08 | RXOVF7 | RXOVF6 | RXOVF5 | RXOVF4 | RXOVF3 | RXOVF2 | RXOVF1 | RXOVF0 | 0000 |
| C2RXOVF2 | 052A | RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 | RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 | 0000 |
| C2TR01CON | 0530 | TXEN1 | TX ABAT1 | TX LARB1 | TX ERR1 | TX REQ1 | RTREN1 | TX1PRI<1:0> | | TXEN0 | TX ABAT0 | TX LARB0 | TX ERR0 | TX REQ0 | RTREN0 | TX0PRI<1:0> | | 0000 |
| C2TR23CON | 0532 | TXEN3 | TX ABAT3 | TX LARB3 | TX ERR3 | TX REQ3 | RTREN3 | TX3PRI<1:0> | | TXEN2 | TX ABAT2 | TX LARB2 | TX ERR2 | TX REQ2 | RTREN2 | TX2PRI<1:0> | | 0000 |
| C2TR45CON | 0534 | TXEN5 | TX ABAT5 | TX LARB5 | TX ERR5 | TX REQ5 | RTREN5 | TX5PRI<1:0> | | TXEN4 | TX ABAT4 | TX LARB4 | TX ERR4 | TX REQ4 | RTREN4 | TX4PRI<1:0> | | 0000 |
| C2TR67CON | 0536 | TXEN7 | TX ABAT7 | TX LARB7 | TX ERR7 | TX REQ7 | RTREN7 | TX7PRI<1:0> | | TXEN6 | TX ABAT6 | TX LARB6 | TX ERR6 | TX REQ6 | RTREN6 | TX6PRI<1:0> | | xxxx |
| C2RXD | 0540 | Recieved Data Word | | | | | | | | | | | | | | | | xxxx |
| C2TXD | 0542 | Transmit Data Word | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**FIGURE 4-9:** **DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION**



**Note 1:** The LSb of program space addresses is always fixed as '0' in order to maintain word alignment of data in the program and data spaces.

**2:** Table operations are not required to be word-aligned. Table read operations are permitted in the configuration memory space.

**REGISTER 7-24: IPC9: INTERRUPT PRIORITY CONTROL REGISTER 9**

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC5IP<2:0> | | | — | IC4IP<2:0> | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC3IP<2:0> | | | — | DMA3IP<2:0> | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared    x = Bit is unknown |

bit 15          **Unimplemented:** Read as '0'

bit 14-12       **IC5IP<2:0>:** Input Capture Channel 5 Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 11          **Unimplemented:** Read as '0'

bit 10-8        **IC4IP<2:0>:** Input Capture Channel 4 Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 7           **Unimplemented:** Read as '0'

bit 6-4         **IC3IP<2:0>:** Input Capture Channel 3 Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 3           **Unimplemented:** Read as '0'

bit 2-0         **DMA3IP<2:0>:** DMA Channel 3 Data Transfer Complete Interrupt Priority bits

111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

**REGISTER 7-27: IPC12: INTERRUPT PRIORITY CONTROL REGISTER 12**

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | T8IP<2:0> | | | — | MI2C2IP<2:0> | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-1 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SI2C2IP<2:0> | | | — | T7IP<2:0> | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **T8IP<2:0>:** Timer8 Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **MI2C2IP<2:0>:** I2C2 Master Events Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SI2C2IP<2:0>:** I2C2 Slave Events Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **T7IP<2:0>:** Timer7 Interrupt Priority bits
111 = Interrupt is priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is priority 1
000 = Interrupt source is disabled

**REGISTER 9-3:    PLLFBD: PLL FEEDBACK DIVISOR REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0[1] |
|-----|-----|-----|-----|-----|-----|-----|------|
| — | — | — | — | — | — | — | PLLDIV<8> |

bit 15 {.right} bit 8

| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-----|-----|-----|-----|-----|-----|-----|------|
| PLLDIV<7:0> | | | | | | | |

bit 7 {.right} bit 0

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared    x = Bit is unknown |

bit 15-9    **Unimplemented:** Read as '0'

bit 8-0    **PLLDIV<8:0>:** PLL Feedback Divisor bits (also denoted as 'M', PLL multiplier)

000000000 = 2
000000001 = 3
000000010 = 4
•
•
•
000110000 = 50 (default)
•
•
•
111111111 = 513

## 11.0 I/O PORTS

> **Note:** This data sheet summarizes the features of the dsPIC33FJXXXMCX06/X08/X10 family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "I/O Ports"** (DS70193) in the *"dsPIC33F Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

All of the device pins (except VDD, VSS, MCLR and OSC1/CLKIN) are shared between the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

### 11.1 Parallel I/O (PIO) Ports

A parallel I/O port that shares a pin with a peripheral is, in general, subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through," in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 shows how ports are shared with other peripherals and the associated I/O pin to which they are connected.

When a peripheral is enabled and actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin may be read, but the output driver for the parallel port bit will be disabled. If a peripheral is enabled but the peripheral is not actively driving a pin, that pin may be driven by a port.

All port pins have three registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx), read the latch. Writes to the latch, write the latch. Reads from the port (PORTx), read the port pins, while writes to the port pins, write the latch.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers and the port pins will read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs. An example is the INT4 pin.

> **Note:** The voltage on a digital input pin can be between -0.3V to 5.6V.

**FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE**
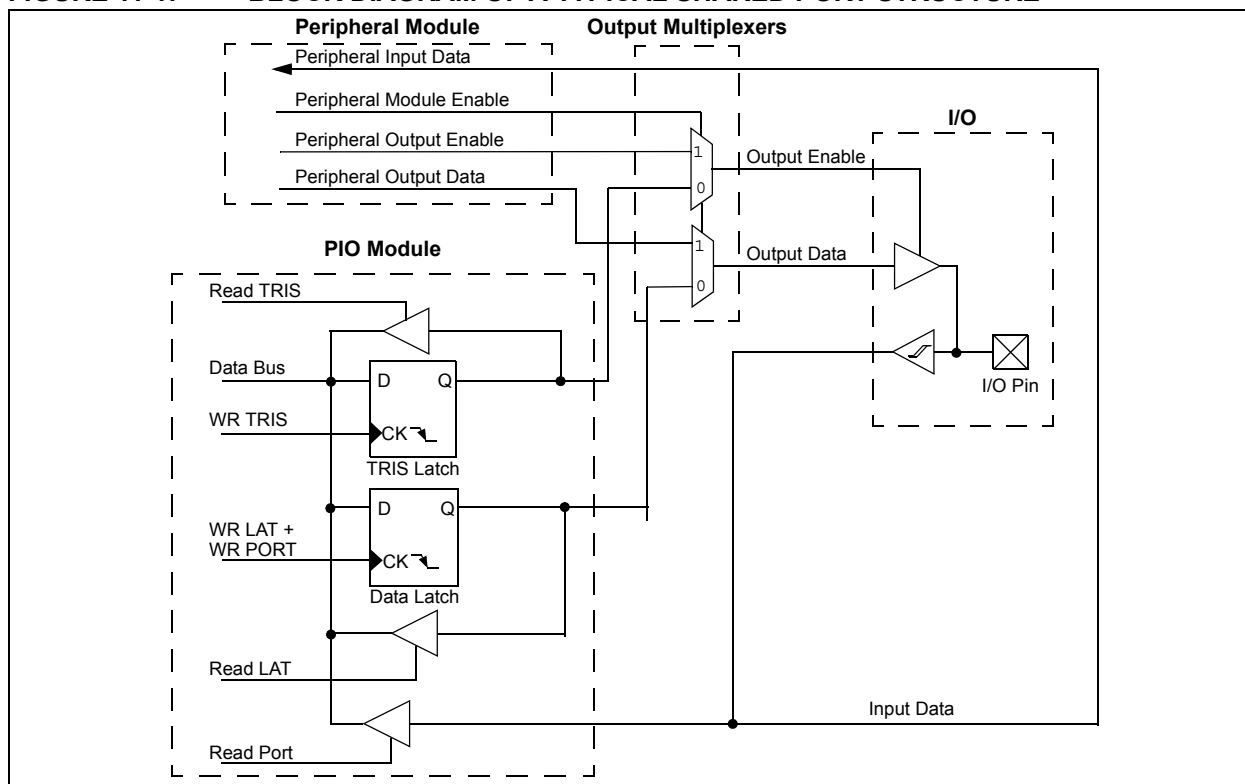
**REGISTER 16-9:    PxFLTACON: FAULT A CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| FAOV4H | FAOV4L | FAOV3H | FAOV3L | FAOV2H | FAOV2L | FAOV1H | FAOV1L |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-----|-----|-----|-------|-------|-------|-------|
| FLTAM | — | — | — | FAEN4 | FAEN3 | FAEN2 | FAEN1 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---------|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8     **FAOVxH<4:1>:FAOVxL<4:1>:** Fault Input A PWM Override Value bits

1 = The PWM output pin is driven active on an external Fault input event
0 = The PWM output pin is driven inactive on an external Fault input event

bit 7          **FLTAM:** Fault A Mode bit

1 = The Fault A input pin functions in the Cycle-by-Cycle mode
0 = The Fault A input pin latches all control pins to the states programmed in FLTACON<15:8>

bit 6-4       **Unimplemented:** Read as '0'

bit 3          **FAEN4:** Fault Input A Enable bit

1 = PWM4H/PWM4L pin pair is controlled by Fault Input A
0 = PWM4H/PWM4L pin pair is not controlled by Fault Input A

bit 2          **FAEN3:** Fault Input A Enable bit

1 = PWM3H/PWM3L pin pair is controlled by Fault Input A
0 = PWM3H/PWM3L pin pair is not controlled by Fault Input A

bit 1          **FAEN2:** Fault Input A Enable bit

1 = PWM2H/PWM2L pin pair is controlled by Fault Input A
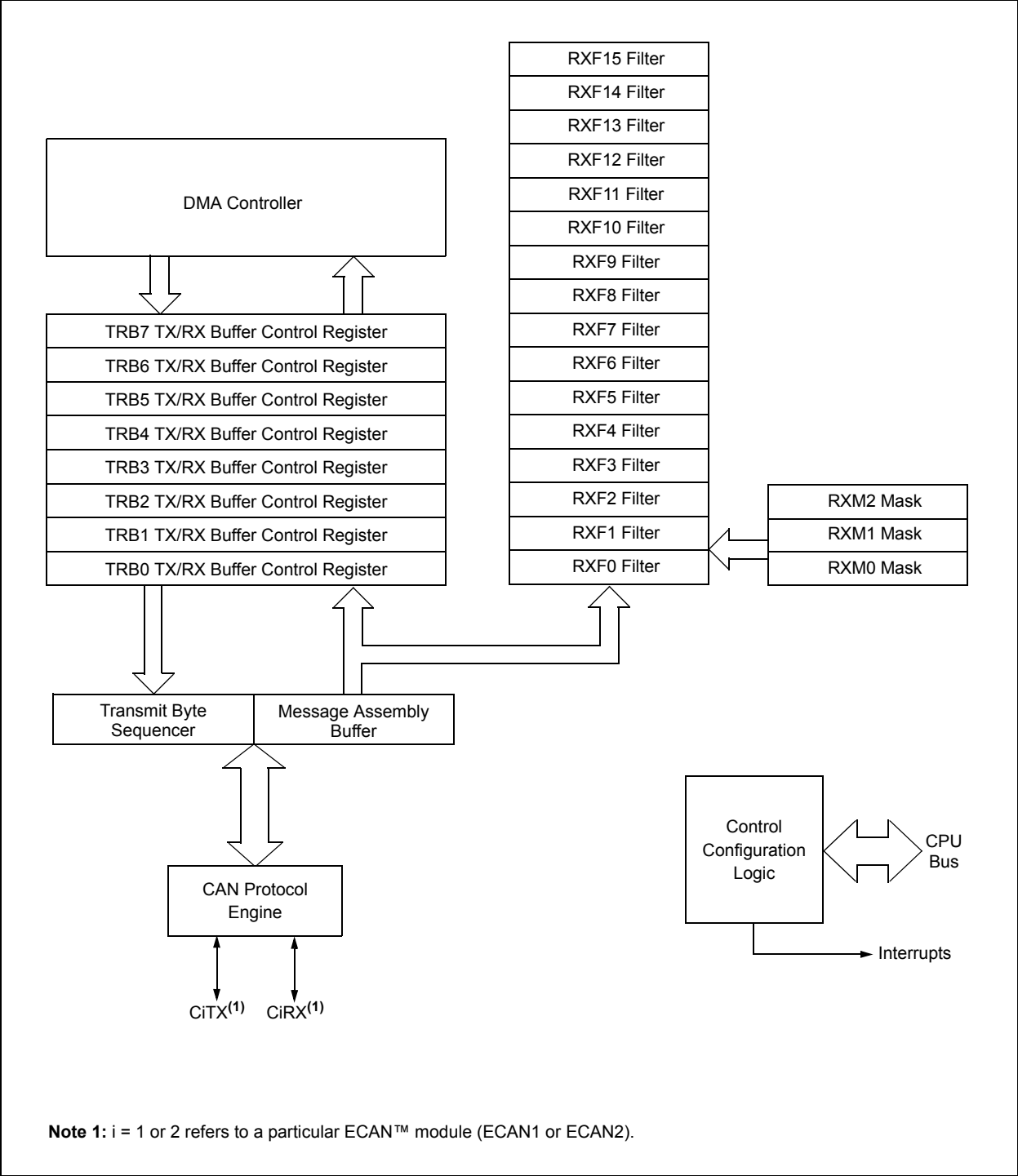0 = PWM2H/PWM2L pin pair is not controlled by Fault Input A

bit 0          **FAEN1:** Fault Input A Enable bit

1 = PWM1H/PWM1L pin pair is controlled by Fault Input A
0 = PWM1H/PWM1L pin pair is not controlled by Fault Input A

**FIGURE 21-1:** **ECAN™ MODULE BLOCK DIAGRAM**



**Note 1:** i = 1 or 2 refers to a particular ECAN™ module (ECAN1 or ECAN2).

**REGISTER 21-16: CiRXFnSID: ECAN™ ACCEPTANCE FILTER n STANDARD IDENTIFIER (n = 0, 1, ...,15)**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | U-0 | R/W-x | U-0 | R/W-x | R/W-x |
|-------|-------|-------|-----|-------|-----|-------|-------|
| SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---------|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared    x = Bit is unknown |

bit 15-5    **SID<10:0>:** Standard Identifier bits

1 = Message address bit SIDx must be '1' to match filter
0 = Message address bit SIDx must be '0' to match filter

bit 4    **Unimplemented:** Read as '0'

bit 3    **EXIDE:** Extended Identifier Enable bit

If MIDE = 1 then:
1 = Match only messages with extended identifier addresses
0 = Match only messages with standard identifier addresses
If MIDE = 0 then:
Ignore EXIDE bit.

bit 2    **Unimplemented:** Read as '0'

bit 1-0    **EID<17:16>:** Extended Identifier bits

1 = Message address bit EIDx must be '1' to match filter
0 = Message address bit EIDx must be '0' to match filter

**REGISTER 21-17: CiRXFnEID: ECAN™ ACCEPTANCE FILTER n EXTENDED IDENTIFIER (n = 0, 1, ..., 15)**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EID15 | EID14 | EID13 | EID12 | EID11 | EID10 | EID9 | EID8 |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|-------|-------|-------|-------|-------|-------|-------|-------|
| EID7 | EID6 | EID5 | EID4 | EID3 | EID2 | EID1 | EID0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---------|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared    x = Bit is unknown |

bit 15-0    **EID<15:0>:** Extended Identifier bits

1 = Message address bit EIDx must be '1' to match filter
0 = Message address bit EIDx must be '0' to match filter

**TABLE 23-2:** **dsPIC33FJXXXMCX06/X08/X10 CONFIGURATION BITS DESCRIPTION (CONTINUED)**

| Bit Field | Register | Description |
|---|---|---|
| HPOL | FPOR | Motor Control PWM High Side Polarity bit<br>`1` = PWM module high side output pins have active-high output polarity<br>`0` = PWM module high side output pins have active-low output polarity |
| LPOL | FPOR | Motor Control PWM Low Side Polarity bit<br>`1` = PWM module low side output pins have active-high output polarity<br>`0` = PWM module low side output pins have active-low output polarity |
| FPWRT<2:0> | FPOR | Power-on Reset Timer Value Select bits<br>`111` = PWRT = 128 ms<br>`110` = PWRT = 64 ms<br>`101` = PWRT = 32 ms<br>`100` = PWRT = 16 ms<br>`011` = PWRT = 8 ms<br>`010` = PWRT = 4 ms<br>`001` = PWRT = 2 ms<br>`000` = PWRT = Disabled |
| JTAGEN | FICD | JTAG Enable bits<br>`1` = JTAG enabled<br>`0` = JTAG disabled |
| ICS<1:0> | FICD | ICD Communication Channel Select bits<br>`11` = Communicate on PGEC1 and PGED1<br>`10` = Communicate on PGEC2 and PGED2<br>`01` = Communicate on PGEC3 and PGED3<br>`00` = Reserved |

## 23.5 JTAG Interface

dsPIC33FJXXXMCX06/X08/X10 devices implement a JTAG interface, which supports boundary scan device testing, as well as in-circuit programming. Detailed information on the interface will be provided in future revisions of the document.

## 23.6 Code Protection and CodeGuard™ Security

The dsPIC33FJXXXMCX06/X08/X10 devices offer the advanced implementation of CodeGuard™ Security. CodeGuard Security enables multiple parties to securely share resources (memory, interrupts and peripherals) on a single chip. This feature helps protect individual Intellectual Property in collaborative system designs.

When coupled with software encryption libraries, CodeGuard Security can be used to securely update Flash even when multiple IP are resident on the single chip. The code protection features vary depending on the actual device implemented. The following sections provide an overview of these features.

The code protection features are controlled by the Configuration registers: FBS, FSS and FGS.

| Note: | Refer to **Section 23. "CodeGuard™ Security"** (DS70199) in the *"dsPIC33F Family Reference Manual"* for further information on usage, configuration and operation of CodeGuard Security. |
|---|---|

## 23.7 In-Circuit Serial Programming

dsPIC33FJXXXMCX06/X08/X10 family digital signal controllers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data and three other lines for power, ground and the programming sequence. This allows customers to manufacture boards with unprogrammed devices and then program the digital signal controller just before shipping the product. This also allows the most recent firmware or a custom firmware, to be programmed. Please refer to the "*dsPIC33F/PIC24H Flash Programming Specification*" (DS70152) document for details about ICSP.

Any one out of three pairs of programming clock/data pins may be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

## 23.8 In-Circuit Debugger

When MPLAB® ICD 2 is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pin functions.

Any one out of three pairs of debugging clock/data pins may be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

To use the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{MCLR}$, $V_{DD}$, $V_{SS}$ and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

**TABLE 24-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | | Description | # of Words | # of Cycles | Status Flags Affected |
|---|---|---|---|---|---|---|---|
| 66 | RRNC | RRNC | f | f = Rotate Right (No Carry) f | 1 | 1 | N,Z |
| | | RRNC | f,WREG | WREG = Rotate Right (No Carry) f | 1 | 1 | N,Z |
| | | RRNC | Ws,Wd | Wd = Rotate Right (No Carry) Ws | 1 | 1 | N,Z |
| 67 | SAC | SAC | Acc,#Slit4,Wdo | Store Accumulator | 1 | 1 | None |
| | | SAC.R | Acc,#Slit4,Wdo | Store Rounded Accumulator | 1 | 1 | None |
| 68 | SE | SE | Ws,Wnd | Wnd = sign-extended Ws | 1 | 1 | C,N,Z |
| 69 | SETM | SETM | f | f = 0xFFFF | 1 | 1 | None |
| | | SETM | WREG | WREG = 0xFFFF | 1 | 1 | None |
| | | SETM | Ws | Ws = 0xFFFF | 1 | 1 | None |
| 70 | SFTAC | SFTAC | Acc,Wn | Arithmetic Shift Accumulator by (Wn) | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | SFTAC | Acc,#Slit6 | Arithmetic Shift Accumulator by Slit6 | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| 71 | SL | SL | f | f = Left Shift f | 1 | 1 | C,N,OV,Z |
| | | SL | f,WREG | WREG = Left Shift f | 1 | 1 | C,N,OV,Z |
| | | SL | Ws,Wd | Wd = Left Shift Ws | 1 | 1 | C,N,OV,Z |
| | | SL | Wb,Wns,Wnd | Wnd = Left Shift Wb by Wns | 1 | 1 | N,Z |
| | | SL | Wb,#lit5,Wnd | Wnd = Left Shift Wb by lit5 | 1 | 1 | N,Z |
| 72 | SUB | SUB | Acc | Subtract Accumulators | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | SUB | f | f = f – WREG | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | f,WREG | WREG = f – WREG | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | #lit10,Wn | Wn = Wn – lit10 | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | Wb,Ws,Wd | Wd = Wb – Ws | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | Wb,#lit5,Wd | Wd = Wb – lit5 | 1 | 1 | C,DC,N,OV,Z |
| 73 | SUBB | SUBB | f | f = f – WREG – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | f,WREG | WREG = f – WREG – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | #lit10,Wn | Wn = Wn – lit10 – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | Wb,Ws,Wd | Wd = Wb – Ws – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | Wb,#lit5,Wd | Wd = Wb – lit5 – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| 74 | SUBR | SUBR | f | f = WREG – f | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR | f,WREG | WREG = WREG – f | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR | Wb,Ws,Wd | Wd = Ws – Wb | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR | Wb,#lit5,Wd | Wd = lit5 – Wb | 1 | 1 | C,DC,N,OV,Z |
| 75 | SUBBR | SUBBR | f | f = WREG – f – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR | f,WREG | WREG = WREG – f – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR | Wb,Ws,Wd | Wd = Ws – Wb – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR | Wb,#lit5,Wd | Wd = lit5 – Wb – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| 76 | SWAP | SWAP.b | Wn | Wn = nibble swap Wn | 1 | 1 | None |
| | | SWAP | Wn | Wn = byte swap Wn | 1 | 1 | None |
| 77 | TBLRDH | TBLRDH | Ws,Wd | Read Prog<23:16> to Wd<7:0> | 1 | 2 | None |
| 78 | TBLRDL | TBLRDL | Ws,Wd | Read Prog<15:0> to Wd | 1 | 2 | None |
| 79 | TBLWTH | TBLWTH | Ws,Wd | Write Ws<7:0> to Prog<23:16> | 1 | 2 | None |
| 80 | TBLWTL | TBLWTL | Ws,Wd | Write Ws to Prog<15:0> | 1 | 2 | None |
| 81 | ULNK | ULNK | | Unlink Frame Pointer | 1 | 1 | None |
| 82 | XOR | XOR | f | f = f .XOR. WREG | 1 | 1 | N,Z |
| | | XOR | f,WREG | WREG = f .XOR. WREG | 1 | 1 | N,Z |
| | | XOR | #lit10,Wn | Wd = lit10 .XOR. Wd | 1 | 1 | N,Z |
| | | XOR | Wb,Ws,Wd | Wd = Wb .XOR. Ws | 1 | 1 | N,Z |
| | | XOR | Wb,#lit5,Wd | Wd = Wb .XOR. lit5 | 1 | 1 | N,Z |
| 83 | ZE | ZE | Ws,Wnd | Wnd = Zero-extend Ws | 1 | 1 | C,Z,N |

**TABLE 26-6:** DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

| DC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature   -40°C ≤ TA ≤ +85°C for Industrial | | |
|---|---|---|---|---|---|---|
| Parameter No. | Typical[1] | Max | Units | Conditions | | |
| **Idle Current (IIDLE): Core OFF Clock ON Base Current[2]** | | | | | | |
| DC40d | 3 | 25 | mA | -40°C | 3.3V | 10 MIPS |
| DC40a | 3 | 25 | mA | +25°C | | |
| DC40b | 3 | 25 | mA | +85°C | | |
| DC41d | 4 | 25 | mA | -40°C | 3.3V | 16 MIPS |
| DC41a | 5 | 25 | mA | +25°C | | |
| DC41b | 6 | 25 | mA | +85°C | | |
| DC42d | 8 | 25 | mA | -40°C | 3.3V | 20 MIPS |
| DC42a | 9 | 25 | mA | +25°C | | |
| DC42b | 10 | 25 | mA | +85°C | | |
| DC43a | 15 | 25 | mA | +25°C | 3.3V | 30 MIPS |
| DC43d | 15 | 25 | mA | -40°C | | |
| DC43b | 15 | 25 | mA | +85°C | | |
| DC44d | 16 | 25 | mA | -40°C | 3.3V | 40 MIPS |
| DC44a | 16 | 25 | mA | +25°C | | |
| DC44b | 16 | 25 | mA | +85°C | | |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

**2:** Base IIDLE current is measured with core off, clock on and all modules turned off. Peripheral Module Disable SFR registers are zeroed. All I/O pins are configured as inputs and pulled to VSS.

**TABLE 26-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature   -40°C ≤ TA ≤ +85°C for Industrial | | | | | |
|---|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min | Typ | Max | Units | Conditions | |
| | VOL | **Output Low Voltage** | | | | | | |
| DO10 | | I/O ports | — | — | 0.4 | V | $I_{OL}$ = 2mA, $V_{DD}$ = 3.3V | |
| DO16 | | OSC2/CLKO | — | — | 0.4 | V | $I_{OL}$ = 2mA, $V_{DD}$ = 3.3V | |
| | VOH | **Output High Voltage** | | | | | | |
| DO20 | | I/O ports | 2.40 | — | — | V | $I_{OH}$ = -2.3 mA, $V_{DD}$ = 3.3V | |
| DO26 | | OSC2/CLKO | 2.41 | — | — | V | $I_{OH}$ = -1.3 mA, $V_{DD}$ = 3.3V | |

**TABLE 26-11: ELECTRICAL CHARACTERISTICS: BOR**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature   -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min[1] | Typ | Max[1] | Units | Conditions |
| BO10 | VBOR | BOR Event on $V_{DD}$ transition high-to-low BOR event is tied to $V_{DD}$ core voltage decrease | 2.40 | — | 2.55 | V | — |

**Note 1:** Parameters are for design guidance only and are not tested in manufacturing.

**TABLE 26-17: PLL CLOCK TIMING SPECIFICATIONS (VDD = 3.0V TO 3.6V)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature   -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min | Typ[1] | Max | Units | Conditions |
| OS50 | FPLLI | PLL Voltage Controlled Oscillator (VCO) Input Frequency Range[2] | 0.8 | — | 8.0 | MHz | ECPLL, HSPLL, XTPLL modes |
| OS51 | FSYS | On-Chip VCO System Frequency | 100 | — | 200 | MHz | — |
| OS52 | TLOCK | PLL Start-up Time (Lock Time) | 0.9 | 1.5 | 3.1 | ms | — |
| OS53 | DCLK | CLKO Stability (Jitter) | -3.0 | 0.5 | 3.0 | % | Measured over 100 ms period |

**Note 1:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

**TABLE 26-18: AC CHARACTERISTICS: INTERNAL FRC ACCURACY**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature        -40°C ≤ TA ≤ +85°C for Industrial | | | |
|---|---|---|---|---|---|---|
| Param No. | Characteristic | Min | Typ | Max | Units | Conditions |
| | **Internal FRC Accuracy @ FRC Frequency = 7.37 MHz[1,2]** | | | | | |
| F20 | FRC | -2 | — | +2 | % | -40°C ≤ TA ≤ +85°C         VDD = 3.0-3.6V |

**Note 1:** Frequency calibrated at 25°C and 3.3V. TUN bits can be used to compensate for temperature drift.
**2:** FRC set to initial frequency of 7.37 MHz (+1-2%) at 25° C FRC.
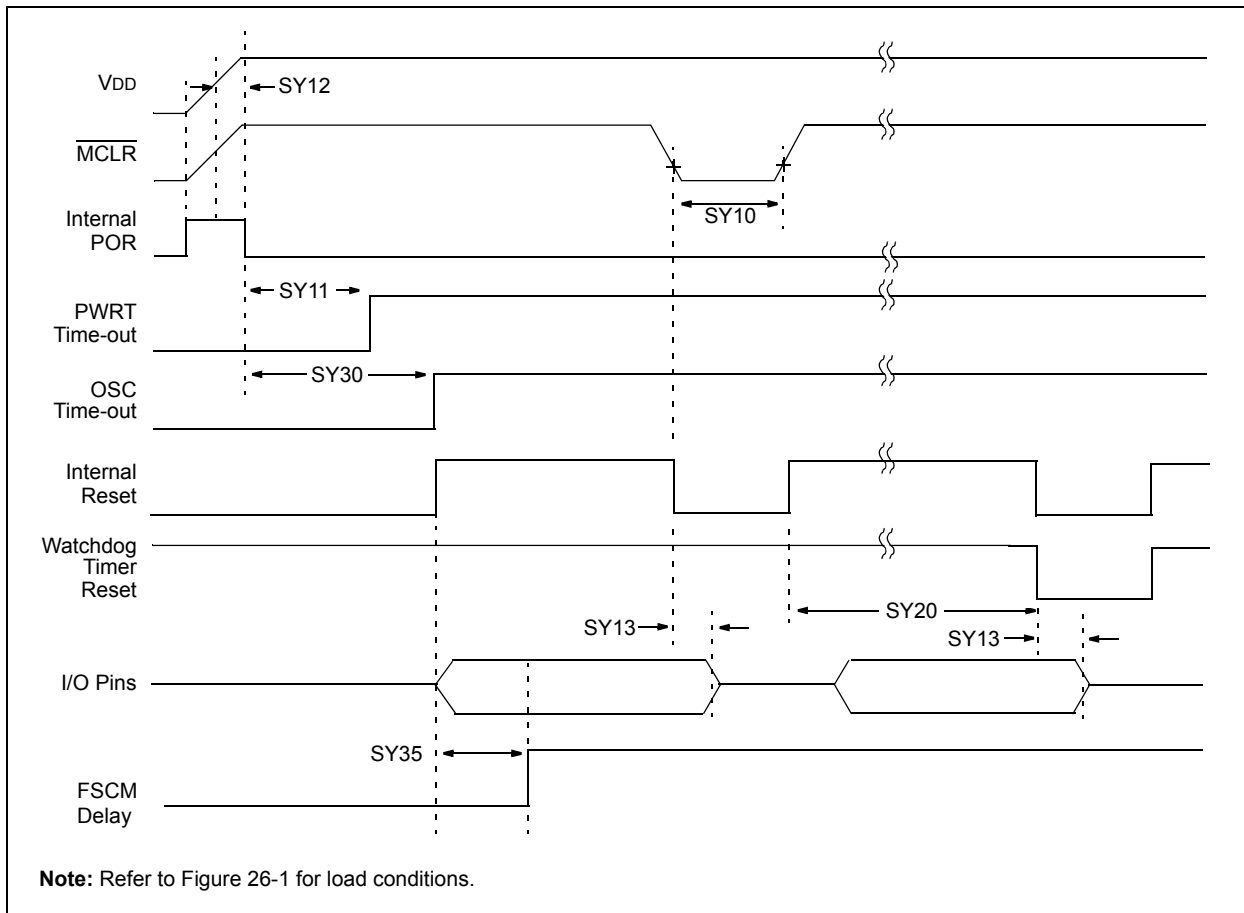
**TABLE 26-19: INTERNAL LPRC ACCURACY**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature   -40°C ≤ TA ≤ +85°C for Industrial | | | |
|---|---|---|---|---|---|---|
| Param No. | Characteristic | Min | Typ | Max | Units | Conditions |
| | **LPRC @ 32.768 kHz[1]** | | | | | |
| F21 | | -20 | ±6 | +20 | % | -40°C ≤ TA ≤ +85°C         VDD = 3.0-3.6V |

**Note 1:** Change of LPRC frequency as VDD changes.

**FIGURE 26-4:** RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING CHARACTERISTICS



**Note:** Refer to Figure 26-1 for load conditions.

**FIGURE 26-11:** QEA/QEB INPUT CHARACTERISTICS
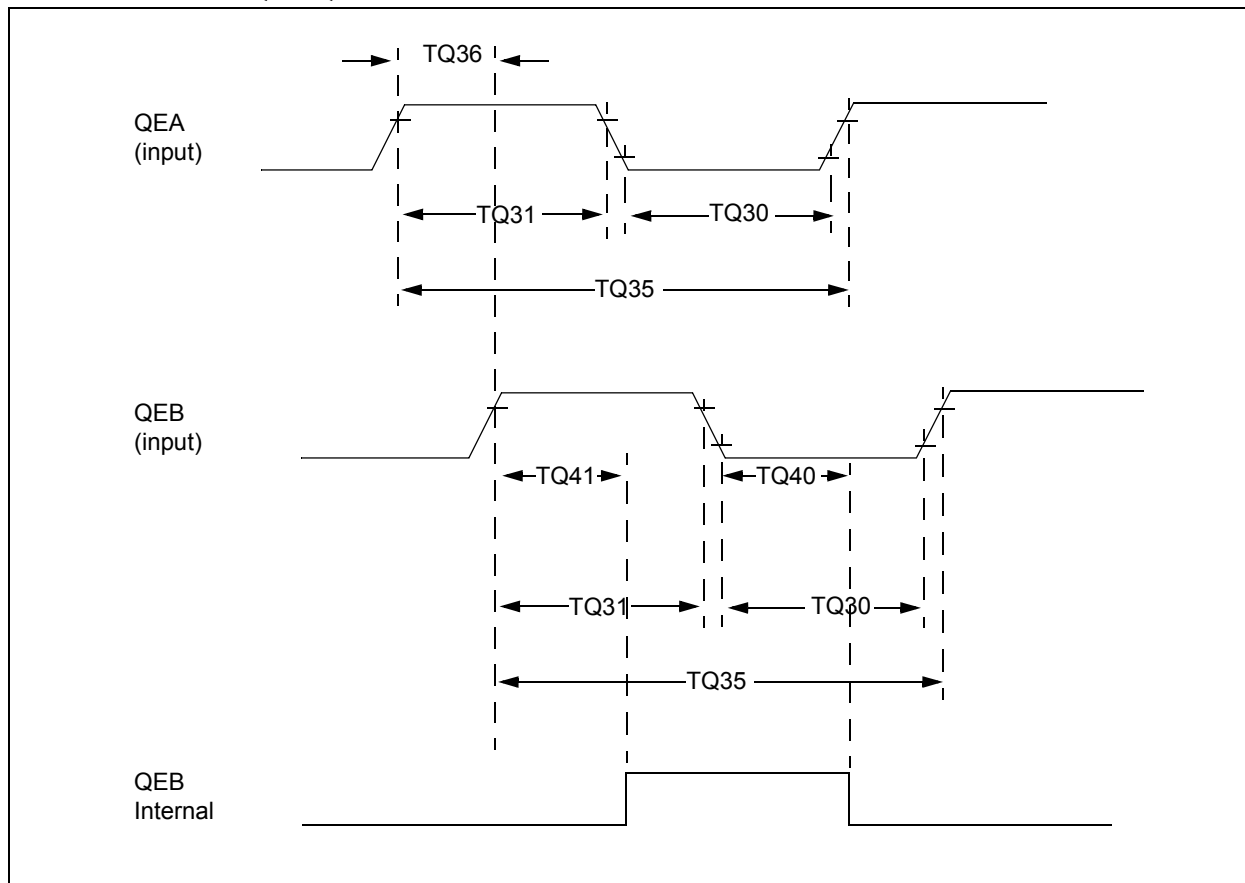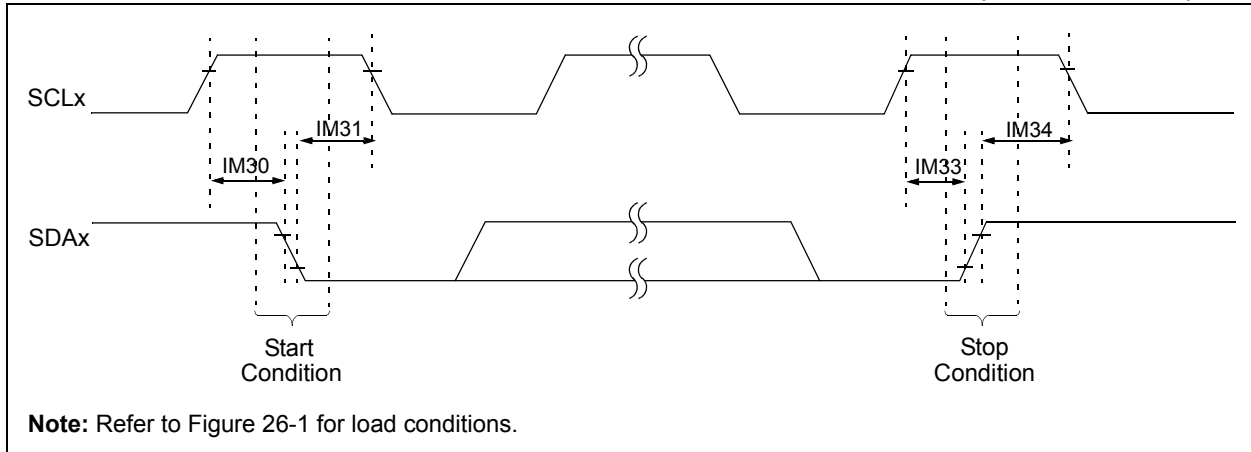


**TABLE 26-29: QUADRATURE DECODER TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature  -40°C ≤ TA ≤ +85°C for Industrial | | | |
|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic[1] | Typ[2] | Max | Units | Conditions |
| TQ30 | TQUL | Quadrature Input Low Time | 6 TCY | — | ns | — |
| TQ31 | TQUH | Quadrature Input High Time | 6 TCY | — | ns | — |
| TQ35 | TQUIN | Quadrature Input Period | 12 TCY | — | ns | — |
| TQ36 | TQUP | Quadrature Phase Period | 3 TCY | — | ns | — |
| TQ40 | TQUFL | Filter Time to Recognize Low, with Digital Filter | 3 * N * TCY | — | ns | N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 3)** |
| TQ41 | TQUFH | Filter Time to Recognize High, with Digital Filter | 3 * N * TCY | — | ns | N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 3)** |

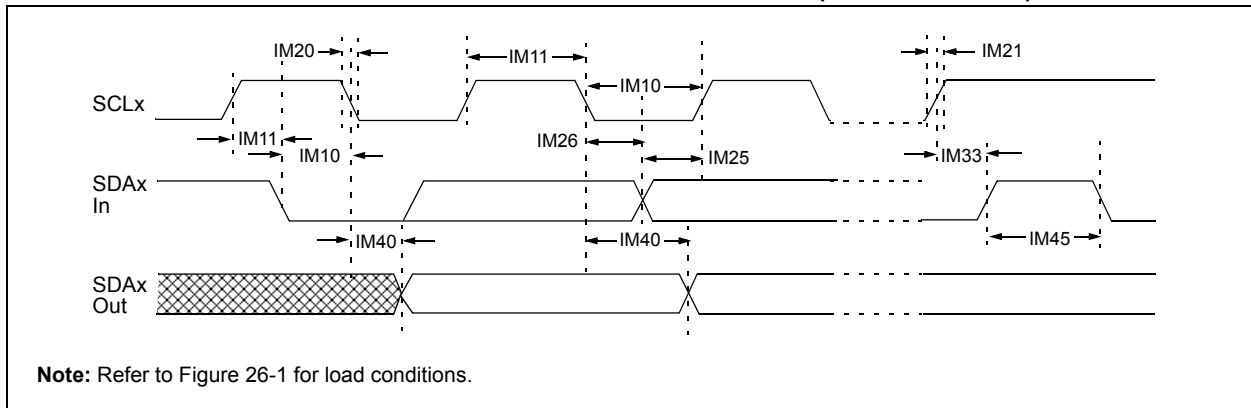**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

**3:** N = Index Channel Digital Filter Clock Divide Select bits. Refer to **Section 15. "Quadrature Encoder Interface (QEI)"** (DS70208) in the "*dsPIC33F Family Reference Manual*".

**FIGURE 26-18:** **I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)**



**Note:** Refer to Figure 26-1 for load conditions.

**FIGURE 26-19:** **I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)**



**Note:** Refer to Figure 26-1 for load conditions.

**TABLE 26-42: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature   -40°C ≤ TA ≤ +85°C for Industrial | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min. | Typ[1] | Max. | Units | Conditions |
| **Clock Parameters** | | | | | | | |
| AD50a | $T_{AD}$ | ADC Clock Period | 117.6 | — | — | ns | — |
| AD51a | $t_{RC}$ | ADC Internal RC Oscillator Period | — | 250 | — | ns | — |
| **Conversion Rate** | | | | | | | |
| AD55a | $t_{CONV}$ | Conversion Time | — | 14 $T_{AD}$ | | — | — |
| AD56a | $F_{CNV}$ | Throughput Rate | — | — | 500 | ksps | — |
| AD57a | $T_{SAMP}$ | Sample Time | 3.0 $T_{AD}$ | — | — | — | — |
| **Timing Parameters** | | | | | | | |
| AD60a | $t_{PCS}$ | Conversion Start from Sample Trigger[2] | 2.0 $T_{AD}$ | — | 3.0 $T_{AD}$ | — | — |
| AD61a | $t_{PSS}$ | Sample Start from Setting Sample (SAMP) bit[2] | 2.0 $T_{AD}$ | — | 3.0 $T_{AD}$ | — | — |
| AD62a | $t_{CSS}$ | Conversion Completion to Sample Start (ASAM = 1)[2] | — | 0.5 $T_{AD}$ | — | — | — |
| AD63a | $t_{DPU}$ | Time to Stabilize Analog Stage from ADC Off to ADC On[2,3] | — | — | 20 | µs | — |

**Note 1:** These parameters are characterized but not tested in manufacturing.

    **2:** Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

    **3:** $t_{DPU}$ is the time required for the ADC module to stabilize when it is turned on (AD1CON1<ADON> = 1). During this time, the ADC result is indeterminate.