# E·XFL

#### NXP USA Inc. - MK60DN256VLL10 Datasheet



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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I <sup>2</sup> S, LVD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 33x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk60dn256vll10

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



**Terminology and guidelines** 





# 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

# 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.



# 5.2.2 LVD and POR operating requirements

Table 2. V<sub>DD</sub> supply LVD and POR operating requirements

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>POR</sub>	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V <sub>LVDH</sub>	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V <sub>LVW1H</sub>	Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V <sub>LVW2H</sub>	Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V <sub>LVW3H</sub>	Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V <sub>LVW4H</sub>	Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V <sub>HYSH</sub>	Low-voltage inhibit reset/recover hysteresis — high range	_	±80	_	mV	
V <sub>LVDL</sub>	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V <sub>LVW1L</sub>	Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V <sub>LVW2L</sub>	Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V <sub>LVW3L</sub>	Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V <sub>LVW4L</sub>	Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V <sub>HYSL</sub>	Low-voltage inhibit reset/recover hysteresis — low range	_	±60		mV	
V <sub>BG</sub>	Bandgap voltage reference	0.97	1.00	1.03	V	
t <sub>LPO</sub>	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

#### Table 3. VBAT power operating requirements

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>POR_VBAT</sub>	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	



General

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.71	_	mA	7
I <sub>DD_VLPW</sub>	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.77		mA	8
I <sub>DD_STOP</sub>	Stop mode current at 3.0 V					
	<ul> <li>@ -40 to 25°C</li> </ul>	—	0.74	1.41	mA	
	• @ 70°C	—	2.45	11.5	mA	
	• @ 105°C	—	6.61	30	mA	
I <sub>DD_VLPS</sub>	Very-low-power stop mode current at 3.0 V					
	<ul> <li>@ -40 to 25°C</li> </ul>	—	83	435	μA	
	• @ 70°C	—	425	2000	μA	
	• @ 105°C	—	1280	4000	μA	
I <sub>DD_LLS</sub>	Low leakage stop mode current at 3.0 V					9
	<ul> <li>@ -40 to 25°C</li> </ul>	—	4.58	19.9	μA	
	• @ 70°C	—	30.6	105	μA	
	• @ 105°C	—	137	500	μA	
I <sub>DD_VLLS3</sub>	Very low-leakage stop mode 3 current at 3.0 V					9
	<ul> <li>@ -40 to 25°C</li> </ul>	—	3.0	23	μA	
	• @ 70°C	—	18.6	43	μA	
	• @ 105°C	—	84.9	230	μA	
I <sub>DD_VLLS2</sub>	Very low-leakage stop mode 2 current at 3.0 V					
	<ul> <li>● -40 to 25°C</li> </ul>	—	2.2	5.4	μA	
	• @ 70°C	—	9.3	35	μA	
	• @ 105°C	—	41.4	128	μA	
I <sub>DD_VLLS1</sub>	Very low-leakage stop mode 1 current at 3.0 V					
	<ul> <li>● -40 to 25°C</li> </ul>	—	2.1	9	μA	
	• @ 70°C	—	7.6	28	μA	
	• @ 105°C	—	33.5	95.5	μA	
I <sub>DD_VBAT</sub>	Average current with RTC and 32kHz disabled at 3.0 V					
	• @ -40 to 25°C		0.19	0.22	υA	
	• @ 70°C		0.49	0.64	μA	
	• @ 105°C	_	2.2	3.2	μΑ	

 Table 6. Power consumption operating behaviors (continued)

Table continues on the next page ...



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I <sub>DD_VBAT</sub>	Average current when CPU is not accessing RTC registers					10
	• @ 1.8V					
	● @ -40 to 25°C	_	0.57	0.67	μA	
	• @ 70°C	_	0.90	1.2	μA	
	• @ 105°C		2.4	3.5	μA	
	• @ 3.0V					
	<ul> <li>@ -40 to 25°C</li> </ul>		0.67	0.94	μA	
	• @ 70°C		1.0	1.4	μA	
	• @ 105°C	_	2.7	3.9	μA	

#### Table 6. Power consumption operating behaviors (continued)

- 1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
- 2. 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock . MCG configured for FEI mode. All peripheral clocks disabled.
- 3. 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
- 4. Max values are measured with CPU executing DSP instructions.
- 5. 25MHz core and system clock, 25MHz bus clock, and 12.5MHz FlexBus and flash clock. MCG configured for FEI mode.
- 6. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
- 7. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
- 8. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
- 9. Data reflects devices with 128 KB of RAM. For devices with 64 KB of RAM, power consumption is reduced by 2 µA.
- 10. Includes 32kHz oscillator current and RTC operation.

### 5.2.5.1 Diagram: Typical IDD\_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at greater than 50 MHz frequencies.
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL



Figure 7. Test Access Port timing





# 6.2 System modules

There are no specifications necessary for the device's system modules.

# 6.3 Clock modules



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>DD</sub>	Supply voltage	1.71	_	3.6	V	
I <sub>DDOSC</sub>	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	_	nA	
	• 4 MHz	—	200	_	μA	
	• 8 MHz (RANGE=01)	—	300	_	μA	
	• 16 MHz	—	950	_	μA	
	• 24 MHz	—	1.2	_	mA	
	• 32 MHz	—	1.5	_	mA	
IDDOSC	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	_	μA	
	• 4 MHz	—	400	_	μA	
	• 8 MHz (RANGE=01)	—	500	_	μA	
	• 16 MHz	—	2.5	_	mA	
	• 24 MHz	—	3	_	mA	
	• 32 MHz	—	4	_	mA	
C <sub>x</sub>	EXTAL load capacitance	_	_	_		2, 3
Cy	XTAL load capacitance	_		_		2, 3
R <sub>F</sub>	Feedback resistor — low-frequency, low-power mode (HGO=0)	_	_	_	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	_	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	_			MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	_	1		MΩ	-
R <sub>S</sub>	Series resistor — low-frequency, low-power mode (HGO=0)	_			kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	_	200		kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	_			kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
		_	0	_	kΩ	

## 6.3.2.1 Oscillator DC electrical specifications Table 16. Oscillator DC electrical specifications

Table continues on the next page...





Figure 10. EzPort Timing Diagram

## 6.4.3 Flexbus switching specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB\_CLK. The FB\_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB\_CLK). All other timing relationships can be derived from these values.

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation		FB_CLK	MHz	
FB1	Clock period	20	_	ns	
FB2	Address, data, and control output valid	_	11.5	ns	1
FB3	Address, data, and control output hold	0.5	_	ns	1
FB4	Data and FB_TA input setup	8.5	_	ns	2
FB5	Data and FB_TA input hold	0.5	—	ns	2

Table 25. Flexbus limited voltage range switching specifications

1. Specification is valid for all FB\_AD[31:0], FB\_BE/BWEn, FB\_CSn, FB\_OE, FB\_R/W, FB\_TBST, FB\_TSIZ[1:0], FB\_ALE, and FB\_TS.



### 6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 27 and Table 28 are achievable on the differential pins ADCx\_DP0, ADCx\_DM0, ADCx\_DP1, ADCx\_DM1, ADCx\_DP3, and ADCx\_DM3.

The ADCx\_DP2 and ADCx\_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in Table 29 and Table 30.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	Absolute	1.71	—	3.6	V	
$\Delta V_{DDA}$	Supply voltage	Delta to V <sub>DD</sub> (V <sub>DD</sub> – V <sub>DDA</sub> )	-100	0	+100	mV	2
$\Delta V_{SSA}$	Ground voltage	Delta to V <sub>SS</sub> (V <sub>SS</sub> – V <sub>SSA</sub> )	-100	0	+100	mV	2
V <sub>REFH</sub>	ADC reference voltage high		1.13	V <sub>DDA</sub>	V <sub>DDA</sub>	V	
V <sub>REFL</sub>	ADC reference voltage low		V <sub>SSA</sub>	V <sub>SSA</sub>	V <sub>SSA</sub>	V	
V <sub>ADIN</sub>	Input voltage	16-bit differential mode	VREFL	_	31/32 * VREFH	V	
		All other modes	VREFL	—	VREFH		
C <sub>ADIN</sub>	Input capacitance	16-bit mode	—	8	10	pF	
		<ul> <li>8-bit / 10-bit / 12-bit modes</li> </ul>	_	4	5		
R <sub>ADIN</sub>	Input resistance		—	2	5	kΩ	
R <sub>AS</sub>	Analog source resistance	13-bit / 12-bit modes f <sub>ADCK</sub> < 4 MHz	_	_	5	kΩ	3
f <sub>ADCK</sub>	ADC conversion clock frequency	≤ 13-bit mode	1.0	_	18.0	MHz	4
f <sub>ADCK</sub>	ADC conversion clock frequency	16-bit mode	2.0	_	12.0	MHz	4
C <sub>rate</sub>	ADC conversion	≤ 13-bit modes					5
	rate	No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	_	818.330	Ksps	

#### 6.6.1.1 16-bit ADC operating conditions Table 27. 16-bit ADC operating conditions

Table continues on the next page...

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
C <sub>rate</sub>	ADC conversion	16-bit mode					5
	rate	No ADC hardware averaging	37.037	_	461.467	Ksps	
		Continuous conversions enabled, subsequent conversion time					

 Table 27.
 16-bit ADC operating conditions (continued)

- 1. Typical values assume  $V_{DDA}$  = 3.0 V, Temp = 25 °C,  $f_{ADCK}$  = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
- 2. DC potential difference.
- 3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8  $\Omega$  analog source resistance. The R<sub>AS</sub>/C<sub>AS</sub> time constant should be kept to < 1 ns.
- 4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
- 5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.



Figure 13. ADC input impedance equivalency diagram

#### 6.6.1.2 16-bit ADC electrical characteristics Table 28. 16-bit ADC characteristics (V<sub>REFH</sub> = V<sub>DDA</sub>, V<sub>REFL</sub> = V<sub>SSA</sub>)

Symbol	Description	Conditions <sup>1</sup> .	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
I <sub>DDA_ADC</sub>	Supply current		0.215		1.7	mA	3

Table continues on the next page ...



Peripheral operating requirements and behaviors



Figure 18. Typical INL error vs. digital code





Figure 19. Offset at half scale vs. temperature

## 6.6.4 Voltage reference electrical specifications

Table 34.	VREF full-range	operating	requirements

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	1.71 3.6		V	
T <sub>A</sub>	Temperature	Operating temperature range of the device		°C	
CL	Output load capacitance	1(	00	nF	1, 2

1. C<sub>L</sub> must be connected to VREF\_OUT if the VREF\_OUT functionality is being used for either an internal or external reference.

 The load capacitance should not exceed +/-25% of the nominal specified C<sub>L</sub> value over the operating temperature range of the device.



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>out</sub>	Voltage reference output with factory trim at nominal $V_{\text{DDA}}$ and temperature=25C	1.1915	1.195	1.1977	V	
V <sub>out</sub>	Voltage reference output — factory trim	1.1584	—	1.2376	V	
V <sub>out</sub>	Voltage reference output — user trim	1.193	—	1.197	V	
V <sub>step</sub>	Voltage reference trim step	—	0.5	—	mV	
V <sub>tdrift</sub>	Temperature drift (Vmax -Vmin across the full temperature range)		_	80	mV	
I <sub>bg</sub>	Bandgap only current	—	—	80	μA	1
I <sub>lp</sub>	Low-power buffer current	—	—	360	uA	1
I <sub>hp</sub>	High-power buffer current	—	—	1	mA	1
$\Delta V_{LOAD}$	Load regulation				μV	1, 2
	• current = ± 1.0 mA	_	200	_		
T <sub>stup</sub>	Buffer startup time	_	—	100	μs	
V <sub>vdrift</sub>	Voltage drift (Vmax -Vmin across the full voltage range)	_	2	_	mV	1

Table 35. VREF full-range operating behaviors

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.

2. Load regulation voltage is the difference between the VREF\_OUT voltage with no load vs. voltage with defined load

#### Table 36. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>A</sub>	Temperature	0	50	°C	

#### Table 37. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>out</sub>	Voltage reference output with factory trim	1.173	1.225	V	

## 6.7 Timers

See General switching specifications.

# 6.8 Communication interfaces



### 6.8.3 USB DCD electrical specifications Table 40. USB DCD electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
V <sub>DP_SRC</sub>	USB_DP source voltage (up to 250 µA)	0.5	_	0.7	V
V <sub>LGC</sub>	Threshold voltage for logic high	0.8	—	2.0	V
I <sub>DP_SRC</sub>	USB_DP source current	7	10	13	μA
I <sub>DM_SINK</sub>	USB_DM sink current	50	100	150	μA
R <sub>DM_DWN</sub>	D- pulldown resistance for data pin contact detect	14.25	—	24.8	kΩ
V <sub>DAT_REF</sub>	Data detect voltage	0.25	0.33	0.4	V

# 6.8.4 USB VREG electrical specifications

#### Table 41. USB VREG electrical specifications

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I <sub>DDon</sub>	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	_	120	186	μA	
I <sub>DDstby</sub>	Quiescent current — Standby mode, load current equal zero	—	1.1	10	μA	
I <sub>DDoff</sub>	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25 °C	_	650	_	nA	
	Across operating voltage and temperature		—	4	μΑ	
I <sub>LOADrun</sub>	Maximum load current — Run mode	—	—	120	mA	
I <sub>LOADstby</sub>	Maximum load current — Standby mode	—	—	1	mA	
V <sub>Reg33out</sub>	Regulator output voltage — Input supply (VREGIN) > 3.6 V					
	Run mode	3	3.3	3.6	v	
	Standby mode	2.1	2.8	3.6	v	
V <sub>Reg33out</sub>	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1		3.6	V	2
C <sub>OUT</sub>	External output capacitor	1.76	2.2	8.16	μF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I <sub>LIM</sub>	Short circuit current	_	290		mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25  $^\circ\text{C}$  unless otherwise stated.

2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to ILoad.



Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	4 x t <sub>BUS</sub>	—	ns
DS10	DSPI_SCK input high/low time	(t <sub>SCK</sub> /2) – 2	(t <sub>SCK</sub> /2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	_	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	_	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	14	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven		14	ns





Figure 23. DSPI classic SPI timing — slave mode

## 6.8.7 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	4 x t <sub>BUS</sub>	_	ns	

Table 44. Master mode DSPI timing (full voltage range)

Table continues on the next page...

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Figure 25. DSPI classic SPI timing — slave mode

#### 6.8.8 Inter-Integrated Circuit Interface (I<sup>2</sup>C) timing Table 46. I<sup>2</sup>C timing

Characteristic	Symbol	Standa	rd Mode	Fast	Mode	Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f <sub>SCL</sub>	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t <sub>HD</sub> ; STA	4	_	0.6	_	μs
LOW period of the SCL clock	t <sub>LOW</sub>	4.7		1.3		μs
HIGH period of the SCL clock	t <sub>HIGH</sub>	4	_	0.6	_	μs
Set-up time for a repeated START condition	t <sub>SU</sub> ; STA	4.7	—	0.6	—	μs
Data hold time for I <sub>2</sub> C bus devices	t <sub>HD</sub> ; DAT	0 <sup>1</sup>	3.45 <sup>2</sup>	0 <sup>3</sup>	0.9 <sup>1</sup>	μs
Data set-up time	t <sub>SU</sub> ; DAT	250 <sup>4</sup>		100 <sup>2, 5</sup>		ns
Rise time of SDA and SCL signals	t <sub>r</sub>	—	1000	20 +0.1C <sub>b</sub> <sup>6</sup>	300	ns
Fall time of SDA and SCL signals	t <sub>f</sub>	—	300	20 +0.1C <sub>b</sub> <sup>5</sup>	300	ns
Set-up time for STOP condition	t <sub>SU</sub> ; STO	4		0.6		μs
Bus free time between STOP and START condition	t <sub>BUF</sub>	4.7	_	1.3	_	μs
Pulse width of spikes that must be suppressed by the input filter	t <sub>SP</sub>	N/A	N/A	0	50	ns

1. The master mode I<sup>2</sup>C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.

2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.

- 3. Input signal Slew = 10 ns and Output Load = 50 pF
- 4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
- 5. A Fast mode l<sup>2</sup>C bus device can be used in a Standard mode l2C bus system, but the requirement t<sub>SU; DAT</sub> ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t<sub>rmax</sub> + t<sub>SU; DAT</sub> = 1000 + 250 = 1250 ns (according to the Standard mode l<sup>2</sup>C bus specification) before the SCL line is released.

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6.  $C_b$  = total capacitance of the one bus line in pF.



Figure 26. Timing definition for fast and standard mode devices on the I<sup>2</sup>C bus

# 6.8.9 UART switching specifications

See General switching specifications.

### 6.8.10 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Num	Symbol	Description	Min.	Max.	Unit		
		Operating voltage	1.71	3.6	V		
		Card input clock	•				
SD1	fpp	Clock frequency (low speed)	0	400	kHz		
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz		
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz		
	f <sub>OD</sub>	Clock frequency (identification mode)	0	400	kHz		
SD2	t <sub>WL</sub>	Clock low time	7	—	ns		
SD3	t <sub>WH</sub>	Clock high time	7	—	ns		
SD4	t <sub>TLH</sub>	Clock rise time	—	3	ns		
SD5	t <sub>THL</sub>	Clock fall time	—	3	ns		
		SDHC output / card inputs SDHC_CMD, SDHC_DAT	(reference to	SDHC_CLK)			
SD6	t <sub>OD</sub>	SDHC output delay (output valid)	-5	8.3	ns		
	SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)						
SD7	t <sub>ISU</sub>	SDHC input setup time	5	_	ns		
SD8	t <sub>IH</sub>	SDHC input hold time	0	_	ns		

Table 47. SDHC switching specifications



# Table 48. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (limited voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	_	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	15	_	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns



#### Figure 28. I2S/SAI timing — master modes

# Table 49. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	4.5	_	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid <ul> <li>Multiple SAI Synchronous mode</li> </ul>	_	21	ns
	All other modes	—	15	

Table continues on the next page...







## 6.9 Human-machine interfaces (HMI)

## 6.9.1 TSI electrical specifications

Table 54. TSI electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>DDTSI</sub>	Operating voltage	1.71	—	3.6	V	
C <sub>ELE</sub>	Target electrode capacitance range	1	20	500	pF	1
f <sub>REFmax</sub>	Reference oscillator frequency	_	8	15	MHz	2, 3
f <sub>ELEmax</sub>	Electrode oscillator frequency	_	1	1.8	MHz	2, 4
C <sub>REF</sub>	Internal reference capacitor	_	1	—	pF	
V <sub>DELTA</sub>	Oscillator delta voltage	_	500	—	mV	2, 5
I <sub>REF</sub>	Reference oscillator current source base current • 2 μA setting (REFCHRG = 0)	_	2	3	μA	2, 6
	<ul> <li>32 µA setting (REFCHRG = 15)</li> </ul>	_	36	50		
I <sub>ELE</sub>	Electrode oscillator current source base current • 2 μA setting (EXTCHRG = 0)	_	2	3	μA	2, 7
	<ul> <li>32 µA setting (EXTCHRG = 15)</li> </ul>	—	36	50		
Pres5	Electrode capacitance measurement precision	_	8.3333	38400	fF/count	8
Pres20	Electrode capacitance measurement precision	_	8.3333	38400	fF/count	9
Pres100	Electrode capacitance measurement precision	_	8.3333	38400	fF/count	10
MaxSens	Maximum sensitivity	0.008	1.46	_	fF/count	11
Res	Resolution	_	_	16	bits	
T <sub>Con20</sub>	Response time @ 20 pF	8	15	25	μs	12
I <sub>TSI_RUN</sub>	Current added in run mode		55	—	μΑ	
I <sub>TSI_LP</sub>	Low power mode current adder	_	1.3	2.5	μΑ	13

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100 LQFP	Pin Name	Default	ALTO	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
	CMP0_IN5/ ADC1_SE18	CMP0_IN5/ ADC1_SE18	CMP0_IN5/ ADC1_SE18								
27	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
28	XTAL32	XTAL32	XTAL32								
29	EXTAL32	EXTAL32	EXTAL32								
30	VBAT	VBAT	VBAT								
31	PTE24	ADC0_SE17	ADC0_SE17	PTE24	CAN1_TX	UART4_TX			EWM_OUT_b		
32	PTE25	ADC0_SE18	ADC0_SE18	PTE25	CAN1_RX	UART4_RX			EWM_IN		
33	PTE26	DISABLED		PTE26	ENET_1588_ CLKIN	UART4_CTS_b			RTC_CLKOUT	USB_CLKIN	
34	PTAO	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTA0	UART0_CTS_ b/ UART0_COL_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
35	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
36	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
37	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UART0_RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
38	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
39	PTA5	DISABLED		PTA5	USB_CLKIN	FTM0_CH2	RMII0_RXER/ MII0_RXER	CMP2_OUT	I2S0_TX_BCLK	JTAG_TRST_b	
40	VDD	VDD	VDD								
41	VSS	VSS	VSS								
42	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0	rmiio_rxd1/ Miio_rxd1		I2S0_TXD0	FTM1_QD_ PHA	
43	PTA13/ LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1	RMII0_RXD0/ MII0_RXD0		I2S0_TX_FS	FTM1_QD_ PHB	
44	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX	RMII0_CRS_ DV/ MII0_RXDV		I2S0_RX_BCLK	12S0_TXD1	
45	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX	RMII0_TXEN/ MII0_TXEN		I2S0_RXD0		
46	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_CTS_ b/ UART0_COL_b	RMII0_TXD0/ MII0_TXD0		12S0_RX_FS	12S0_RXD1	
47	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_b	RMII0_TXD1/ MII0_TXD1		I2S0_MCLK		
48	VDD	VDD	VDD								
49	VSS	VSS	VSS								
50	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
51	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1		
52	RESET_b	RESET_b	RESET_b								



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