# E·XFL

### NXP USA Inc. - MK60DN512VLL10 Datasheet



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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I <sup>2</sup> S, LVD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 33x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk60dn512vll10

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





# 1 Ordering parts

# 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK60 and MK60.

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

# 2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

# 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> </ul>
K##	Kinetis family	• K60
A	Key attribute	<ul> <li>D = Cortex-M4 w/ DSP</li> <li>F = Cortex-M4 w/ DSP and FPU</li> </ul>
М	Flash memory type	<ul> <li>N = Program flash only</li> <li>X = Program flash and FlexMemory</li> </ul>





### 3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	0.9	1.1	V

# 3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

### 3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I <sub>WP</sub>	Digital I/O weak pullup/ pulldown current	10	130	μA

# 3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

### 3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF



Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	Digital supply voltage	-0.3	3.8	V
I <sub>DD</sub>	Digital supply current	—	185	mA
V <sub>DIO</sub>	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	5.5	V
V <sub>AIO</sub>	Analog <sup>1</sup> , RESET, EXTAL, and XTAL input voltage	-0.3	V <sub>DD</sub> + 0.3	V
۱ <sub>D</sub>	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V <sub>DDA</sub>	Analog supply voltage	V <sub>DD</sub> – 0.3	V <sub>DD</sub> + 0.3	V
$V_{USB_{DP}}$	USB_DP input voltage	-0.3	3.63	V
$V_{USB_{DM}}$	USB_DM input voltage	-0.3	3.63	V
VREGIN	USB regulator input	-0.3	6.0	V
V <sub>BAT</sub>	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

# 5 General

### 5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is  $V_{IL}$  +  $(V_{IH} - V_{IL})/2$ .

### Figure 1. Input signal measurement reference

All digital I/O switching characteristics assume:

- 1. output pins
  - have C<sub>L</sub>=30pF loads,
  - are configured for fast slew rate (PORTx\_PCRn[SRE]=0), and
  - are configured for high drive strength (PORTx\_PCRn[DSE]=1)
- 2. input pins
  - have their passive filter disabled (PORTx\_PCRn[PFE]=0)



General



Figure 2. Run mode supply current vs. core frequency

# 5.2.6 EMC radiated emissions operating behaviors

# Table 7. EMC radiated emissions operating behaviors for 144LQFP and144MAPBGA

Symbol	Description	Frequency band (MHz)	144LQFP	144MAPBGA	Unit	Notes
V <sub>RE1</sub>	Radiated emissions voltage, band 1	0.15–50	23	12	dBµV	1, 2
V <sub>RE2</sub>	Radiated emissions voltage, band 2	50–150	27	24	dBµV	
V <sub>RE3</sub>	Radiated emissions voltage, band 3	150–500	28	27	dBµV	
V <sub>RE4</sub>	Radiated emissions voltage, band 4	500–1000	14	11	dBµV	
V <sub>RE_IEC</sub>	IEC level	0.15–1000	К	К	_	2, 3

 Determined according to IEC Standard 61967-1, Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions and IEC Standard 61967-2, Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions – TEM Cell and Wideband TEM Cell Method. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

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Board type	Symbol	Description	100 LQFP	Unit	Notes
Single-layer (1s)	R <sub>θJMA</sub>	Thermal resistance, junction to ambient (200 ft./ min. air speed)	37	°C/W	1
Four-layer (2s2p)	R <sub>θJMA</sub>	Thermal resistance, junction to ambient (200 ft./ min. air speed)	29	°C/W	1
_	R <sub>eJB</sub>	Thermal resistance, junction to board	20	°C/W	2
_	R <sub>θJC</sub>	Thermal resistance, junction to case	9	°C/W	3
	Ψ <sub>JT</sub>	Thermal characterization parameter, junction to package top outside center (natural convection)	2	°C/W	4

- 1. Determined according to JEDEC Standard JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air), or EIA/JEDEC Standard JESD51-6, Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air).
- 2. Determined according to JEDEC Standard JESD51-8, Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board.
- 3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
- 4. Determined according to JEDEC Standard JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air).

# 6 Peripheral operating requirements and behaviors

### 6.1 Core modules

### 6.1.1 Debug trace timing specifications

 Table 12.
 Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T <sub>cyc</sub>	Clock period	Frequency	MHz	
T <sub>wl</sub>	Low pulse width	2	_	ns
T <sub>wh</sub>	High pulse width	2	_	ns
T <sub>r</sub>	Clock and data rise time		3	ns

Table continues on the next page...

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Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>DD</sub>	Supply voltage	1.71	_	3.6	V	
I <sub>DDOSC</sub>	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	_	nA	
	• 4 MHz	—	200	_	μA	
	• 8 MHz (RANGE=01)	—	300	_	μA	
	• 16 MHz	—	950	_	μA	
	• 24 MHz	—	1.2	_	mA	
	• 32 MHz	—	1.5	_	mA	
IDDOSC	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	_	μA	
	• 4 MHz	—	400	_	μA	
	• 8 MHz (RANGE=01)	—	500	_	μA	
	• 16 MHz	—	2.5	_	mA	
	• 24 MHz	—	3	_	mA	
	• 32 MHz	—	4	_	mA	
C <sub>x</sub>	EXTAL load capacitance	_	_	_		2, 3
Cy	XTAL load capacitance	_		_		2, 3
R <sub>F</sub>	Feedback resistor — low-frequency, low-power mode (HGO=0)	_	_	_	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	_	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	_			MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	_	1		MΩ	-
R <sub>S</sub>	Series resistor — low-frequency, low-power mode (HGO=0)	_			kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	_	200		kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	_			kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
		_	0	_	kΩ	

### 6.3.2.1 Oscillator DC electrical specifications Table 16. Oscillator DC electrical specifications



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>pp</sub> <sup>5</sup>	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	_	0.6		V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	_	V <sub>DD</sub>	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	_	0.6		V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)		V <sub>DD</sub>		V	

### Table 16. Oscillator DC electrical specifications (continued)

- 1. V<sub>DD</sub>=3.3 V, Temperature =25 °C
- 2. See crystal or resonator manufacturer's recommendation
- 3. C<sub>x</sub>,C<sub>y</sub> can be provided by using either the integrated capacitors or by using external components.
- 4. When low power mode is selected, R<sub>F</sub> is integrated and must not be attached externally.
- 5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

# 6.3.2.2 Oscillator frequency specifications

### Table 17. Oscillator frequency specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f <sub>osc_lo</sub>	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	_	40	kHz	
f <sub>osc_hi_1</sub>	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	_	8	MHz	
f <sub>osc_hi_2</sub>	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	_	32	MHz	
f <sub>ec_extal</sub>	Input clock frequency (external clock mode)	—		50	MHz	1, 2
t <sub>dc_extal</sub>	Input clock duty cycle (external clock mode)	40	50	60	%	
t <sub>cst</sub>	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	_	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	_	250	_	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	_	0.6	_	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	_	1	_	ms	

- 1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
- 2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
- 3. Proper PC board layout procedures must be followed to achieve specifications.

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### 6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the flash memory module to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

 $Writes\_subsystem = \frac{EEPROM - 2 \times EEESPLIT \times EEESIZE}{EEESPLIT \times EEESIZE} \times Write\_efficiency \times n_{nvmcycd}$ 

where

- Writes\_subsystem minimum number of writes to each FlexRAM location for subsystem (each subsystem can have different endurance)
- EEPROM allocated FlexNVM for each EEPROM subsystem based on DEPART; entered with the Program Partition command
- EEESPLIT FlexRAM split factor for subsystem; entered with the Program Partition command
- EEESIZE allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write\_efficiency
  - 0.25 for 8-bit writes to FlexRAM
  - 0.50 for 16-bit or 32-bit writes to FlexRAM
- n<sub>nvmcycd</sub> data flash cycling endurance (the following graph assumes 10,000 cycles)



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Figure 9. EEPROM backup writes to FlexRAM

## 6.4.2 EzPort switching specifications

Table 24. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	f <sub>SYS</sub> /2	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	f <sub>SYS</sub> /8	MHz
EP2	EZP_CS negation to next EZP_CS assertion	2 x t <sub>EZP_CK</sub>	—	ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5		ns
EP4	EZP_CK high to EZP_CS input invalid (hold)	5		ns
EP5	EZP_D input valid to EZP_CK high (setup)	2		ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	16	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	EZP_CS negation to EZP_Q tri-state	—	12	ns



### 6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 27 and Table 28 are achievable on the differential pins ADCx\_DP0, ADCx\_DM0, ADCx\_DP1, ADCx\_DM1, ADCx\_DP3, and ADCx\_DM3.

The ADCx\_DP2 and ADCx\_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in Table 29 and Table 30.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	Absolute	1.71	—	3.6	V	
$\Delta V_{DDA}$	Supply voltage	Delta to V <sub>DD</sub> (V <sub>DD</sub> – V <sub>DDA</sub> )	-100	0	+100	mV	2
$\Delta V_{SSA}$	Ground voltage	Delta to V <sub>SS</sub> (V <sub>SS</sub> – V <sub>SSA</sub> )	-100	0	+100	mV	2
V <sub>REFH</sub>	ADC reference voltage high		1.13	V <sub>DDA</sub>	V <sub>DDA</sub>	V	
V <sub>REFL</sub>	ADC reference voltage low		V <sub>SSA</sub>	V <sub>SSA</sub>	V <sub>SSA</sub>	V	
V <sub>ADIN</sub>	Input voltage	16-bit differential mode	VREFL	_	31/32 * VREFH	V	
		All other modes	VREFL	—	VREFH		
C <sub>ADIN</sub>	Input capacitance	16-bit mode	—	8	10	pF	
		<ul> <li>8-bit / 10-bit / 12-bit modes</li> </ul>	_	4	5		
R <sub>ADIN</sub>	Input resistance		—	2	5	kΩ	
R <sub>AS</sub>	Analog source resistance	13-bit / 12-bit modes f <sub>ADCK</sub> < 4 MHz	_	_	5	kΩ	3
f <sub>ADCK</sub>	ADC conversion clock frequency	≤ 13-bit mode	1.0	_	18.0	MHz	4
f <sub>ADCK</sub>	ADC conversion clock frequency	16-bit mode	2.0	_	12.0	MHz	4
C <sub>rate</sub>	ADC conversion	≤ 13-bit modes					5
	rate	No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	_	818.330	Ksps	

### 6.6.1.1 16-bit ADC operating conditions Table 27. 16-bit ADC operating conditions

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Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
C <sub>rate</sub>	ADC conversion	16-bit mode					5
	rate	No ADC hardware averaging	37.037	_	461.467	Ksps	
		Continuous conversions enabled, subsequent conversion time					

 Table 27.
 16-bit ADC operating conditions (continued)

- 1. Typical values assume  $V_{DDA}$  = 3.0 V, Temp = 25 °C,  $f_{ADCK}$  = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
- 2. DC potential difference.
- 3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8  $\Omega$  analog source resistance. The R<sub>AS</sub>/C<sub>AS</sub> time constant should be kept to < 1 ns.
- 4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
- 5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.



Figure 13. ADC input impedance equivalency diagram

### 6.6.1.2 16-bit ADC electrical characteristics Table 28. 16-bit ADC characteristics (V<sub>REFH</sub> = V<sub>DDA</sub>, V<sub>REFL</sub> = V<sub>SSA</sub>)

Symbol	Description	Conditions <sup>1</sup> .	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
I <sub>DDA_ADC</sub>	Supply current		0.215		1.7	mA	3



Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
SFDR	Spurious free dynamic range	• Gain=1 • Gain=64	85 53	105 88		dB dB	16-bit differential mode, Average=32, f <sub>in</sub> =100Hz
ENOB	Effective number	Gain=1. Average=4	11.6	13.4		bits	16-bit
	of bits	Gain=1, Average=8	8.0	13.6	—	bits	differential
		• Gain=64, Average=4	7.2	9.6	—	bits	
		Gain=64, Average=8	6.3	9.6	—	bits	
		• Gain=1, Average=32	12.8	14.5	—	bits	
		Gain=2, Average=32	11.0	14.3	—	bits	
		• Gain=4, Average=32	7.9	13.8	—	bits	
		Gain=8, Average=32	7.3	13.1	—	bits	
		Gain=16, Average=32	6.8	12.5	—	bits	
		• Gain=32, Average=32	6.8	11.5	—	bits	
		• Gain=64, Average=32	7.5	10.6	—	bits	
SINAD	Signal-to-noise plus distortion ratio	See ENOB	6.02	× ENOB +	1.76	dB	

### Table 30. 16-bit ADC with PGA characteristics (continued)

- 1. Typical values assume  $V_{DDA}$  =3.0V, Temp=25°C,  $f_{ADCK}$ =6MHz unless otherwise stated.
- 2. This current is a PGA module adder, in addition to ADC conversion currents.
- Between IN+ and IN-. The PGA draws a DC current from the input terminals. The magnitude of the DC current is a strong function of input common mode voltage (V<sub>CM</sub>) and the PGA gain.
- 4. Gain =  $2^{PGAG}$
- 5. After changing the PGA gain setting, a minimum of 2 ADC+PGA conversions should be ignored.
- 6. Limit the input signal swing so that the PGA does not saturate during operation. Input signal swing is dependent on the PGA reference voltage and gain setting.

### 6.6.2 CMP and 6-bit DAC electrical specifications Table 31. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
V <sub>DD</sub>	Supply voltage	1.71	—	3.6	V
I <sub>DDHS</sub>	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μA
I <sub>DDLS</sub>	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μA
V <sub>AIN</sub>	Analog input voltage	V <sub>SS</sub> – 0.3	_	V <sub>DD</sub>	V
V <sub>AIO</sub>	Analog input offset voltage	—	—	20	mV



Peripheral operating requirements and behaviors



Figure 17. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=1)

### 6.6.3 12-bit DAC electrical characteristics

### 6.6.3.1 12-bit DAC operating requirements Table 32. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	1.71	3.6	V	
V <sub>DACR</sub>	Reference voltage	1.13	3.6	V	1
T <sub>A</sub>	Temperature	Operating t range of t	emperature he device	°C	
CL	Output load capacitance	— 100		pF	2
١L	Output load current		1	mA	

1. The DAC reference can be selected to be V<sub>DDA</sub> or the voltage output of the VREF module (VREF\_OUT)

2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

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### 6.6.3.2 12-bit DAC operating behaviors Table 33. 12-bit DAC operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I <sub>DDA_DACL</sub>	Supply current — low-power mode	_	—	330	μΑ	
I <sub>DDA_DACH</sub> P	Supply current — high-speed mode	_	—	1200	μΑ	
tDACLP	Full-scale settling time (0x080 to 0xF7F) — low-power mode	_	100	200	μs	1
t <sub>DACHP</sub>	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
t <sub>CCDACLP</sub>	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	_	0.7	1	μs	1
V <sub>dacoutl</sub>	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
V <sub>dacouth</sub>	DAC output voltage range high — high- speed mode, no load, DAC set to 0xFFF	V <sub>DACR</sub> -100	—	V <sub>DACR</sub>	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V <sub>DACR</sub> > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V <sub>DACR</sub> = VREF_OUT	—	—	±1	LSB	4
V <sub>OFFSET</sub>	Offset error	_	±0.4	±0.8	%FSR	5
E <sub>G</sub>	Gain error	_	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} > = 2.4 \text{ V}$	60	—	90	dB	
T <sub>CO</sub>	Temperature coefficient offset voltage	_	3.7	_	μV/C	6
T <sub>GE</sub>	Temperature coefficient gain error	_	0.000421		%FSR/C	
Rop	Output resistance load = $3 \text{ k}\Omega$	_	—	250	Ω	
SR	Slew rate -80h $\rightarrow$ F7Fh $\rightarrow$ 80h				V/µs	
	<ul> <li>High power (SP<sub>HP</sub>)</li> </ul>	1.2	1.7	_		
	Low power (SP <sub>LP</sub> )	0.05	0.12	—		
СТ	Channel to channel cross talk	_	—	-80	dB	
BW	3dB bandwidth				kHz	
	<ul> <li>High power (SP<sub>HP</sub>)</li> </ul>	550	_	_		
	Low power (SP <sub>LP</sub> )	40	_	—		

1. Settling within ±1 LSB

- 2. The INL is measured for 0+100mV to  $V_{DACR}$ -100 mV
- 3. The DNL is measured for 0+100 mV to  $V_{\text{DACR}}\text{--}100 \text{ mV}$
- 4. The DNL is measured for 0+100mV to  $V_{DACR}\mbox{--}100$  mV with  $V_{DDA}\mbox{-}2.4V$
- 5. Calculated by a best fit curve from  $V_{SS}\text{+}100\mbox{ mV}$  to  $V_{DACR}\text{-}100\mbox{ mV}$
- 6. VDDA = 3.0V, reference select set for VDDA (DACx\_CO:DACRFS = 1), high power mode(DACx\_CO:LPEN = 0), DAC set to 0x800, Temp range from -40C to 105C



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>out</sub>	Voltage reference output with factory trim at nominal $V_{\text{DDA}}$ and temperature=25C	1.1915	1.195	1.1977	V	
V <sub>out</sub>	Voltage reference output — factory trim	1.1584	—	1.2376	V	
V <sub>out</sub>	Voltage reference output — user trim	1.193	—	1.197	V	
V <sub>step</sub>	Voltage reference trim step	—	0.5	—	mV	
V <sub>tdrift</sub>	Temperature drift (Vmax -Vmin across the full temperature range)		_	80	mV	
I <sub>bg</sub>	Bandgap only current	—	—	80	μA	1
I <sub>lp</sub>	Low-power buffer current	—	—	360	uA	1
I <sub>hp</sub>	High-power buffer current	—	—	1	mA	1
$\Delta V_{LOAD}$	Load regulation				μV	1, 2
	• current = ± 1.0 mA	_	200	_		
T <sub>stup</sub>	Buffer startup time	_	—	100	μs	
V <sub>vdrift</sub>	Voltage drift (Vmax -Vmin across the full voltage range)	_	2	_	mV	1

Table 35. VREF full-range operating behaviors

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.

2. Load regulation voltage is the difference between the VREF\_OUT voltage with no load vs. voltage with defined load

### Table 36. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>A</sub>	Temperature	0	50	°C	

### Table 37. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>out</sub>	Voltage reference output with factory trim	1.173	1.225	V	

### 6.7 Timers

See General switching specifications.

# 6.8 Communication interfaces



### 6.8.5 CAN switching specifications

See General switching specifications.

### 6.8.6 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation		25	MHz	
DS1	DSPI_SCK output cycle time	2 x t <sub>BUS</sub>	—	ns	
DS2	DSPI_SCK output high/low time	(t <sub>SCK</sub> /2) – 2	$(t_{SCK}/2) + 2$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	(t <sub>BUS</sub> x 2) – 2	_	ns	1
DS4	DSPI_SCK to DSPI_PCSn invalid delay	(t <sub>BUS</sub> x 2) – 2	_	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	_	8	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	0	_	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	14		ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

 Table 42.
 Master mode DSPI timing (limited voltage range)

1. The delay is programmable in SPIx\_CTARn[PSSCK] and SPIx\_CTARn[CSSCK].

2. The delay is programmable in SPIx\_CTARn[PASC] and SPIx\_CTARn[ASC].







Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	4 x t <sub>BUS</sub>	—	ns
DS10	DSPI_SCK input high/low time	(t <sub>SCK</sub> /2) – 2	(t <sub>SCK</sub> /2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	_	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	_	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	14	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven		14	ns





Figure 23. DSPI classic SPI timing — slave mode

### 6.8.7 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	4 x t <sub>BUS</sub>	_	ns	

Table 44. Master mode DSPI timing (full voltage range)

Table continues on the next page...

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Num	Description	Min.	Max.	Unit	Notes
DS2	DSPI_SCK output high/low time	(t <sub>SCK</sub> /2) - 4	(t <sub>SCK/2)</sub> + 4	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	(t <sub>BUS</sub> x 2) – 4	_	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	(t <sub>BUS</sub> x 2) – 4	_	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-1.2	_	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	19.1	_	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0		ns	

Table 44. Master mode DSPI timing (full voltage range) (continued)

- 1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
- 2. The delay is programmable in SPIx\_CTARn[PSSCK] and SPIx\_CTARn[CSSCK].
- 3. The delay is programmable in SPIx\_CTARn[PASC] and SPIx\_CTARn[ASC].



### Figure 24. DSPI classic SPI timing — master mode

### Table 45. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation		6.25	MHz
DS9	DSPI_SCK input cycle time	8 x t <sub>BUS</sub>		ns
DS10	DSPI_SCK input high/low time	(t <sub>SCK</sub> /2) - 4	(t <sub>SCK/2)</sub> + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid		24	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2		ns
DS14	DSPI_SCK to DSPI_SIN input hold	7		ns
DS15	DSPI_SS active to DSPI_SOUT driven		19	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven		19	ns



# Table 48. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (limited voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	_	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	15	_	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns



### Figure 28. I2S/SAI timing — master modes

# Table 49. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	4.5	_	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid <ul> <li>Multiple SAI Synchronous mode</li> </ul>	_	21	ns
	All other modes	—	15	



- 1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
- 2. Fixed external capacitance of 20 pF.
- 3. REFCHRG = 2, EXTCHRG=0.
- 4. REFCHRG = 0, EXTCHRG = 10.
- 5.  $V_{DD} = 3.0 V.$
- 6. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
- 7. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
- 8. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; lext = 16.
- 9. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; lext = 16.
- 10. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; lext = 16.
- 11. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes. Sensitivity depends on the configuration used. The documented values are provided as examples calculated for a specific configuration of operating conditions using the following equation: (C<sub>ref</sub> \* I<sub>ext</sub>)/(I<sub>ref</sub> \* PS \* NSCN)

The typical value is calculated with the following configuration:

I<sub>ext</sub> = 6 μA (EXTCHRG = 2), PS = 128, NSCN = 2, I<sub>ref</sub> = 16 μA (REFCHRG = 7), C<sub>ref</sub> = 1.0 pF

The minimum value is calculated with the following configuration:

I<sub>ext</sub> = 2 μA (EXTCHRG = 0), PS = 128, NSCN = 32, I<sub>ref</sub> = 32 μA (REFCHRG = 15), C<sub>ref</sub> = 0.5 pF

The highest possible sensitivity is the minimum value because it represents the smallest possible capacitance that can be measured by a single count.

- 12. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, EXTCHRG = 7.
- 13. REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

# 7 Dimensions

### 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
100-pin LQFP	98ASS23308W
104-pin MAPBGA	98ASA00344D

# 8 Pinout