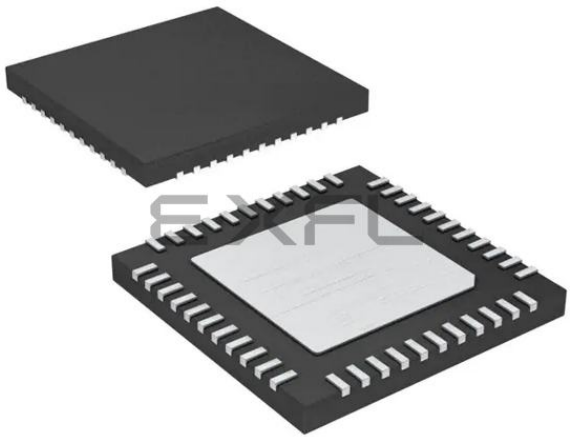

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 28x10b; D/A 4x5b, 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1777-e-ml

TABLE 1-3: PIC16(L)F1777/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA5/AN4/OPA1IN0-/ DAC2OUT1/PRG1F/ MD1MOD/$\overline{SS}$	RA5	TTL/ST	CMOS	General purpose I/O.
	AN4	AN	—	ADC Channel 4 input.
	OPA1IN0-	AN	—	Operational amplifier 1 inverting input.
	DAC2OUT1	—	AN	DAC2 voltage output.
	PRG1F(1)	TTL/ST	—	Ramp generator set_falling input.
	MD1MOD(1)	TTL/ST	—	Data signal modulator modulation input.
	$\overline{SS}$	ST	—	Slave Select input.
RA6/CLKOUT/C6IN1+/OSC2	RA6	TTL/ST	CMOS	General purpose I/O.
	CLKOUT	—	CMOS	FOSC/4 output.
	C6IN1+	AN	—	Comparator 6 positive input.
	OSC2	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
RA7/CLKIN/OSC1	RA7	TTL/ST	CMOS	General purpose I/O.
	CLKIN	TTL/ST	—	CLC input.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
RB0/AN12/ZCD/HIB0/C2IN1+/ CCP8/COG1IN/MD4CL/ INT	RB0	TTL/ST	CMOS	General purpose I/O.
	AN12	AN	—	ADC Channel 12 input.
	ZCD	AN	—	Zero-cross detection input.
	HIB0	HP	HP	High-Power output.
	C2IN1+	AN	—	Comparator 2 positive input.
	CCP8(1)	TTL/ST	—	CCP8 capture input.
	COG1IN(1)	TTL/ST	—	Complementary output generator 1 input.
	MD4CL(1)	TTL/ST	—	Data signal modulator 4 low carrier input.
	INT	TTL/ST	—	External interrupt.
RB1/AN10/PRG1IN1/PRG2IN0/ PRG4R/HIB1/C1IN3-/C2IN3-/ C3IN3-/C4IN3-/OPA2OUT/ OPA1IN1+/OPA1IN1-/COG2IN/ MD4CH	RB1	TTL/ST	CMOS	General purpose I/O.
	AN10	AN	—	ADC Channel 10 input.
	PRG1IN1	AN	—	Ramp generator 1 reference voltage input.
	PRG2IN0	AN	—	Ramp generator 2 reference voltage input.
	PRG4R(1)	TTL/ST	—	Ramp generator set_rising input.
	HIB1	HP	HP	High-Power output.
	C1IN3-	AN	—	Comparator 1 negative input.
	C2IN3-	AN	—	Comparator 2 negative input.
	C3IN3-	AN	—	Comparator 3 negative input.
	C4IN3-	AN	—	Comparator 4 negative input.
	OPA2OUT	—	AN	Operational amplifier 2 output.
	OPA1IN1+	AN	—	Operational amplifier 1 non-inverting input.
	OPA1IN1-	AN	—	Operational amplifier 1 inverting input.
	COG2IN(1)	TTL/ST	—	Complementary output generator 2 input.
	MD4CH(1)	TTL/ST	—	Data signal modulator 4 high carrier input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HP = High Power XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.
2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F1777/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RE1/AN6/DAC6OUT1/ DAC6REF1-/DAC8REF1-	RE1	TTL/ST	CMOS	General purpose I/O.
	AN6	AN	—	ADC Channel 6 input.
	DAC6OUT1	—	AN	DAC6 voltage output.
	DAC6REF1-	AN	—	DAC6 negative reference.
	DAC8REF1-	AN	—	DAC8 negative reference.
RE2/AN7/DAC8OUT1	RE2	TTL/ST	CMOS	General purpose I/O.
	AN7	AN	—	ADC Channel 7 input.
	DAC8OUT1	—	AN	DAC8 voltage output.
RE3/$\overline{MCLR}$/V_{PP}	RE3	TTL/ST	CMOS	General purpose input.
	$\overline{MCLR}$	ST	—	Master clear input.
V_{DD}	V_{DD}	Power	—	Positive supply.
V_{SS}	V_{SS}	Power	—	Ground reference.
OUT(2)	C1OUT		CMOS	Comparator 1 output.
	C2OUT		CMOS	Comparator 2 output.
	C3OUT		CMOS	Comparator 3 output.
	C4OUT		CMOS	Comparator 4 output.
	C5OUT		CMOS	Comparator 5 output.
	C6OUT		CMOS	Comparator 6 output.
	C7OUT		CMOS	Comparator 7 output.
	C8OUT		CMOS	Comparator 8 output.
	CCP1		CMOS	Compare/PWM1 output.
	CCP2		CMOS	Compare/PWM2 output.
	CCP7		CMOS	Compare/PWM7 output.
	CCP8		CMOS	Compare/PWM8 output.
	MD1OUT		CMOS	Data signal modulator 1 output.
	MD2OUT		CMOS	Data signal modulator 2 output.
	MD3OUT		CMOS	Data signal modulator 3 output.
	MD4OUT		CMOS	Data signal modulator 4 output.
	PWM3OUT		CMOS	PWM3 output.
	PWM4OUT		CMOS	PWM4 output.
	PWM5OUT		CMOS	PWM5 output.
	PWM6OUT		CMOS	PWM6 output.
	PWM9OUT		CMOS	PWM9 output.
	PWM10OUT		CMOS	PWM10 output.
	PWM11OUT		CMOS	PWM11 output.
	PWM12OUT		CMOS	PWM12 output.
	COG1A		CMOS	Complementary output generator 1 output A.
	COG1B		CMOS	Complementary output generator 1 output B.
	COG1C		CMOS	Complementary output generator 1 output C.
	COG1D		CMOS	Complementary output generator 1 output D.
	COG2A		CMOS	Complementary output generator 2 output A.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HP = High Power XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-4: PERIPHERAL CONNECTION MATRIX

	Peripheral Input																							
Peripheral Output	**ADC Trigger**	**COG Clock**	**COG Rising/Falling**	**COG Shutdown**	**10-bit DAC**	**5-bit DAC**	**PRG Analog Input**	**PRG Rising/Falling**	**Comparator +**	**Comparator -**	**CLC**	**DSM CH**	**DSM CL**	**DSM Mod**	**Op Amp +**	**Op Amp -**	**Op Amp Override**	**10-bit PWM**	**16-bit PWM**	**CCP Capture**	**CCP Clock**	**Timer2/4/6/8 Clock**	**Timer2/4/6/8 Reset**	**Timer1/3/5 Gate**	**Timer0 Clock**
FVR					●	●	●		●	●					●	●									
ZCD											●						●					●			
PRG									●						●	●									
10-bit DAC							●		●						●	●									
5-bit DAC							●		●						●	●									
CCP	●		●					●			●	●	●	●			●						●		
Comparator (sync)	●							●			●						●			●			●	●	
Comparator (async)			●	●										●											
CLC	●		●	●							●	●	●	●			●			●		●	●		
DSM																									
COG																	●								
EUSART TX/CK											●			●											
EUSART DT											●			●											
MSSP SCK/SCL											●			●											
MSSP SDO/SDA											●			●											
Op Amp							●																		
10-bit PWM	●		●					●			●	●	●	●			●						●		
16-bit PWM	●		●					●			●	●	●	●			●						●		
Timer0 overflow	●										●													●	
Timer2 = T2PR				●							●							●			●		●		
Timer4 = T4PR				●							●							●			●		●		
Timer6 = T6PR				●							●							●			●		●		
Timer8 = T8PR				●							●							●			●		●		
Timer2 Postscale	●			●							●							●			●		●		
Timer4 Postscale	●			●							●							●			●		●		
Timer6 Postscale	●			●							●							●			●		●		
Timer8 Postscale	●			●							●							●			●		●		
Timer1 overflow	●										●							●			●				
Timer3 overflow	●										●							●			●				
Timer5 overflow	●										●							●			●				
SOSC																			●			●			
FOSC/4		●																				●			
FOSC		●									●	●	●						●			●			
HFINTOSC		●									●	●	●						●			●			
LFINTOSC											●								●			●			
MFINTOSC																						●			
IOCIF											●									●	●				
PPS Input pin			●	●				●				●	●	●						●	●	●	●	●	●

TABLE 3-12: PIC16(L)F1777 MEMORY MAP, BANK 24-31

BANK 24		BANK 25		BANK 26		BANK 27		BANK 28		BANK 29		BANK 30		BANK 31	
C00h	Core Registers (Table 3-2)	C80h	Core Registers (Table 3-2)	D00h	Core Registers (Table 3-2)	D80h	Core Registers (Table 3-2)	E00h	Core Registers (Table 3-2)	E80h	Core Registers (Table 3-2)	F00h	Core Registers (Table 3-2)	F80h	Core Registers (Table 3-2)
C0Bh		C8Bh		D0Bh		D8Bh		E0Bh		E8Bh		F0Bh		F8Bh	
C0Ch	—	C8Ch	—	D0Ch	—										
C0Dh	—	C8Dh	—	D0Dh	—										
C0Eh	—	C8Eh	—	D0Eh	—										
C0Fh	—	C8Fh	—	D0Fh	—										
C10h	—	C90h	—	D10h	—										
C11h	—	C91h	—	D11h	—										
C12h	—	C92h	—	D12h	—										
C13h	—	C93h	—	D13h	—										
C14h	—	C94h	—	D14h	—										
C15h	—	C95h	—	D15h	—										
C16h	—	C96h	—	D16h	—										
C17h	—	C97h	—	D17h	—										
C18h	—	C98h	—	D18h	—										
C19h	—	C99h	—	D19h	—										
C1Ah	—	C9Ah	—	D1Ah	—										
C1Bh	—	C9Bh	—	D1Bh	MD4CON0										
C1Ch	—	C9Ch	—	D1Ch	MD4CON1										
C1Dh	—	C9Dh	—	D1Dh	MD4SRC										
C1Eh	—	C9Eh	—	D1Eh	MD4CARL										
C1Fh	—	C9Fh	—	D1Fh	MD4CARH										
C20h	Unimplemented Read as '0'	CA0h	Unimplemented Read as '0'	D20h	Unimplemented Read as '0'										
C6Fh		CEFh		D6Fh		DEFh		E6Fh		EEFh		F6Fh		FEFh	
C70h	Accesses 70h – 7Fh	CF0h	Accesses 70h – 7Fh	D70h	Accesses 70h – 7Fh	DF0h	Accesses 70h – 7Fh	E70h	Accesses 70h – 7Fh	EF0h	Accesses 70h – 7Fh	F70h	Accesses 70h – 7Fh	FF0h	Accesses 70h – 7Fh
CFFh		CFFh		D7Fh		DFFh		E7Fh		EFFh		F7Fh		FFFh	
							See Table 3-15 for register mapping details		See Table 3-15 for register mapping details		See Table 3-15 for register mapping details		See Table 3-15 for register mapping details		See Table 3-16 for register mapping details

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 9											
48Ch to 48Dh	—	Unimplemented								—	—
48Eh	ADRESL	ADC Result Register Low								xxxx xxxx	uuuu uuuu
48Fh	ADRESH	ADC Result Register High								xxxx xxxx	uuuu uuuu
490h	ADCON0	CHS<5:0>						GO/$\overline{\text{DONE}}$	ADON	0000 0000	0000 0000
491h	ADCON1	ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>		0000 -000	0000 -000
492h	ADCON2	—	—	TRIGSEL<5:0>						--00 0000	--00 0000
493h	T2TMR	Holding Register for the 8-bit TMR2 Register								0000 0000	0000 0000
494h	T2PR	TMR2 Period Register								1111 1111	1111 1111
495h	T2CON	ON	CKPS<2:0>			OUTPS<3:0>				0000 0000	0000 0000
496h	T2HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					0000 0000	0000 0000
497h	T2CLKCON	—	—	—	—	CS<3:0>				---- 0000	---- 0000
498h	T2RST	—	—	—	RSEL<4:0>					---0 0000	---0 0000
499h	—	Unimplemented								—	—
49Ah	T8TMR	Holding Register for the 8-bit TMR8 Register								0000 0000	0000 0000
49Bh	T8PR	TMR8 Period Register								1111 1111	1111 1111
49Ch	T8CON	ON	CKPS<2:0>			OUTPS<3:0>				0000 0000	0000 0000
49Dh	T8HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					0000 0000	0000 0000
49Eh	T8CLKCON	—	—	—	—	CS<3:0>				---- 0000	---- 0000
49Fh	T8RST	—	—	—	RSEL<4:0>					---0 0000	---0 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

4.6 Device ID and Revision ID

The 14-bit device ID word is located at 8006h and the 14-bit revision ID is located at 8005h. These locations are read-only and cannot be erased or modified. See **Section 10.4 "User ID, Device ID and Configuration Word Access"** for more information on accessing these memory locations.

Development tools, such as device programmers and debuggers, may be used to read the Device ID and Revision ID.

4.7 Register Definitions: Device and Revision

REGISTER 4-3: DEVID: DEVICE ID REGISTER

R	R	R	R	R	R
DEV<13:8>					
bit 13					bit 8

R	R	R	R	R	R	R	R
DEV<7:0>							
bit 7							bit 0

Legend:	
R = Readable bit	
'1' = Bit is set	'0' = Bit is cleared

bit 13-0 **DEV<13:0>:** Device ID bits

Device	DEVID<13:0> Values
PIC16F1777	11 0000 1000 1110 (308E)
PIC16F1778	11 0000 1000 1111 (308F)
PIC16F1779	11 0000 1001 0000 (3090)
PIC16LF1777	11 0000 1001 0001 (3091)
PIC16LF1778	11 0000 1001 0010 (3092)
PIC16LF1779	11 0000 1001 0011 (3093)

REGISTER 7-9: PIR2: PERIPHERAL INTERRUPT REQUEST REGISTER 2

R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
OSFIF	C2IF	C1IF	COG1IF	BCL1IF	C4IF	C3IF	CCP2IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **OSFIF:** Oscillator Fail Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 6 **C2IF:** Comparator C2 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 5 **C1IF:** Comparator C1 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 4 **COG1IF:** COG1 Auto-Shutdown Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 3 **BCL1IF:** MSSP Bus Collision Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 2 **C4IF:** Comparator C4 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 1 **C3IF:** Comparator C3 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 0 **CCP2IF:** CCP2 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

9.1 Independent Clock Source

The WDT derives its time base from the 31 kHz LFINTOSC internal oscillator. Time intervals in this chapter are based on a nominal interval of 1 ms. See Table 36-8: Oscillator Parameters for the LFINTOSC specification.

9.2 WDT Operating Modes

The Watchdog Timer module has four operating modes controlled by the WDTE<1:0> bits in Configuration Words. See Table 9-1.

9.2.1 WDT IS ALWAYS ON

When the WDTE bits of Configuration Words are set to '11', the WDT is always on.

WDT protection is active during Sleep.

9.2.2 WDT IS OFF IN SLEEP

When the WDTE bits of Configuration Words are set to '10', the WDT is on, except in Sleep.

WDT protection is not active during Sleep.

9.2.3 WDT CONTROLLED BY SOFTWARE

When the WDTE bits of Configuration Words are set to '01', the WDT is controlled by the SWDTEN bit of the WDTCON register.

WDT protection is unchanged by Sleep. See Table 9-1 for more details.

TABLE 9-1: WDT OPERATING MODES

WDTE<1:0>	SWDTEN	Device Mode	WDT Mode
11	X	X	Active
10	X	Awake	Active
		Sleep	Disabled
01	1	X	Active
	0		Disabled
00	X	X	Disabled

9.3 Time-Out Period

The WDTPS bits of the WDTCON register set the time-out period from 1 ms to 256 seconds (nominal). After a Reset, the default time-out period is two seconds.

9.4 Clearing the WDT

The WDT is cleared when any of the following conditions occur:

- Any Reset
- CLRWDT instruction is executed
- Device enters Sleep
- Device wakes up from Sleep
- Oscillator fail
- WDT is disabled
- Oscillator Start-up Timer (OST) is running

See Table 9-2 for more information.

9.5 Operation During Sleep

When the device enters Sleep, the WDT is cleared. If the WDT is enabled during Sleep, the WDT resumes counting.

When the device exits Sleep, the WDT is cleared again. The WDT remains clear until the OST, if enabled, completes. See **Section 5.0 "Oscillator Module (with Fail-Safe Clock Monitor)"** for more information on the OST.

When a WDT time-out occurs while the device is in Sleep, no Reset is generated. Instead, the device wakes up and resumes operation. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register are changed to indicate the event. See STATUS Register (Register 3-1) for more information.

16.1.6 INTERRUPTS

The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC Interrupt Flag is the ADIF bit in the PIR1 register. The ADC Interrupt Enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

Note 1:	The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.
2:	The ADC operates during Sleep only when the FRC oscillator is selected.

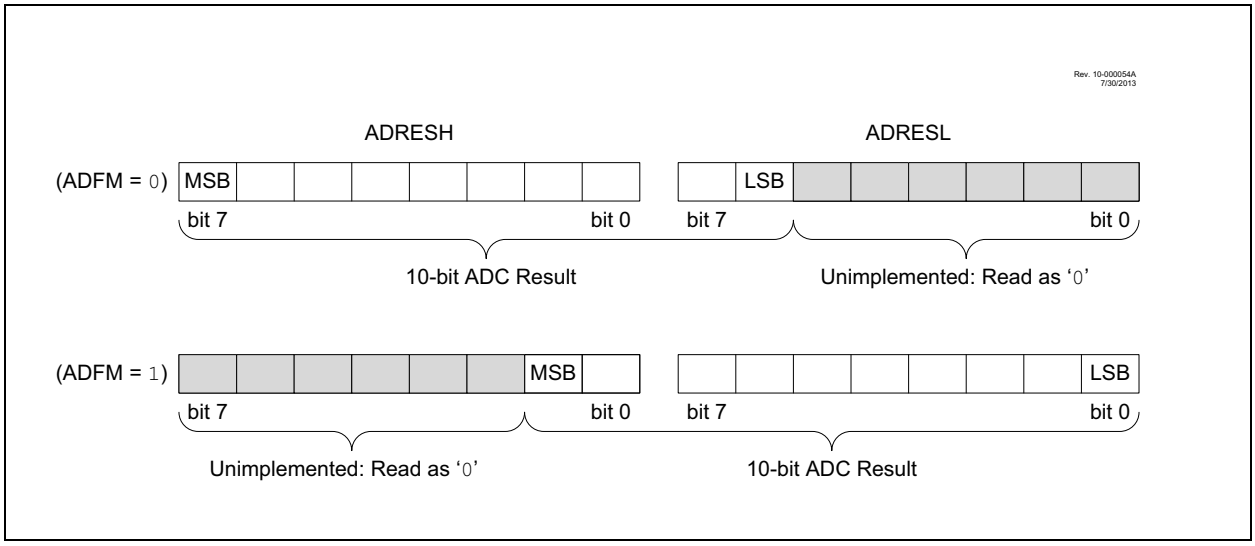
This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the ADIE bit of the PIE1 register and the PEIE bit of the INTCON register must both be set and the GIE bit of the INTCON register must be cleared. If all three of these bits are set, the execution will switch to the Interrupt Service Routine.

16.1.7 RESULT FORMATTING

The 10-bit ADC conversion result can be supplied in two formats, left justified or right justified. The ADFM bit of the ADCON1 register controls the output format.

Figure 16-3 shows the two output formats.

FIGURE 16-3: 10-BIT ADC CONVERSION RESULT FORMAT



17.6 Register Definitions: DAC Control

Long bit name prefixes for the 5-bit DAC peripherals are shown in Table 17-2. Refer to **Section 1.1 "Register and Bit naming conventions"** for more information

TABLE 17-2:

Peripheral	Bit Name Prefix
DAC3	DAC3
DAC4	DAC4
DAC7	DAC7
DAC8(1)	DAC8

Note 1: PIC16(L)F1777/9 only.

REGISTER 17-1: DACxCON0: DACx CONTROL REGISTER 0

R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0
EN	—	OE1	OE2	PSS<1:0>		NSS<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **EN:** DAC Enable bit
1 = DAC is enabled
0 = DAC is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **OE1:** DAC Voltage Output Enable bit
1 = DAC voltage level is also an output on the DACxOUT1 pin
0 = DAC voltage level is disconnected from the DACxOUT1 pin

bit 4 **OE2:** DAC Voltage Output Enable bit
1 = DAC voltage level is also an output on the DACxOUT2 pin
0 = DAC voltage level is disconnected from the DACxOUT2 pin

bit 3-2 **PSS<1:0>:** DAC Positive Source Select bits
11 = Reserved, do not use
10 = FVR Buffer2 output
01 = V_{REF+} pin
00 = V_{DD}

bit 1-0 **NSS<1:0>:** DAC Negative Source Select bits
11 = Reserved, do not use
10 = DACxREF1- (DAC7/8) or Reserved (DAC3/4)
01 = DACxREF0-
00 = AG_{ND} (AV_{SS})

19.2 Comparator Control

Each comparator has two control registers: CMxCON0 and CMxCON1.

The CMxCON0 register (see Register 19-1) contains Control and Status bits for the following:

- Enable
- Output
- Output polarity
- Zero latency filter
- Speed/Power selection
- Hysteresis enable
- Output synchronization

The CMxCON1 register (see Register 19-2) contains Control bits for the following:

- Interrupt enable
- Interrupt edge polarity
- Positive input channel selection
- Negative input channel selection

19.2.1 COMPARATOR ENABLE

Setting the ON bit of the CMxCON0 register enables the comparator for operation. Clearing the ON bit disables the comparator resulting in minimum current consumption.

19.2.2 COMPARATOR OUTPUT SELECTION

The output of the comparator can be monitored by reading either the OUT bit of the CMxCON0 register or the MCxOUT bit of the CMOUT register. In order to make the output available for an external connection, the following conditions must be true:

- Desired pin PPS control
- Corresponding TRIS bit must be cleared
- ON bit of the CMxCON0 register must be set

Note 1:	The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

19.2.3 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the POL bit of the CMxCON0 register. Clearing the POL bit results in a non-inverted output.

Table 19-2 shows the output state versus input conditions, including polarity control.

TABLE 19-2: COMPARATOR OUTPUT STATE VS. INPUT CONDITIONS

Input Condition	CxPOL	CxOUT
CxVN > CxVP	0	0
CxVN < CxVP	0	1
CxVN > CxVP	1	1
CxVN < CxVP	1	0

27.10.3 AUTO-SHUTDOWN RESTART

After an auto-shutdown event has occurred, there are two ways to resume operation:

- Software controlled
- Auto-restart

The restart method is selected with the ARSEN bit of the COGxASD0 register. Waveforms of a software controlled automatic restart are shown in Figure 27-15.

27.10.3.1 Software Controlled Restart

When the ARSEN bit of the COGxASD0 register is cleared, software must clear the ASE bit to restart COG operation after an auto-shutdown event.

The COG will resume operation on the first rising event after the ASE bit is cleared. Clearing the shutdown state requires all selected shutdown inputs to be false, otherwise, the ASE bit will remain set.

27.10.3.2 Auto-Restart

When the ARSEN bit of the COGxASD0 register is set, the COG will restart from the auto-shutdown state automatically.

The ASE bit will clear automatically and the COG will resume operation on the first rising event after all selected shutdown inputs go false.

REGISTER 27-18: COGxPHR: COG RISING EVENT PHASE DELAY COUNT REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	PHR<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **PHR<5:0>:** Rising Event Phase Delay Count Value bits
= Number of COGx clock periods to delay rising event

REGISTER 27-19: COGxPHF: COG FALLING EVENT PHASE DELAY COUNT REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	PHF<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **PHF<5:0>:** Falling Event Phase Delay Count Value bits
= Number of COGx clock periods to delay falling event

sensitive timing inputs that occur during, and extend beyond, the one-shot period will be suspended until the end of the one-shot time.

30.1.2.2 Rising Ramp

The Rising Ramp mode is identical to the Slope Compensation mode except that the ramps have a rising slope instead of a falling slope. One side of the internal capacitor is connected to the voltage input source and the other side is connected to the internal current source. The internal current source charges this capacitor at a programmable rate. As the capacitor charges, the capacitor voltage is added to the voltage source, producing a linear voltage rise at the required rate (see Figure 30-5). The ramp terminates and the capacitor is discharged when the set_falling timing input goes true. The next ramp starts when the set_rising timing input goes true.

Enabling the optional one-shot by setting the OS bit of the PRGxCON0 register ensures that the capacitor is fully discharged by overriding the set_rising timing input and holding the shorting switch closed for at least the one-shot period, typically 50 ns. Edge sensitive timing inputs that occur during the one-shot period will be ignored. Level sensitive timing inputs that occur during, and extend beyond, the one-shot period will be suspended until the end of the one-shot time.

30.2 Enable, Ready, Go

The EN bit of the PRGxCON0 register enables the analog circuitry including the current sources. This permits preparing the PRG module for use and allowing it to become stable before putting it into operation. When the EN bit is set then the timing inputs are enabled so that initial ramp action can be determined before the GO bit is set. The capacitor shorting switch is closed when the EN bit is set and remains closed while the GO bit is zero.

The RDY bit of the PRGxCON1 register indicates that the analog circuits and current sources are stable.

The GO bit of the PRGxCON0 register enables the switch control circuits, thereby putting the PRG into operation. The GO transition from cleared to set triggers the one-shot, thereby extending the capacitor shorting switch closure for the one-shot period.

To ensure predictable operation, set the EN bit first then wait for the RDY bit to go high before setting the GO bit.

30.3 Independent Set_rising and Set_falling Timing Inputs

The timing inputs determine when the ramp starts and stops. In the Alternating Rising/Falling mode the ramp rises when the set_rising input goes true and falls when the set_falling input goes true. In the Slope Compensation and Rising Ramp modes the capacitor is discharged when the set_falling timing input goes true and the ramp starts when the set_rising timing input goes true. The set_falling input dominates the set_rising input.

30.4 Level and Edge Timing Sensitivity

The set_rising and set_falling timing inputs can be independently configured as either level or edge sensitive.

Level sensitive operation is useful when it is necessary to detect a timing input true state after an overriding condition ceases. For example, level sensitivity is useful for capacitor generated timing inputs that may be suppressed by the overriding action of the one-shot. With level sensitivity a capacitor output that changes during the one-shot period will be detected at the end of the one-shot time. With edge sensitivity the change would be ignored.

Edge sensitive operation is useful for periodic timing inputs such as those generated by PWMs and clocks. The duty cycle of a level sensitive periodic signal may interfere with the other timing input. Consider an Alternating Ramp mode with a level sensitive 50% PWM as the set_rising timing source and a level sensitive comparator as the set_falling timing source. If the comparator output reverses the ramp while the PWM signal is still high then the ramp will improperly reverse again when the comparator signal goes low. That same scenario with the set_rising timing input set for edge sensitivity would properly change the ramp output to rising only on the rising edge of the PWM signal.

Set_rising and set_falling timing input edge sensitivity is selected with the respective REDG and FEDG bits of the PRGxCON1 register.

30.5 One-Shot Minimum Timing

The one-shot timer ensures a minimum capacitor discharge time in the Slope Compensation and Rising Ramp modes, and a minimum rising or falling ramp duration in the Alternating Ramp mode. Setting the OS bit of the PRGxCON0 register enables the one-shot timer.

30.6 DAC Voltage Sources

When using any of the DACs as the voltage source expect a voltage offset equal to the current setting times the DAC equivalent resistance. This will be a constant offset in the Slope Compensation and Ramp modes and a positive/negative step offset in the Alternating mode. To avoid this limitation, feed the DAC output to the PRG input through one of the op amps set for unity gain.

30.7 Operation During Sleep

The RG module is unaffected by Sleep.

30.8 Effects of a Reset

The RG module resets to a disabled condition.

REGISTER 30-5: PRGxRTSS: SET_RISING TIMING SOURCE SELECT REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	RTSS<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = value depends on configuration bits

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **RTSS<3:0>:** Set_rising Timing Source Select bits
See Table 30-5.

REGISTER 30-6: PRGxFTSS: SET_FALLING TIMING SOURCE SELECT REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	FTSS<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = value depends on configuration bits

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **FTSS<3:0>:** Set_falling Timing Source Select bits
See Table 30-5.

32.2 SPI Mode Overview

The Serial Peripheral Interface (SPI) bus is a synchronous serial data communication bus that operates in Full-Duplex mode. Devices communicate in a master/slave environment where the master device initiates the communication. A slave device is controlled through a Chip Select known as Slave Select.

The SPI bus specifies four signal connections:

- Serial Clock (SCK)
- Serial Data Out (SDO)
- Serial Data In (SDI)
- Slave Select ($\overline{SS}$)

Figure 32-1 shows the block diagram of the MSSP module when operating in SPI mode.

The SPI bus operates with a single master device and one or more slave devices. When multiple slave devices are used, an independent Slave Select connection is required from the master device to each slave device.

Figure 32-4 shows a typical connection between a master device and multiple slave devices.

The master selects only one slave at a time. Most slave devices have tri-state outputs so their output signal appears disconnected from the bus when they are not selected.

Transmissions involve two shift registers, eight bits in size, one in the master and one in the slave. With either the master or the slave device, data is always shifted out one bit at a time, with the Most Significant bit (MSb) shifted out first. At the same time, a new Least Significant bit (LSb) is shifted into the same register.

Figure 32-5 shows a typical connection between two processors configured as master and slave devices.

Data is shifted out of both shift registers on the programmed clock edge and latched on the opposite edge of the clock.

The master device transmits information out on its SDO output pin which is connected to, and received by, the slave's SDI input pin. The slave device transmits information out on its SDO output pin, which is connected to, and received by, the master's SDI input pin.

To begin communication, the master device first sends out the clock signal. Both the master and the slave devices should be configured for the same clock polarity.

The master device starts a transmission by sending out the MSb from its shift register. The slave device reads this bit from that same line and saves it into the LSb position of its shift register.

During each SPI clock cycle, a full-duplex data transmission occurs. This means that while the master device is sending out the MSb from its shift register (on its SDO pin) and the slave device is reading this bit and saving it as the LSb of its shift register, that the slave device is also sending out the MSb from its shift register (on its SDO pin) and the master device is reading this bit and saving it as the LSb of its shift register.

After eight bits have been shifted out, the master and slave have exchanged register values.

If there is more data to exchange, the shift registers are loaded with new data and the process repeats itself.

Whether the data is meaningful or not (dummy data), depends on the application software. This leads to three scenarios for data transmission:

- Master sends useful data and slave sends dummy data.
- Master sends useful data and slave sends useful data.
- Master sends dummy data and slave sends useful data.

Transmissions may involve any number of clock cycles. When there is no more data to be transmitted, the master stops sending the clock signal and it deselects the slave.

Every slave device connected to the bus that has not been selected through its slave select line must disregard the clock and transmission signals and must not transmit out any data of its own.

FIGURE 32-18: I²C SLAVE, 7-BIT ADDRESS, TRANSMISSION (AHEN = 0)

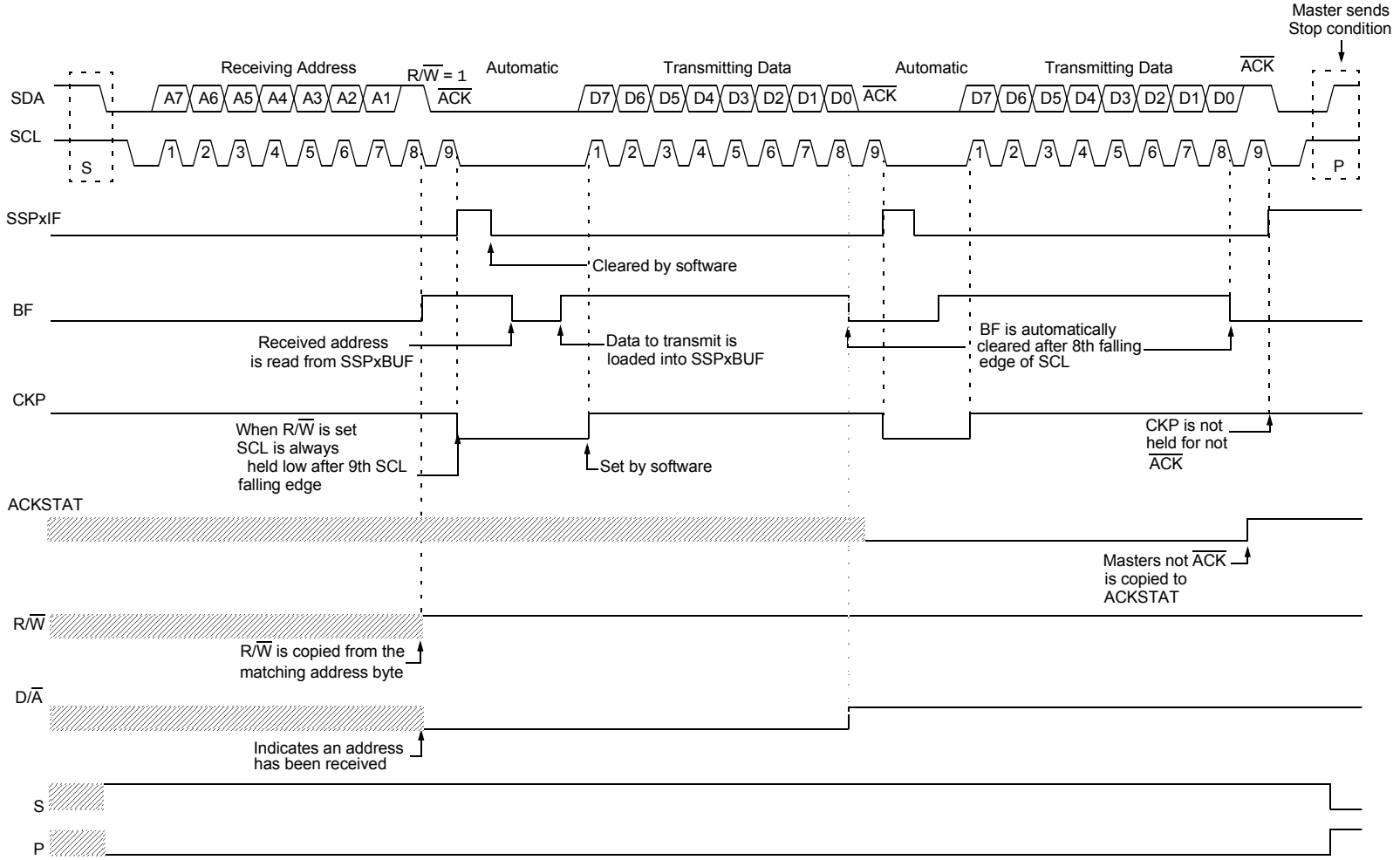


TABLE 33-5: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
	FOSC = 32.000 MHz			FOSC = 20.000 MHz			FOSC = 18.432 MHz			FOSC = 11.0592 MHz		
	Actual Rate	% Error	SPxBRG value (decimal)	Actual Rate	% Error	SPxBRG value (decimal)	Actual Rate	% Error	SPxBRG value (decimal)	Actual Rate	% Error	SPxBRG value (decimal)
300	300.0	0.00	26666	300.0	0.00	16665	300.0	0.00	15359	300.0	0.00	9215
1200	1200	0.00	6666	1200	-0.01	4166	1200	0.00	3839	1200	0.00	2303
2400	2400	0.01	3332	2400	0.02	2082	2400	0.00	1919	2400	0.00	1151
9600	9604	0.04	832	9597	-0.03	520	9600	0.00	479	9600	0.00	287
10417	10417	0.00	767	10417	0.00	479	10425	0.08	441	10433	0.16	264
19.2k	19.18k	-0.08	416	19.23k	0.16	259	19.20k	0.00	239	19.20k	0.00	143
57.6k	57.55k	-0.08	138	57.47k	-0.22	86	57.60k	0.00	79	57.60k	0.00	47
115.2k	115.9k	0.64	68	116.3k	0.94	42	115.2k	0.00	39	115.2k	0.00	23

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
	FOSC = 8.000 MHz			FOSC = 4.000 MHz			FOSC = 3.6864 MHz			FOSC = 1.000 MHz		
	Actual Rate	% Error	SPxBRG value (decimal)	Actual Rate	% Error	SPxBRG value (decimal)	Actual Rate	% Error	SPxBRG value (decimal)	Actual Rate	% Error	SPxBRG value (decimal)
300	300.0	0.00	6666	300.0	0.01	3332	300.0	0.00	3071	300.1	0.04	832
1200	1200	-0.02	1666	1200	0.04	832	1200	0.00	767	1202	0.16	207
2400	2401	0.04	832	2398	0.08	416	2400	0.00	383	2404	0.16	103
9600	9615	0.16	207	9615	0.16	103	9600	0.00	95	9615	0.16	25
10417	10417	0	191	10417	0.00	95	10473	0.53	87	10417	0.00	23
19.2k	19.23k	0.16	103	19.23k	0.16	51	19.20k	0.00	47	19.23k	0.16	12
57.6k	57.14k	-0.79	34	58.82k	2.12	16	57.60k	0.00	15	—	—	—
115.2k	117.6k	2.12	16	111.1k	-3.55	8	115.2k	0.00	7	—	—	—

MOVIW **Move INDFn to W**

Syntax: [*label*] MOVIW ++FSRn
[*label*] MOVIW --FSRn
[*label*] MOVIW FSRn++
[*label*] MOVIW FSRn--
[*label*] MOVIW k[FSRn]

Operands: n ∈ [0,1]
mm ∈ [00,01, 10, 11]
-32 ≤ k ≤ 31

Operation: INDFn → W
Effective address is determined by
- FSR + 1 (preincrement)
- FSR - 1 (predecrement)
- FSR + k (relative offset)

After the Move, the FSR value will be either:
- FSR + 1 (all increments)
- FSR - 1 (all decrements)
- Unchanged

Status Affected: Z

Mode	Syntax	mm
Preincrement	++FSRn	00
Predecrement	--FSRn	01
Postincrement	FSRn++	10
Postdecrement	FSRn--	11

Description: This instruction is used to move data between W and one of the indirect registers (INDFn). Before/after this move, the pointer (FSRn) is updated by pre/post incrementing/decrementing it.

Note: The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn.

FSRn is limited to the range 0000h - FFFFh. Incrementing/decrementing it beyond these bounds will cause it to wrap-around.

MOVLB **Move literal to BSR**

Syntax: [*label*] MOVLB k

Operands: 0 ≤ k ≤ 31

Operation: k → BSR

Status Affected: None

Description: The 5-bit literal 'k' is loaded into the Bank Select Register (BSR).

MOVLP **Move literal to PCLATH**

Syntax: [*label*] MOVLP k

Operands: 0 ≤ k ≤ 127

Operation: k → PCLATH

Status Affected: None

Description: The 7-bit literal 'k' is loaded into the PCLATH register.

MOVLW **Move literal to W**

Syntax: [*label*] MOVLW k

Operands: 0 ≤ k ≤ 255

Operation: k → (W)

Status Affected: None

Description: The 8-bit literal 'k' is loaded into W register. The "don't cares" will assemble as '0's.

Words: 1

Cycles: 1

Example:
```
MOVLW   0x5A
```
After Instruction
W = 0x5A

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f

Operands: 0 ≤ f ≤ 127

Operation: (W) → (f)

Status Affected: None

Description: Move data from W register to register 'f'.

Words: 1

Cycles: 1

Example:
```
MOVWF   OPTION_REG
```
Before Instruction
OPTION_REG = 0xFF
W = 0x4F
After Instruction
OPTION_REG = 0x4F
W = 0x4F

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

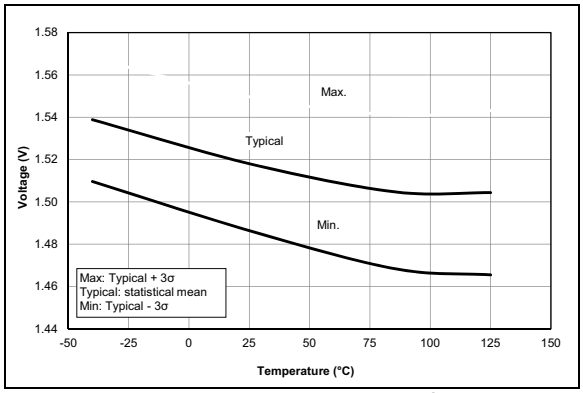


FIGURE 37-73: *POR Rearm Voltage, NP Mode (VREGPM1 = 0), PIC16F1773/6 Only.*

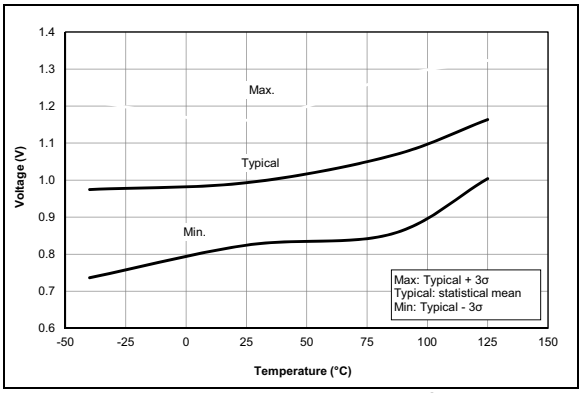


FIGURE 37-74: *POR Rearm Voltage, NP Mode, PIC16LF1777/8/9 Only.*

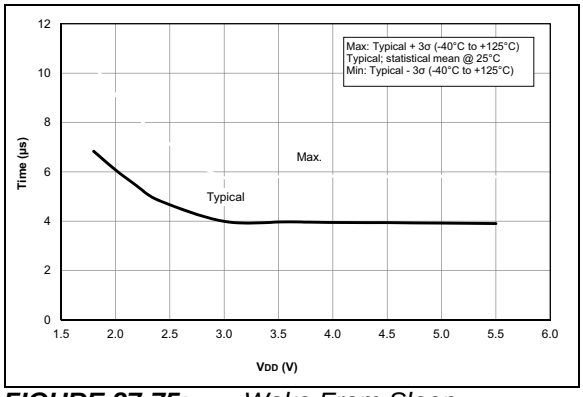


FIGURE 37-75: *Wake From Sleep, VREGPM = 0.*

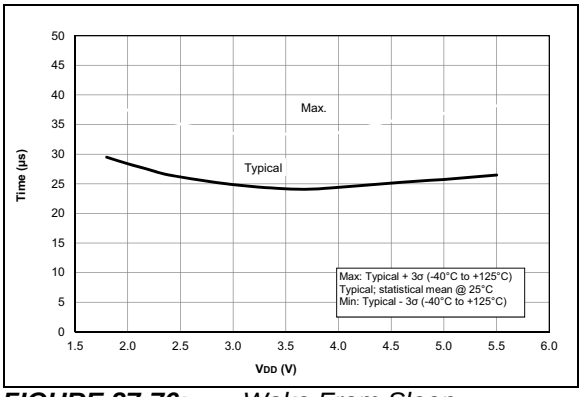


FIGURE 37-76: *Wake From Sleep, VREGPM = 1.*

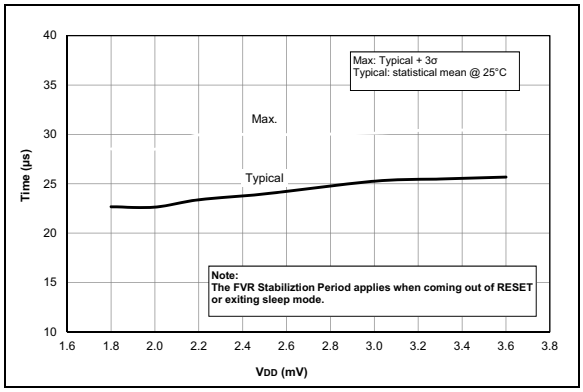


FIGURE 37-77: FVR Stabilization Period, *PIC16LF1777/8/9 Only.*

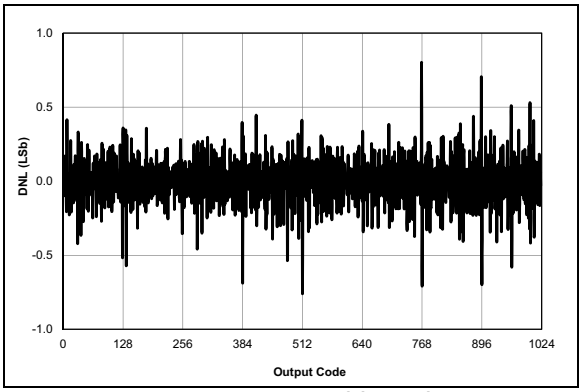


FIGURE 37-78: *ADC 10-bit Mode, Single-Ended DNL, V_{DD} = 3.0V, T_{AD} = 1 µS, 25°C.*