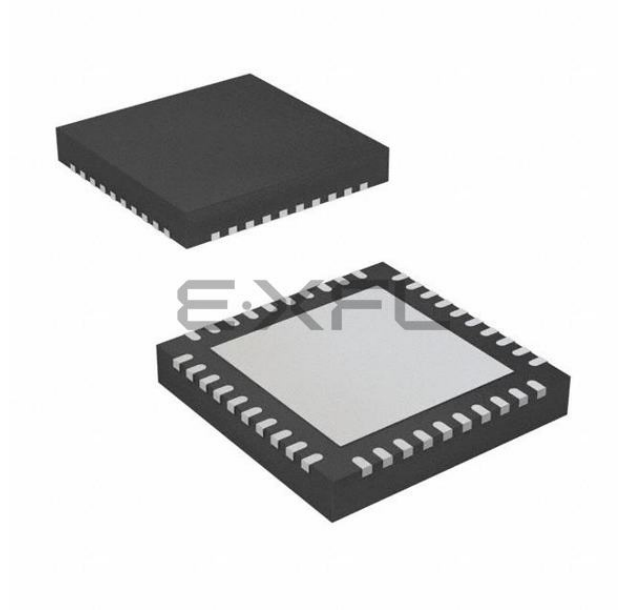

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Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1777-e-mv

TABLE 3: 28-PIN ALLOCATION TABLE (PIC16(L)F1778) (CONTINUED)

I/O	28-Pin SPDIP/SOIC/SSOP	28-Pin UQFN	ADC	VREF	DAC	Op Amp	Comparator	ZCD	PRG	Timers	PWM	CCP	COG	CLC	Modulator	EUSART	MSSP	Interrupt	Pull-ups	High Current	Basic
RB4	25	22	AN11	—	—	—	C3IN1+	—	—	T5G	—	—	—	—	MD3CH(1)	—	—	IOC	Y	—	—
RB5	26	23	AN13	DAC5REF1- DAC7REF1-	—	—	C4IN2-	—	—	T1G	—	CCP7(1)	—	—	MD3MOD(1)	—	—	IOC	Y	—	—
RB6	27	24	—	DAC5REF1+ DAC7REF1+	—	—	C4IN1+	—	—	—	—	—	—	CLCIN2(1)	—	—	—	IOC	Y	—	ICSPCLK
RB7	28	25	—	—	DAC1OUT2 DAC2OUT2 DAC3OUT2 DAC4OUT2 DAC5OUT2 DAC7OUT2	—	C5IN1+	—	—	T6IN(1)	—	—	—	CLCIN3(1)	—	—	—	IOC	Y	—	ICSPDAT
RC0	11	8	—	—	DAC5OUT1	—	—	—	—	T1CKI(1) T3CKI(1) T3G(1) SOSCO	—	—	—	—	—	—	—	IOC	Y	—	—
RC1	12	9	—	—	DAC7OUT1	—	—	—	PRG2R(1)	SOSCI	—	CCP2(1)	—	—	—	—	—	IOC	Y	—	—
RC2	13	10	AN14	—	—	—	C5IN2- C6IN2-	—	PRG2F(1)	T5CKI	—	CCP1(1)	—	—	—	—	—	IOC	Y	—	—
RC3	14	11	AN15	—	—	—	C1IN4- C2IN4- C3IN4- C4IN4- C5IN4- C6IN4-	—	—	T2IN(1)	—	—	—	—	MD2CL(1)	—	SCL	IOC	Y	—	—
RC4	15	12	AN16	—	—	—	C5IN3- C6IN3-	—	PRG3R(1)	T8IN(1)	—	—	—	—	MD2CH(1)	—	SDA	IOC	Y	—	—
RC5	16	13	AN17	—	—	OPA3IN0+	—	—	PRG3F(1)	T4IN(1)	—	—	—	—	MD2MOD(1)	—	—	IOC	Y	—	—
RC6	17	14	AN18	—	—	OPA3OUT	C5IN1- C6IN1-	—	PRG3IN0	—	—	—	—	—	—	—	—	IOC	Y	—	—
RC7	18	15	AN19	—	—	OPA3IN0-	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	—
RE3	1	26	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	—	—	$\overline{MCLR}$ V_{PP}
VDD	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	8	5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
VSS	19	16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection register.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F1777/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RD1/AN21/PRG3IN1/PRG4IN0/ C1IN4-/C2IN4-/C3IN4-/C4IN4-/ C5IN4-/C6IN4-/C7IN4-/C8IN4-/ OPA4OUT/OPA3IN1+/OPA3IN1-	RD1	TTL/ST	CMOS	General purpose I/O.
	AN21	AN	—	ADC Channel 21 input.
	PRG3IN1	AN	—	Ramp generator 3 reference voltage input.
	PRG4IN0	AN	—	Ramp generator 4 reference voltage input.
	C1IN4-	AN	—	Comparator 1 negative input.
	C2IN4-	AN	—	Comparator 2 negative input.
	C3IN4-	AN	—	Comparator 3 negative input.
	C4IN4-	AN	—	Comparator 4 negative input.
	C5IN4-	AN	—	Comparator 5 negative input.
	C6IN4-	AN	—	Comparator 6 negative input.
	C7IN4-	AN	—	Comparator 7 negative input.
	C8IN4-	AN	—	Comparator 8 negative input.
	OPA4OUT	—	AN	Operational amplifier 4 output.
	OPA3IN1+	AN	—	Operational amplifier 3 non-inverting input.
	OPA3IN1-	AN	—	Operational amplifier 3 inverting input.
RD2/AN22/DAC4OUT1/ OPA4IN0-	RD2	TTL/ST	CMOS	General purpose I/O.
	AN22	AN	—	ADC Channel 22 input.
	DAC4OUT1	—	AN	DAC4 voltage output.
	OPA4IN0-	AN	—	Operational amplifier 4 inverting input.
RD3/AN23/C8IN2-	RD3	TTL/ST	CMOS	General purpose I/O.
	AN23	AN	—	ADC Channel 23 input.
	C8IN2-	AN	—	Comparator 8 negative input.
RD4/AN24/C7IN2-	RD4	TTL/ST	CMOS	General purpose I/O.
	AN24	AN	—	ADC Channel 24 input.
	C7IN2-	AN	—	Comparator 8 negative input.
RD5/AN25/C7IN3-/C8IN3-	RD5	TTL/ST	CMOS	General purpose I/O.
	AN25	AN	—	ADC Channel 25 input.
	C7IN3-	AN	—	Comparator 7 negative input.
	C8IN3-	AN	—	Comparator 8 negative input.
RD6/AN26/C7IN1+	RD6	TTL/ST	CMOS	General purpose I/O.
	AN26	AN	—	ADC Channel 26 input.
	C7IN1+	AN	—	Comparator 7 positive input.
RD7/AN27/C8IN1+	RD7	TTL/ST	CMOS	General purpose I/O.
	AN27	AN	—	ADC Channel 27 input.
	C8IN1+	AN	—	Comparator 8 positive input.
RE0/AN5/DAC6REF1+/ DAC8REF1+	RE0	TTL/ST	CMOS	General purpose I/O.
	AN5	AN	—	ADC Channel 5 input.
	DAC6REF1+	AN	—	DAC6 positive reference.
	DAC8REF1+	AN	—	DAC8 positive reference.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HP = High Power XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 6											
30Ch	SLRCONA	SLRA7	SLRA6	SLRA5	SLRA4	SLRA3	SLRA2	SLRA1	SLRA0	1111 1111	1111 1111
30Dh	SLRCONB	SLRB7	SLRB6	SLRB5	SLRB4	SLRB3	SLRB2	SLRB1	SLRB0	1111 1111	1111 1111
30Eh	SLRCONC	SLRC7	SLRC6	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0	1111 1111	1111 1111
30Fh	SLRCOND(3)	SLRD7	SLRD6	SLRD5	SLRD4	SLRD3	SLRD2	SLRD1	SLRD0	1111 1111	1111 1111
310h	SLRCONE(3)	—	—	—	—	—	SLRE2	SLRE1	SLRE0	---- -111	---- -111
311h	CCPR8L	Capture/Compare/PWM Register 8 (LSB)								xxxx xxxx	uuuu uuuu
312h	CCPR8H	Capture/Compare/PWM Register 8 (MSB)								xxxx xxxx	uuuu uuuu
313h	CCP8CON	EN	—	OUT	FMT	MODE<3:0>				0-00 0000	0-00 0000
314h	CCP8CAP	—	—	—	—	CTS<3:0>				---- 0000	---- 0000
315h	MD1CON0	EN	—	OUT	OPOL	—	—	—	BIT	0-00 ---0	0-00 ---0
316h	MD1CON1	—	—	CHPOL	CHSYNC	—	—	CLPOL	CLSYNC	--00 --00	--00 --00
317h	MD1SRC	—	—	—	MS<4:0>					---0 0000	---0 0000
318h	MD1CARL	—	—	—	CL<4:0>					---0 0000	---0 0000
319h	MD1CARH	—	—	—	CH<4:0>					---0 0000	---0 0000
31Ah	—	Unimplemented								—	—
31Bh	MD2CON0	EN	—	OUT	OPOL	—	—	—	BIT	0-00 ---0	0-00 ---0
31Ch	MD2CON1	—	—	CHPOL	CHSYNC	—	—	CLPOL	CLSYNC	--00 --00	--00 --00
31Dh	MD2SRC	—	—	—	MS<4:0>					---0 0000	---0 0000
31Eh	MD2CARL	—	—	—	CL<4:0>					---0 0000	---0 0000
31Fh	MD2CARH	—	—	—	CH<4:0>					---0 0000	---0 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 10											
50Ch — 50Eh	—	Unimplemented								—	—
50Fh	OPA1NCHS	—	—	—	—	NCH<3:0>				---- 0000	---- 0000
510h	OPA1PCHS	—	—	—	—	PCH<3:0>				---- 0000	---- 0000
511h	OPA1CON	EN	—	—	UG	—	ORPOL	ORM<1:0>		0--0 -000	0--0 -000
512h	OPA1ORS	—	—	—	ORS<4:0>					---0 0000	---0 0000
513h	OPA2NCHS	—	—	—	—	NCH<3:0>				---- 0000	---- 0000
514h	OPA2PCHS	—	—	—	—	PCH<3:0>				---- 0000	---- 0000
515h	OPA2CON	EN	—	—	UG	—	ORPOL	ORM<1:0>		0--0 -000	0--0 -000
516h	OPA2ORS	—	—	—	ORS<4:0>					---0 0000	---0 0000
517h	OPA3NCHS	—	—	—	—	NCH<3:0>				---- 0000	---- 0000
518h	OPA3PCHS	—	—	—	—	PCH<3:0>				---- 0000	---- 0000
519h	OPA3CON	EN	SP	—	UG	—	ORPOL	ORM<1:0>		00-0 -000	00-0 -000
51Ah	OPA3ORS	—	—	—	ORS<4:0>					---0 0000	---0 0000
51Bh	OPA4NCHS(3)	—	—	—	—	NCH<3:0>				---- 0000	---- 0000
51Ch	OPA4PCHS(3)	—	—	—	—	PCH<3:0>				---- 0000	---- 0000
51Dh	OPA4CON(3)	EN	SP	—	UG	—	ORPOL	ORM<1:0>		00-0 -000	00-0 -000
51Eh	OPA4ORS(3)	—	—	—	ORS<4:0>					---0 0000	---0 0000
51Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

5.2.2.5 Internal Oscillator Frequency Selection

The system clock speed can be selected via software using the Internal Oscillator Frequency Select bits IRCF<3:0> of the OSCCON register.

The postscaled output of the 16 MHz HFINTOSC, 500 kHz MFINTOSC, and 31 kHz LFINTOSC connect to a multiplexer (see Figure 5-1). The Internal Oscillator Frequency Select bits IRCF<3:0> of the OSCCON register select the frequency output of the internal oscillators. One of the following frequencies can be selected via software:

- 32 MHz (requires 4x PLL)
- 16 MHz
- 8 MHz
- 4 MHz
- 2 MHz
- 1 MHz
- 500 kHz (default after Reset)
- 250 kHz
- 125 kHz
- 62.5 kHz
- 31.25 kHz
- 31 kHz (LFINTOSC)

Note:	Following any Reset, the IRCF<3:0> bits of the OSCCON register are set to '0111' and the frequency selection is set to 500 kHz. The user can modify the IRCF bits to select a different frequency.

The IRCF<3:0> bits of the OSCCON register allow duplicate selections for some frequencies. These duplicate choices can offer system design trade-offs. Lower power consumption can be obtained when changing oscillator sources for a given frequency. Faster transition times can be obtained between frequency changes that use the same oscillator source.

5.2.2.6 32 MHz Internal Oscillator Frequency Selection

The Internal Oscillator Block can be used with the 4x PLL associated with the External Oscillator Block to produce a 32 MHz internal system clock source. The following settings are required to use the 32 MHz internal clock source:

- The FOSC bits in Configuration Words must be set to use the INTOSC source as the device system clock (FOSC<2:0> = 100).
- The SCS bits in the OSCCON register must be cleared to use the clock determined by FOSC<2:0> in Configuration Words (SCS<1:0> = 00).
- The IRCF bits in the OSCCON register must be set to the 8 MHz HFINTOSC set to use (IRCF<3:0> = 1110).
- The SPLLEN bit in the OSCCON register must be set to enable the 4x PLL, or the PLLEN bit of the Configuration Words must be programmed to a '1'.

Note:	When using the PLLEN bit of the Configuration Words, the 4x PLL cannot be disabled by software and the SPLLEN option will not be available.

The 4x PLL is not available for use with the internal oscillator when the SCS bits of the OSCCON register are set to '1x'. The SCS bits must be set to '00' to use the 4x PLL with the internal oscillator.

5.3 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bits of the OSCCON register. The following clock sources can be selected using the SCS bits:

- Default system oscillator determined by FOSC bits in Configuration Words
- Timer1 32 kHz crystal oscillator
- Internal Oscillator Block (INTOSC)

5.3.1 SYSTEM CLOCK SELECT (SCS) BITS

The System Clock Select (SCS) bits of the OSCCON register select the system clock source that is used for the CPU and peripherals.

- When the SCS bits of the OSCCON register = 00, the system clock source is determined by the value of the FOSC<2:0> bits in the Configuration Words.
- When the SCS bits of the OSCCON register = 01, the system clock source is the secondary oscillator.
- When the SCS bits of the OSCCON register = 1x, the system clock source is chosen by the internal oscillator frequency selected by the IRCF<3:0> bits of the OSCCON register. After a Reset, the SCS bits of the OSCCON register are always cleared.

Note:	Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, does not update the SCS bits of the OSCCON register. The user can monitor the OSTS bit of the OSCSTAT register to determine the current system clock source.

When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 5-1.

5.3.2 OSCILLATOR START-UP TIMER STATUS (OSTS) BIT

The Oscillator Start-up Timer Status (OSTS) bit of the OSCSTAT register indicates whether the system clock is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Words, or from the internal clock source. In particular, OSTS indicates that the Oscillator Start-up Timer (OST) has timed out for LP, XT or HS modes. The OST does not reflect the status of the secondary oscillator.

5.3.3 SECONDARY OSCILLATOR

The secondary oscillator is a separate crystal oscillator associated with the Timer1 peripheral. It is optimized for timekeeping operations with a 32.768 kHz crystal connected between the SOSCO and SOSCI device pins.

The secondary oscillator is enabled using the OSCEN control bit in the T1CON register. See **Section 22.0 "Timer1/3/5 Module with Gate Control"** for more information about the Timer1 peripheral.

5.3.4 SECONDARY OSCILLATOR READY (SOSCR) BIT

The user must ensure that the secondary oscillator is ready to be used before it is selected as a system clock source. The Secondary Oscillator Ready (SOSCR) bit of the OSCSTAT register indicates whether the secondary oscillator is ready to be used. After the SOSCR bit is set, the SCS bits can be configured to select the secondary oscillator.

5.3.5 CLOCK SWITCH BEFORE SLEEP

When a clock switch from an old clock to a new clock is requested just prior to entering Sleep mode, it is necessary to confirm that the switch is complete before the sleep instruction is executed. Failure to do so may result in an incomplete switch and consequential loss of the system clock altogether. Clock switching is confirmed by monitoring the clock status bits in the OSCSTAT register. Switch confirmation can be accomplished by sensing that the ready bit for the new clock is set or the ready bit for the old clock is cleared. For example, when switching between the internal oscillator with the PLL and the internal oscillator without the PLL, monitor the PLLR bit. When PLLR is set, the switch to 32 MHz operation is complete. Conversely, when PLLR is cleared the switch from 32 MHz operation to the selected internal clock is complete.

8.3 Register Definitions: Voltage Regulator Control

REGISTER 8-1: VREGCON: VOLTAGE REGULATOR CONTROL REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-1/1
—	—	—	—	—	—	VREGPM	Reserved
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **VREGPM:** Voltage Regulator Power Mode Selection bit
- 1 = Low-Power Sleep mode enabled in Sleep(2)
  Draws lowest current in Sleep, slower wake-up
- 0 = Normal Power mode enabled in Sleep(2)
  Draws higher current in Sleep, faster wake-up

bit 0 **Reserved:** Read as ‘1’. Maintain this bit set.

Note 1: PIC16F1777/8/9 only.
2: See **Section 36.0 “Electrical Specifications”**.

TABLE 16-1: ADC CLOCK PERIOD (TAD) VS. DEVICE OPERATING FREQUENCIES

ADC Clock Period (TAD)		Device Frequency (FOSC)					
ADC Clock Source	ADCS<2:0>	32 MHz	20 MHz	16 MHz	8 MHz	4 MHz	1 MHz
FOSC/2	000	62.5ns(2)	100 ns(2)	125 ns(2)	250 ns(2)	500 ns(2)	2.0 μs
FOSC/4	100	125 ns(2)	200 ns(2)	250 ns(2)	500 ns(2)	1.0 μs	4.0 μs
FOSC/8	001	0.5 μs(2)	400 ns(2)	0.5 μs(2)	1.0 μs	2.0 μs	8.0 μs(3)
FOSC/16	101	800 ns	800 ns	1.0 μs	2.0 μs	4.0 μs	16.0 μs(3)
FOSC/32	010	1.0 μs	1.6 μs	2.0 μs	4.0 μs	8.0 μs(3)	32.0 μs(2)
FOSC/64	110	2.0 μs	3.2 μs	4.0 μs	8.0 μs(3)	16.0 μs(2)	64.0 μs(2)
FRC	x11	1.0-6.0 μs(1,4)	1.0-6.0 μs(1,4)	1.0-6.0 μs(1,4)	1.0-6.0 μs(1,4)	1.0-6.0 μs(1,4)	1.0-6.0 μs(1,4)

Legend: Shaded cells are outside of recommended range.

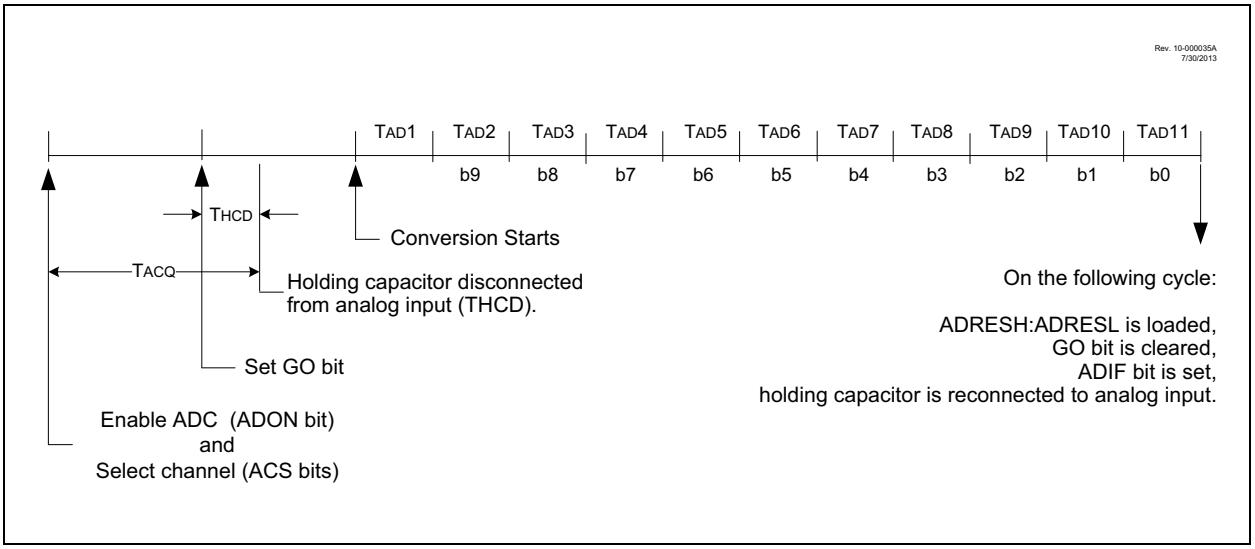
Note 1: See TAD parameter for FRC source typical TAD value.

2: These values violate the required TAD time.

3: Outside the recommended TAD time.

4: The ADC clock period (TAD) and total ADC conversion time can be minimized when the ADC clock is derived from the system clock FOSC. However, the FRC oscillator source must be used when conversions are to be performed with the device in Sleep mode.

FIGURE 16-2: ANALOG-TO-DIGITAL CONVERSION TAD CYCLES



18.0 10-BIT DIGITAL-TO-ANALOG CONVERTER (DAC) MODULE

The 10-bit Digital-to-Analog Converter (DAC) supplies a variable voltage reference, ratiometric with the input source, with 1024 selectable output levels.

The input of the DAC can be connected to:

- External VREF pins
- VDD supply voltage
- FVR (Fixed Voltage Reference)

The output of the DAC can be configured to supply a reference voltage to the following:

- Comparator positive input
- ADC input channel
- DACxOUT1 pin
- Op Amp

The Digital-to-Analog Converter is enabled by setting the EN bit of the DACxCON0 register.

TABLE 18-1: AVAILABLE 10-BIT DACS

Device	DAC1	DAC2	DAC5	DAC6
PIC16(L)F1778	•	•	•	
PIC16(L)F1777/9	•	•	•	•

18.1 Output Voltage Level Selection

The DAC has 1024 voltage levels that are set by the 10-bit reference selection word contained in the DACxREFH and DACxREFL registers. This 10-bit word can be left or right justified. See **Section 18.4 "DAC Reference Selection Justification"** for more detail.

The DAC output voltage can be determined with Equation 18-1.

18.2 Ratiometric Output Voltage

The DAC output voltage is derived using a resistor ladder with each end of the ladder tied to a positive and negative voltage source. If the voltage of either input source fluctuates, a similar fluctuation will result in the DAC output value.

The value of the individual resistors within the ladder can be found in Table 36-20.

18.3 DAC Output

The DAC voltage is always available to the internal peripherals that use it. The DAC voltage can be output to the DACxOUTx pin by setting the OEx bit of the DACxCON0 register. Selecting the DAC voltage for output on the DACxOUTx pin automatically overrides the digital output buffer and digital input threshold detector functions of that pin. Reading the DACxOUTx pin when it has been configured for DAC voltage output will always return a '0'.

Due to the limited current drive capability, a buffer must be used on the DAC voltage output for external connections to either DACxOUTx pin. Figure 18-3 shows a buffering technique example.

18.4 DAC Reference Selection Justification

The DAC reference selection can be configured to be left or right justified. When the FM bit of the DACxCON0 register is set, the 10-bit word is left justified such that the eight Most Significant bits fill the DACxREFH register and the two Least Significant bits are left justified in the DACxREFL register. When the FM bit is cleared, the 10-bit word is right justified such that the eight Least Significant bits fill the DACxREFL register and the two Most Significant bits are right justified in the DACxREFH register. Refer to Figure 18-1.

The DACxREFL and DACxREFH registers are double buffered. Writing to either register does not take effect immediately. Writing a '1' to the DACxLD bit of the DACLD register transfers the contents of the DACxREFH and DACxREFL registers to the buffers, thereby changing all 10-bits of the DAC reference selection simultaneously.

EQUATION 18-1: DAC OUTPUT VOLTAGE

IF EN = 1

$$DACx\_output = \left((V_{SOURCE+} - V_{SOURCE-}) \times \frac{DACxR[9:0]}{2^{10}} \right) + V_{SOURCE-}$$

$V_{SOURCE+} = V_{DD}$, V_{REF+}, *or FVR_buffer2*

$V_{SOURCE-} = V_{SS}$ *or* V_{REF-}

EQUATION 20-2: R-C CALCULATIONS

V_{peak} = external voltage source peak voltage
f = external voltage source frequency
C = series capacitor
R = series resistor
V_C = Peak capacitor voltage
ϕ = Capacitor induced zero crossing phase advance in radians
T_ϕ = Time ZC event occurs before actual zero crossing

$$Z = \frac{V_{PEAK}}{3x10^{-4}}$$

$$X_C = \frac{1}{(2\pi fC)}$$

$$R = \sqrt{Z^2 - X_C}$$

$$V_C = X_C(3x10^{-4})$$

$$\phi = Tan^{-1}\left(\frac{X_C}{R}\right)$$

$$T_\phi = \frac{\phi}{(2\pi f)}$$

V_{rms} = 120

EQUATION 20-3: R-C CALCULATIONS EXAMPLE

$$V_{peak} = V_{rms} \cdot \sqrt{2} = 169.7$$

f = 60 Hz
C = 0.1 μf

$$Z = \frac{V_{peak}}{3 \times 10^{-4}} = \frac{169.7}{3 \times 10^{-4}} = 565.7\ kOhms$$

$$X_C = \frac{1}{(2\pi fC)} = \frac{1}{(2\pi \cdot 60 \cdot 1 \cdot 10^{-7})} = 26.53\ \text{kOhms}$$

R = 560 kOhms

$$Z_R = \sqrt{(R^2 + X_C^2)} = 560.6\ kOhm\ \text{(using actual resistor)}$$

$$I_{peak} = \frac{V_{peak}}{Z_R} = 302.7 \cdot 10^{-6}$$

$$V_C = X_C \cdot I_{peak} = 8.0\ \text{V}$$

$$\phi = Tan^{-1}\left(\frac{X_C}{R}\right) = 0.047\ radians$$

$$T_\phi = \frac{\phi}{(2\pi f)} = 125.6\ \mu s$$

TABLE 24-4: SUMMARY OF REGISTERS ASSOCIATED WITH STANDARD PWM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CCPxCAP	—	—	—	—	CTS<3:0>				321
CCPxCON	EN	—	OUT	FMT	MODE<3:0>				319
CCPRxL	Capture/Compare/PWM Register x (LSB)								320
CCPRxH	Capture/Compare/PWM Register x (MSB)								320
CCPTMRS1	C8TSEL<1:0>(1)		C7TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>		323
CCPTMRS2	P10TSEL<1:0>(1)		P9TSEL<1:0>		P4TSEL<1:0>		P3TSEL<1:0>		323
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	132
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	133
PIE2	OSFIE	C2IE	C1IE	COG1IE	BCL1IE	C4IE	C3IE	CCP2IE	134
PIE5	CCP8IE(1)	CCP7IE	COG4IE(1)	COG3IE	C8IE(1)	C7IE(1)	C6IE	C5IE	137
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	139
PIR2	OSFIF	C2IF	C1IF	COG1IF	BCL1IF	C4IF	C3IF	CCP2IF	140
PIR5	CCP8IF(1)	CCP7IF	COG4IF(1)	COG3IF	C8IF(1)	C7IF(1)	C6IF	C5IF	143
T2PR	Timer2 Period Register								287*
T2CON	ON	CKPS<2:0>			OUTPS<3:0>				307
TMR2	Timer2 Module Register								287
T4PR	Timer4 Period Register								287*
T4CON	ON	CKPS<2:0>			OUTPS<3:0>				307
TMR4	Timer4 Module Register								287
T6PR	Timer6 Period Register								287*
T6CON	ON	CKPS<2:0>			OUTPS<3:0>				307
TMR6	Timer6 Module Register								287
T8PR	Timer8 Period Register								287*
T8CON	ON	CKPS<2:0>			OUTPS<3:0>				307
TMR8	Timer8 Module Register								287

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the PWM.
* Page provides register information.
Note 1: PIC16(L)F1777/9 only.

27.11 Buffer Updates

Changes to the phase, dead-band, and blanking count registers need to occur simultaneously during COG operation to avoid unintended operation that may occur as a result of delays between each register write. This is accomplished with the LD bit of the COGxCON0 register and double buffering of the phase, blanking and dead-band count registers.

Before the COG module is enabled, writing the count registers loads the count buffers without need of the LD bit. However, when the COG is enabled, the count buffer updates are suspended after writing the count registers until after the LD bit is set. When the LD bit is set, the phase, dead-band and blanking register values are transferred to the corresponding buffers synchronous with COG operation. The LD bit is cleared by hardware when the transfer is complete.

27.12 Input and Output Pin Selection

The COG has one selection for an input from a device pin. That one input can be used as rising and falling event source or a fault source. The COGxINPPS register is used to select the pin. Refer to registers xxxPPS (Register 12-1) and RxyPPS (Register 12-2).

The pin PPS control registers are used to enable the COG outputs. Any combination of outputs to pins is possible including multiple pins for the same output. See the RxyPPS control register and **Section 12.2 "PPS Outputs"** for more details.

27.13 Operation During Sleep

The COG continues to operate in Sleep provided that the COG_clock, rising event, and falling event sources remain active.

The HFINTSOC remains active during Sleep when the COG is enabled and the HFINTOSC is selected as the COG_clock source.

27.14 Configuring the COG

The following steps illustrate how to properly configure the COG to ensure a synchronous start with the rising event input:

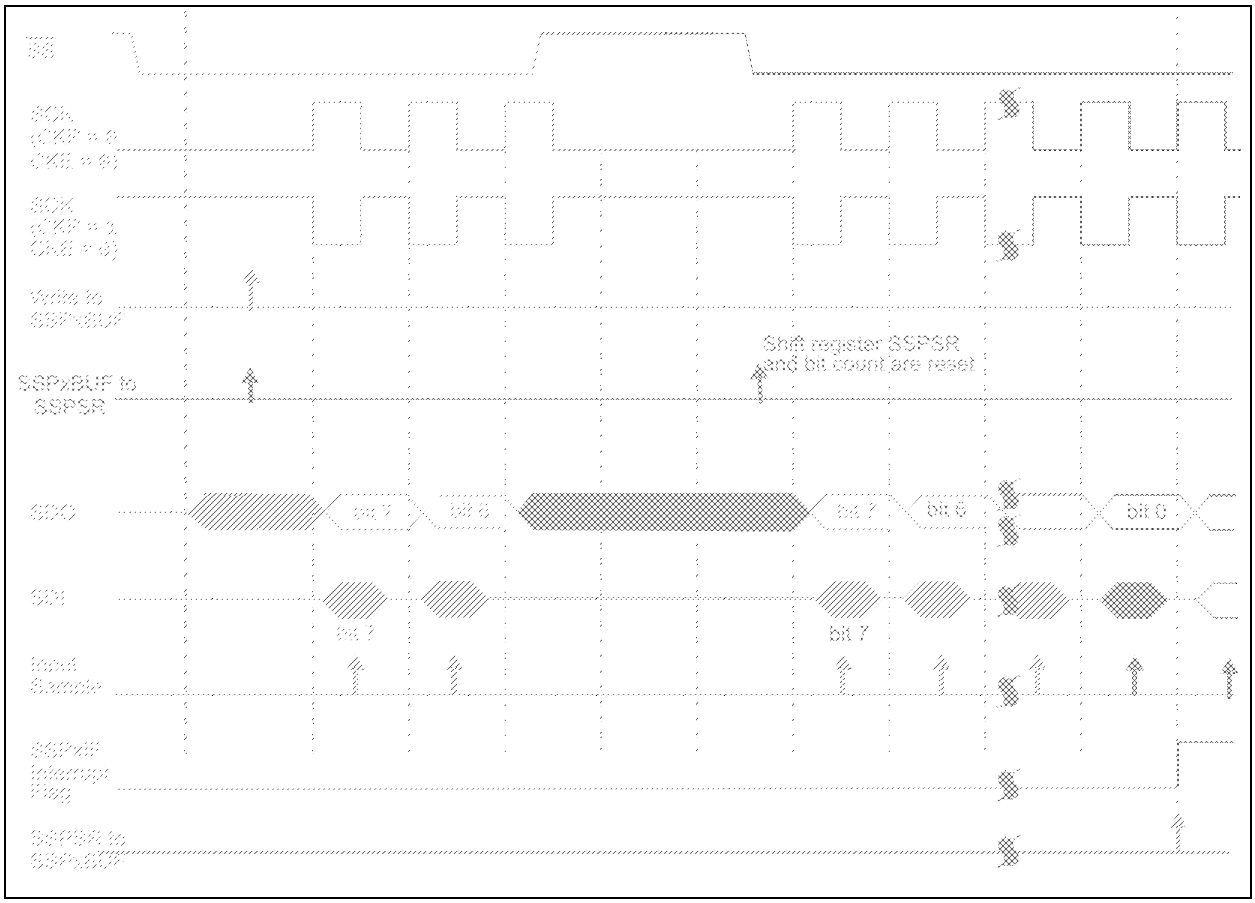
1. If a pin is to be used for the COG fault or event input, use the COGxINPPS register to configure the desired pin.
2. Clear all ANSEL register bits associated with pins that are used for COG functions.
3. Ensure that the TRIS control bits corresponding to the COG outputs to be used are set so that all are configured as inputs. The COG module will enable the output drivers as needed later.
4. Clear the EN bit, if not already cleared.
5. Set desired dead-band times with the COGxDBR and COGxDBF registers and select the source with the RDBS and FDBS bits of the COGxCON1 register.
6. Set desired blanking times with the COGxBLKR and COGxBLKF registers.
7. Set desired phase delay with the COGxPHR and COGxPHF registers.
8. Select the desired shutdown sources with the COGxASD1 register.
9. Setup the following controls in COGxASD0 auto-shutdown register:
   - Select both output override controls to the desired levels (this is necessary, even if not using auto-shutdown because start-up will be from a shutdown state).
   - Set the ASE bit and clear the ARSEN bit.
10. Select the desired rising and falling event sources with the COGxRIS0, COGxRIS1, COGxFIS0, and COGxFIS1 registers.
11. Select the desired rising and falling event modes with the COGxRSIM0, COGxRSIMI1, COGxFSIM0, and COGxFSIM1 registers.
12. Configure the following controls in the COGxCON1 register:
    - Set the polarity for each output
    - Select the desired dead-band timing sources
13. Configure the following controls in the COGxCON0 register:
    - Set the desired operating mode
    - Select the desired clock source
14. If one of the steering modes is selected then configure the following controls in the COGxSTR register:
    - Set the steering bits of the outputs to be used.
    - Set the desired static levels.
15. Set the EN bit.
16. Set the pin PPS controls to direct the COG outputs to the desired pins.
17. If auto-restart is to be used, set the ARSEN bit and the ASE will be cleared automatically. Otherwise, clear the ASE bit to start the COG.

TABLE 29-6: SUMMARY OF REGISTERS ASSOCIATED WITH OP AMPS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELB	---	---	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	182
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—	187
DAC1CON0	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC2CON0	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC5CON0	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC3CON0	EN	—	OE1	OE2	PSS<1:0>		NSS<1:0>		244
DAC4CON0	EN	—	OE1	OE2	PSS<1:0>		NSS<1:0>		244
DAC7CON0	EN	—	OE1	OE2	PSS<1:0>		NSS<1:0>		244
DAC3REF	---	---	---	REF<4:0>					245
DAC4REF	---	---	---	REF<4:0>					245
DAC7REF	---	---	---	REF<4:0>					245
DAC1REFH	REF<9:x> (x Depends on FM bit)								250
DAC2REFH	REF<9:x> (x Depends on FM bit)								250
DAC5REFH	REF<9:x> (x Depends on FM bit)								250
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		223
OPAxCON	EN	—	—	UG	—	ORPOL	ORM<1:0>		408
OPAxNCHS	—	—	—	—	NCH<3:0>				410
OPAxPCHS	—	—	—	—	PCH<3:0>				411
OPAxORS	—	—	—	ORS<4:0>					409
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	181
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	186

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by op amps.

FIGURE 32-8: SLAVE SELECT SYNCHRONOUS WAVEFORM



32.2.6 SPI OPERATION IN SLEEP MODE

In SPI Master mode, module clocks may be operating at a different speed than when in Full-Power mode; in the case of the Sleep mode, all clocks are halted.

Special care must be taken by the user when the MSSP clock is much faster than the system clock.

In Slave mode, when MSSP interrupts are enabled, after the master completes sending data, an MSSP interrupt will wake the controller from Sleep.

If an exit from Sleep mode is not desired, MSSP interrupts should be disabled.

In SPI Master mode, when the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the device wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all eight bits have been received, the MSSP interrupt flag bit will be set and if enabled, will wake the device.

TABLE 32-1: SUMMARY OF REGISTERS ASSOCIATED WITH SPI OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	177
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—	187
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	132
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	133
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	139
RxyPPS	—	—	RxyPPS<5:0>						205
SSPCLKPPS	—	—	SSPCLKPPS<5:0>						205, 207
SSPDATPPS	—	—	SSPDATPPS<5:0>						205, 207
SSPSSPPS	—	—	SSPSSPPS<5:0>						205, 207
SSP1BUF	Synchronous Serial Port Receive Buffer/Transmit Register								444*
SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				489
SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	488
SSP1STAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	488
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	176
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	181
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	186

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the MSSP in SPI mode.

* Page provides register information.

TABLE 36-3: POWER-DOWN CURRENTS (I_{PD})(1,2) (CONTINUED)

PIC16LF1777/8/9		Operating Conditions: (unless otherwise stated) Low-Power Sleep Mode						
PIC16F1777/8/9		Low-Power Sleep Mode, VREGPM = 1						
Param No.	Device Characteristics	Min.	Typ†	Max. +85°C	Max. +125°C	Units	Conditions	
							V_{DD}	Note
D029		—	0.05	2	9	μA	1.8	ADC Current **(Note 3)**, no conversion in progress
		—	0.08	3	10	μA	3.0	
D029		—	0.3	4	12	μA	2.3	ADC Current **(Note 3)**, no conversion in progress
		—	0.4	5	13	μA	3.0	
		—	0.5	7	16	μA	5.0	
D030		—	250	—	—	μA	1.8	ADC Current **(Note 3)**, conversion in progress
		—	250	—	—	μA	3.0	
D030		—	280	—	—	μA	2.3	ADC Current **(Note 3)**, conversion in progress
		—	280	—	—	μA	3.0	
		—	280	—	—	μA	5.0	
D031		—	250	650	—	μA	3.0	Op Amp (High power)
D031		—	250	650	—	μA	3.0	Op Amp (High power)
		—	350	850	—	μA	5.0	
D032		—	250	600	—	μA	1.8	Comparator, CxSP = 0
		—	300	650	—	μA	3.0	
D032		—	280	600	—	μA	2.3	Comparator, CxSP = 0 VREGPM = 0
		—	300	650	—	μA	3.0	
		—	310	650	—	μA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base I_{PD} and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base I_{DD} or I_{PD} current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{SS}.

3: ADC clock source is FRC.

FIGURE 36-17: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)

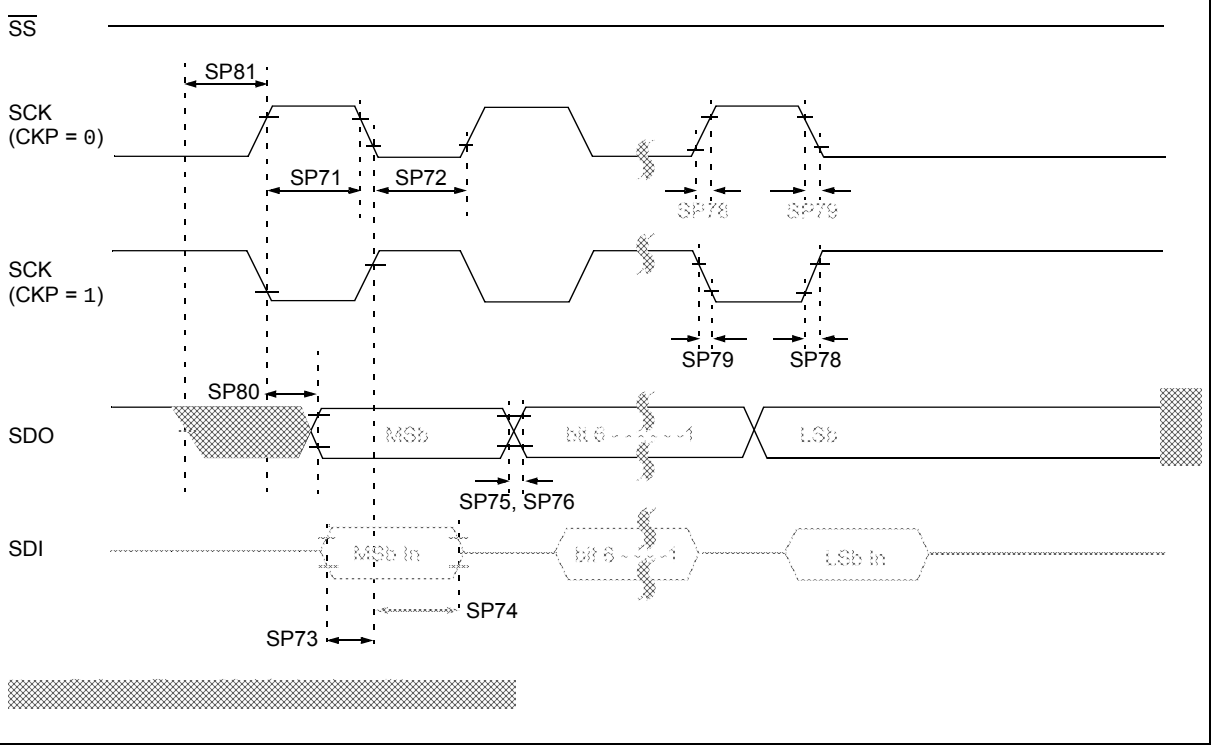
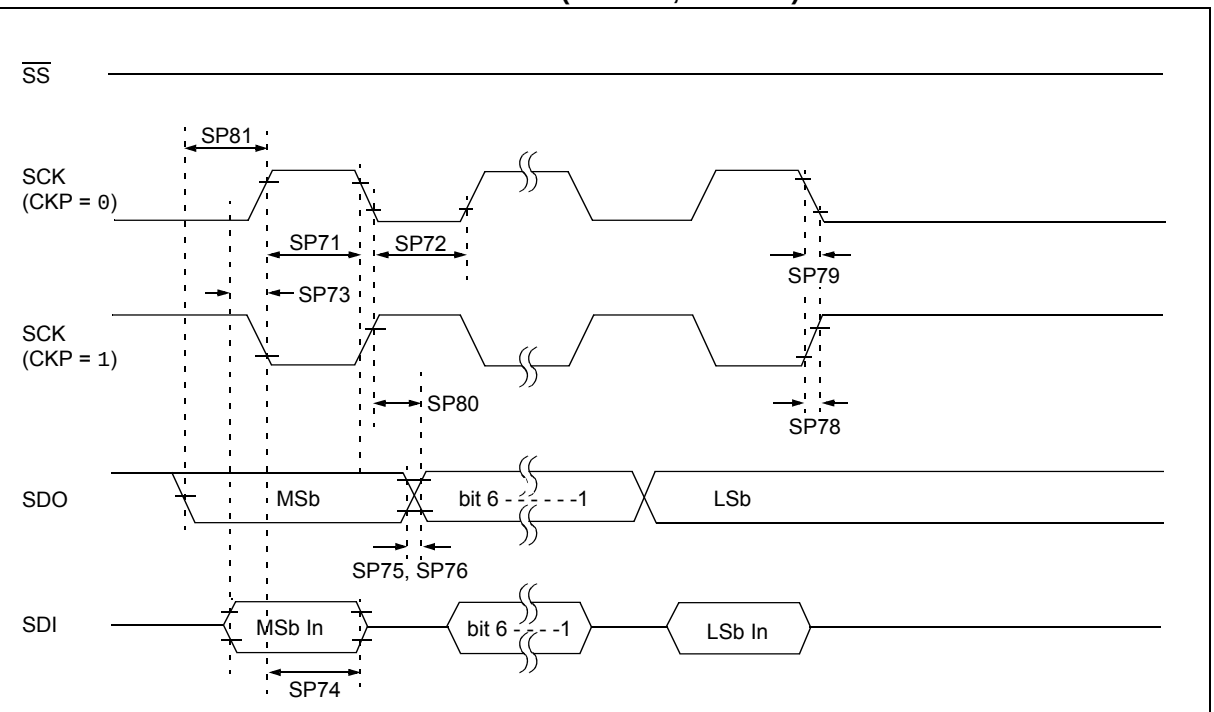


FIGURE 36-18: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)



Note: Refer to Figure 36-4 for load conditions.

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

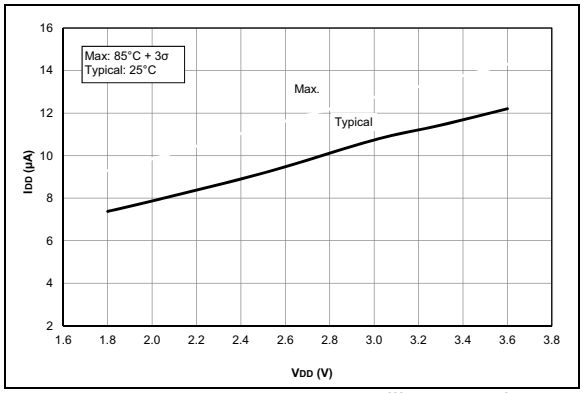


FIGURE 37-1: *IDD, LP Oscillator Mode, Fosc = 32 kHz, PIC16LF1777/8/9 Only.*

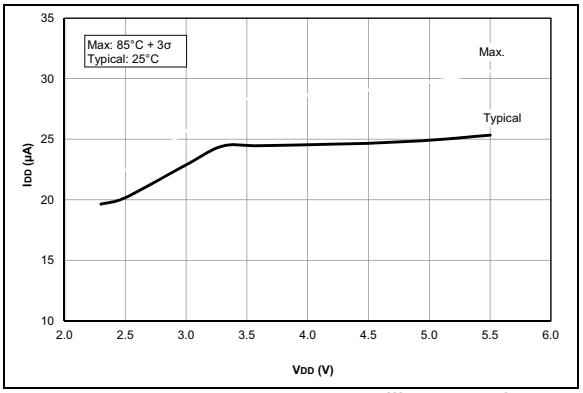


FIGURE 37-2: *IDD, LP Oscillator Mode, Fosc = 32 kHz, PIC16F1777/8/9 Only.*

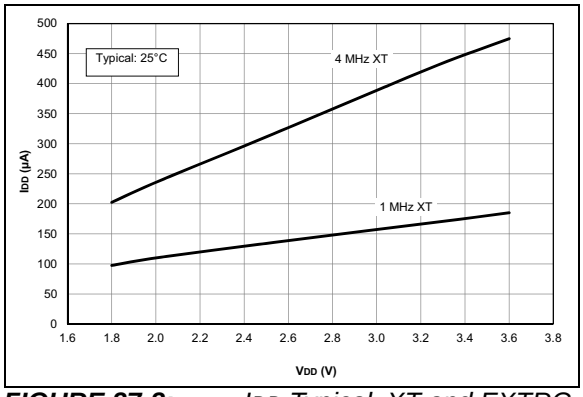


FIGURE 37-3: *IDD Typical, XT and EXTRC Oscillator, PIC16LF1777/8/9 Only.*

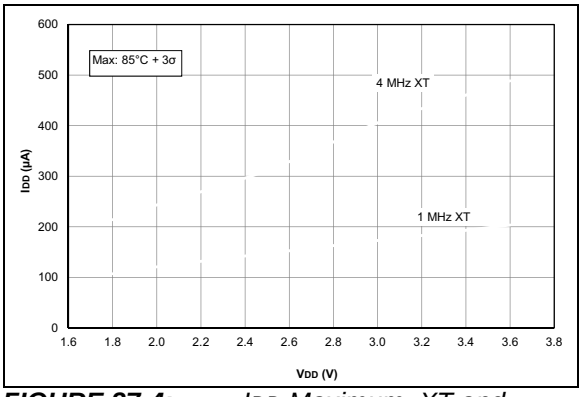


FIGURE 37-4: *IDD Maximum, XT and EXTRC Oscillator, PIC16LF1777/8/9 Only.*

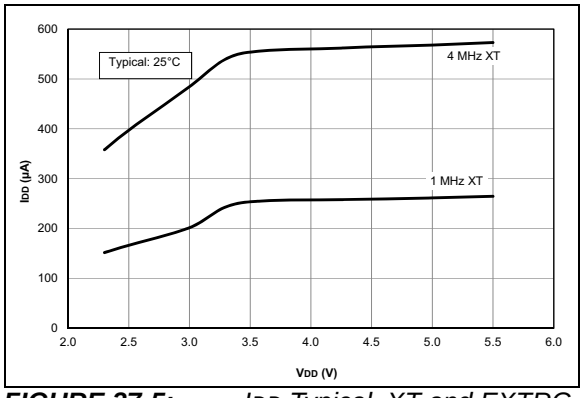


FIGURE 37-5: *IDD Typical, XT and EXTRC Oscillator, PIC16F1777/8/9 Only.*

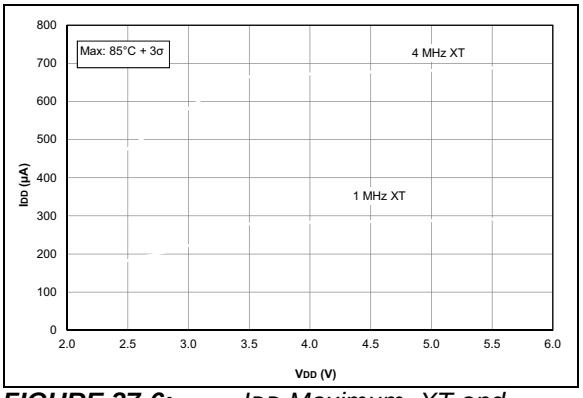


FIGURE 37-6: *IDD Maximum, XT and EXTRC Oscillator, PIC16F1777/8/9 Only.*

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

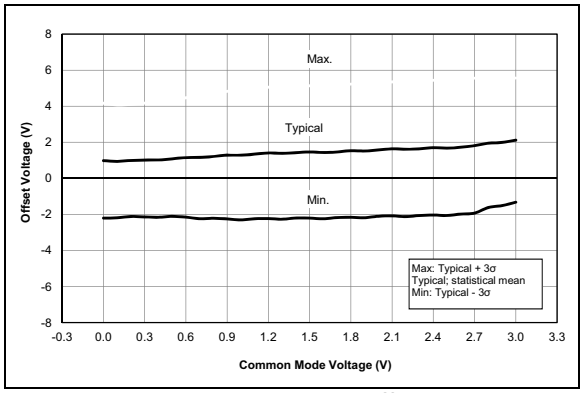


FIGURE 37-97: *Op Amp, Offset over Common Mode Voltage, V_{DD} = 3.0V, Temp. = 25°C*

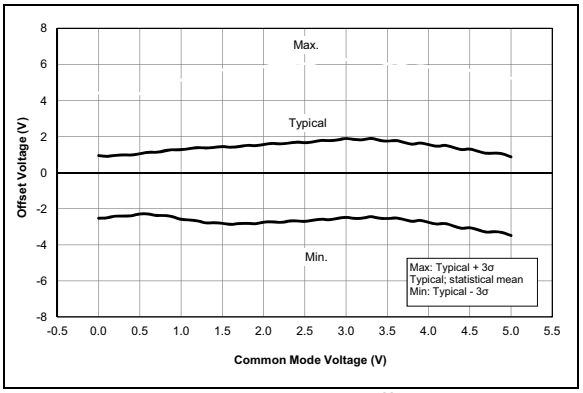


FIGURE 37-98: *Op Amp, Offset over Common Mode Voltage, V_{DD} = 5.0V, Temp. = 25°C, PIC16F1777/8/9 Only.*

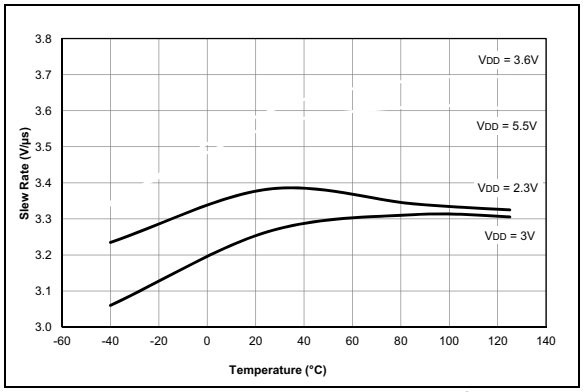


FIGURE 37-99: *Op Amp, Output Slew Rate, Rising Edge, PIC16F1777/8/9 Only.*

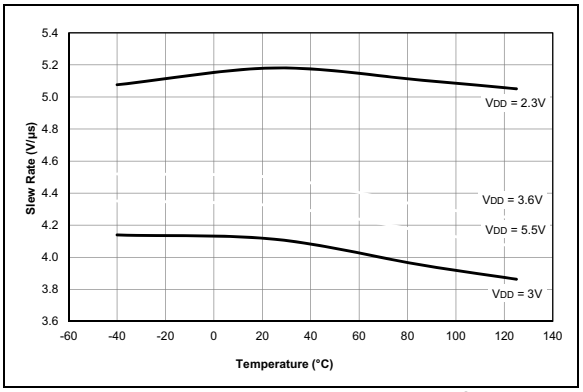


FIGURE 37-100: *Op Amp, Output Slew Rate, Falling Edge, PIC16F1777/8/9 Only.*

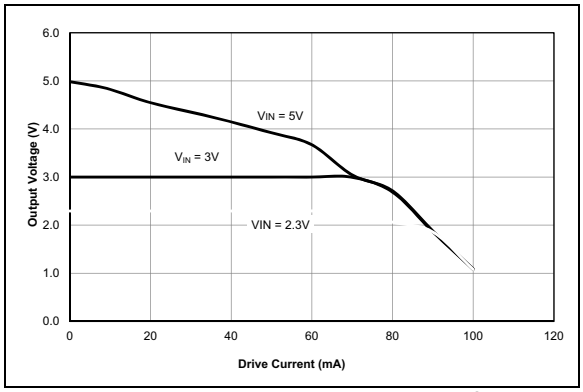


FIGURE 37-101: *Op Amp, Output Drive Strength, V_{DD} = 5.0V, Temp. = 25°C, PIC16F1777/8/9 Only.*

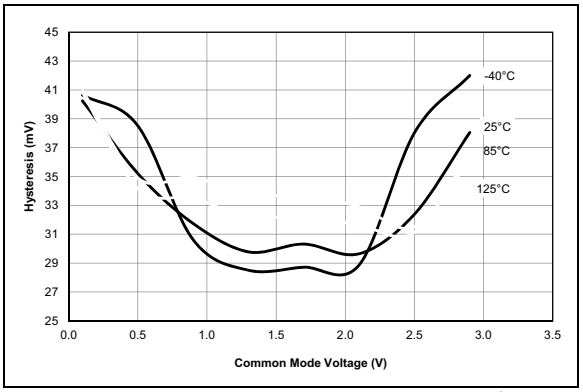


FIGURE 37-102: *Comparator Hysteresis, NP Mode (CxSP = 1), V_{DD} = 3.0V, Typical Measured Values.*

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A (11/2015)

Initial release of this document.

Revision B (10/2016)

Updated Figures 14-1, 23-3, 23-8, 23-9, and 23-10; Registers 7-5, 7-11, 18-1, 19-1, 24-6, 27-11, 31-3, 31-4, 31-5, 31-6, 31-7, and 32-4; Section 32.6; Tables 3, 4, 3-4, 3-6, 3-7, 3-14, 3-15, 3-18, 12-1, 12-2, 12-3, 24-4, 25-5, 27-5, 27-6, 28-1, 32-4, 36-1, 36-2, 36-7 and 36-8.

Updated the Cover page.

Section 20.5 rewritten. Added Characterization Data.