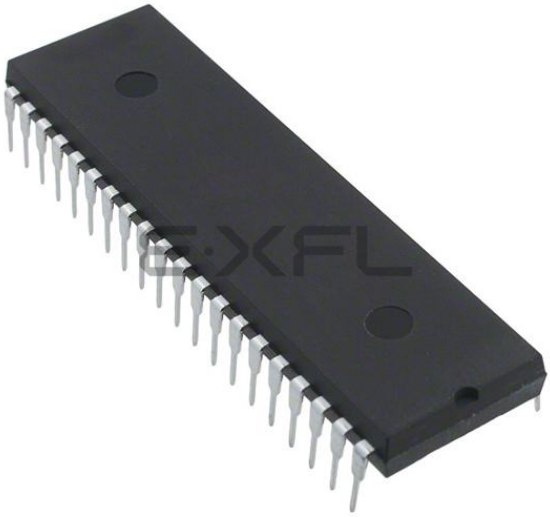

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 28x10b; D/A 4x5b, 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1777-e-p

TABLE 1-3: PIC16(L)F1777/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC4/AN16/C5IN3-/C6IN3-/ PRG3R/T8IN/MD2CH/SDA	RC4	TTL/ST	CMOS	General purpose I/O.
	AN16	AN	—	ADC Channel 16 input.
	C5IN3-	AN	—	Comparator 5 negative input.
	C6IN3-	AN	—	Comparator 6 negative input.
	PRG3R(1)	TTL/ST	—	Ramp generator set_rising input.
	T8IN(1)	TTL/ST	—	Timer8 gate input.
	MD2CH(1)	TTL/ST	—	Data signal modulator 2 high carrier input.
	SDA	I^2C	OD	I^2C data input/output.
RC5/AN17/OPA3IN0+/PRG3F/ T4IN/MD2MOD	RC5	TTL/ST	CMOS	General purpose I/O.
	AN17	AN	—	ADC Channel 17 input.
	OPA3IN0	AN	—	Operational amplifier 3 inverting input.
	PRG3F(1)	TTL/ST	—	Ramp generator set_falling input.
	T4IN(1)	TTL/ST	—	Timer4 gate input.
	MD2MOD(1)	TTL/ST	—	Data signal modulator modulation input.
RC6/AN18/PRG3IN0/PRG4IN1/ C5IN1-/C6IN1-/C7IN1-/C8IN1-/ OPA3OUT/OPA4IN1+/OPA4IN1-	RC6	TTL/ST	CMOS	General purpose I/O.
	AN18	AN	—	ADC Channel 18 input.
	PRG3IN0	AN	—	Ramp generator 3 reference voltage input.
	PRG4IN1	AN	—	Ramp generator 4 reference voltage input.
	C5IN1-	AN	—	Comparator 5 negative input.
	C6IN1-	AN	—	Comparator 6 negative input.
	C7IN1-	AN	—	Comparator 7 negative input.
	C8IN1-	AN	—	Comparator 8 negative input.
	OPA3OUT	—	AN	Operational amplifier 3 output.
	OPA4IN1+	AN	—	Operational amplifier 4 non-inverting input.
	OPA4IN1-	AN	—	Operational amplifier 4 inverting input.
RC7/AN19/OPA3IN0-	RC7	TTL/ST	CMOS	General purpose I/O.
	AN19	AN	—	ADC Channel 19 input.
	OPA3IN0-	AN	—	Operational amplifier 3 non-inverting input.
RD0/AN20/OPA4IN0+	RD0	TTL/ST	CMOS	General purpose I/O.
	AN20	AN	—	ADC Channel 20 input.
	OPA4IN0+	AN	—	Operational amplifier 4 non-inverting input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HP = High Power XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

3.4 Register Definitions: Status

REGISTER 3-1: STATUS: STATUS REGISTER

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **$\overline{TO}$:** Time-Out bit
1 = After power-up, CLRWDT instruction or SLEEP instruction
0 = A WDT Time-out occurred

bit 3 **$\overline{PD}$:** Power-Down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{\text{Digit Borrow}}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{\text{Borrow}}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{\text{Borrow}}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand.

TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 29 (Cont.)											
EA8h	RD0PPS(3)	—	—	RD0PPS<5:0>						--00 0000	--uu uuuu
EA9h	RD1PPS(3)	—	—	RD1PPS<5:0>						--00 0000	--uu uuuu
EAAh	RD2PPS(3)	—	—	RD2PPS<5:0>						--00 0000	--uu uuuu
EABh	RD3PPS(3)	—	—	RD3PPS<5:0>						--00 0000	--uu uuuu
EACh	RD4PPS(3)	—	—	RD4PPS<5:0>						--00 0000	--uu uuuu
EADh	RD5PPS(3)	—	—	RD5PPS<5:0>						--00 0000	--uu uuuu
EAEh	RD6PPS(3)	—	—	RD6PPS<5:0>						--00 0000	--uu uuuu
EAFh	RD7PPS(3)	—	—	RD7PPS<5:0>						--00 0000	--uu uuuu
EB0h	RE0PPS(3)	—	—	RE0PPS<5:0>						--00 0000	--uu uuuu
EB1h	RE1PPS(3)	—	—	RE1PPS<5:0>						--00 0000	--uu uuuu
EB2h	RE2PPS(3)	—	—	RE2PPS<5:0>						--00 0000	--uu uuuu
EB3h to EEFh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

7.6 Register Definitions: Interrupt Control

REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-0/0
GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all active interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all active peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **TMR0IE:** Timer0 Overflow Interrupt Enable bit
1 = Enables the Timer0 interrupt
0 = Disables the Timer0 interrupt

bit 4 **INTE:** INT External Interrupt Enable bit
1 = Enables the INT external interrupt
0 = Disables the INT external interrupt

bit 3 **IOCIE:** Interrupt-on-Change Enable bit
1 = Enables the interrupt-on-change
0 = Disables the interrupt-on-change

bit 2 **TMR0IF:** Timer0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed
0 = TMR0 register did not overflow

bit 1 **INTF:** INT External Interrupt Flag bit
1 = The INT external interrupt occurred
0 = The INT external interrupt did not occur

bit 0 **IOCIF:** Interrupt-on-Change Interrupt Flag bit(1)
1 = When at least one of the interrupt-on-change pins changed state
0 = None of the interrupt-on-change pins have changed state

Note 1: The IOCIF Flag bit is read-only and cleared when all the interrupt-on-change flags in the IOCxF registers have been cleared by software.

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 7-6: PIE5: PERIPHERAL INTERRUPT ENABLE REGISTER 5

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
CCP8IE(1)	CCP7IE	COG4IE	COG3IE	C8IE(1)	C7IE(1)	C6IE	C5IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **CCP8IE:** CCP8 Interrupt Enable bit(1)
- 1 = Enables the CCP8 interrupt
- 0 = Disables the CCP8 interrupt

bit 6 **CCP7IE:** CCP7 Interrupt Enable bit
- 1 = Enables the CCP7 interrupt
- 0 = Disables the CCP7 interrupt

bit 5 **COG4IE:** COG4 Auto-Shutdown Interrupt Enable bit
- 1 = COG4 interrupt enabled
- 0 = COG4 interrupt disabled

bit 4 **COG3IE:** COG3 Auto-Shutdown Interrupt Enable bit
- 1 = COG3 interrupt enabled
- 0 = COG3 interrupt disabled

bit 3 **C8IE:** Comparator C8 Interrupt Enable bit(1)
- 1 = Enables the Comparator C8 interrupt
- 0 = Disables the Comparator C8 interrupt

bit 2 **C7IE:** Comparator C7 Interrupt Enable bit(1)
- 1 = Enables the Comparator C7 interrupt
- 0 = Disables the Comparator C7 interrupt

bit 1 **C6IE:** Comparator C6 Interrupt Enable bit
- 1 = Enables the Comparator C6 interrupt
- 0 = Disables the Comparator C6 interrupt

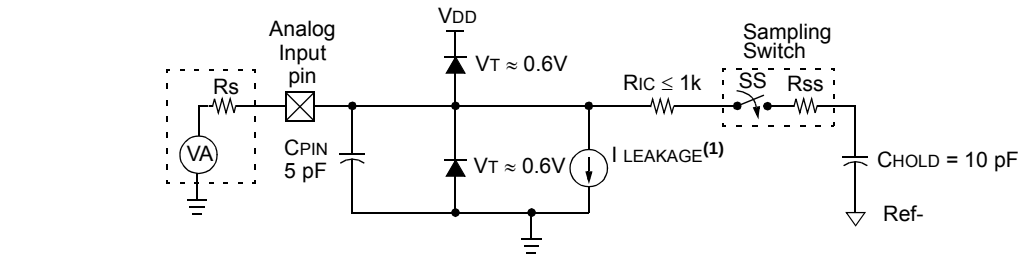
bit 0 **C5IE:** Comparator C5 Interrupt Enable bit
- 1 = Enables the Comparator C5 interrupt
- 0 = Disables the Comparator C5 interrupt

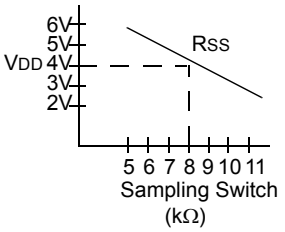
Note 1: PIC16(L)F1777/9 only.

EXAMPLE 10-2: ERASING ONE ROW OF PROGRAM MEMORY

```
; This row erase routine assumes the following:
; 1. A valid address within the erase row is loaded in ADDRH:ADDRL
; 2. ADDRH and ADDRL are located in shared data memory 0x70 - 0x7F (common RAM)


        BCF         INTCON,GIE      ; Disable ints so required sequences will execute properly
        BANKSEL     PMADRL
        MOVF        ADDRL,W         ; Load lower 8 bits of erase address boundary
        MOVWF       PMADRL
        MOVF        ADDRH,W         ; Load upper 6 bits of erase address boundary
        MOVWF       PMADRH
        BCF         PMCON1,CFGS     ; Not configuration space
        BSF         PMCON1,FREE     ; Specify an erase operation
        BSF         PMCON1,WREN     ; Enable writes

Required
Sequence
        MOVLW       55h             ; Start of required sequence to initiate erase
        MOVWF       PMCON2          ; Write 55h
        MOVLW       0AAh            ;
        MOVWF       PMCON2          ; Write AAh
        BSF         PMCON1,WR       ; Set WR bit to begin erase
        NOP                         ; NOP instructions are forced as processor starts
        NOP                         ; row erase of program memory.
                                    ;
                                    ; The processor stalls until the erase process is complete
                                    ; after erase processor continues with 3rd instruction

        BCF         PMCON1,WREN     ; Disable writes
        BSF         INTCON,GIE      ; Enable interrupts
```

FIGURE 16-4: ANALOG INPUT MODEL



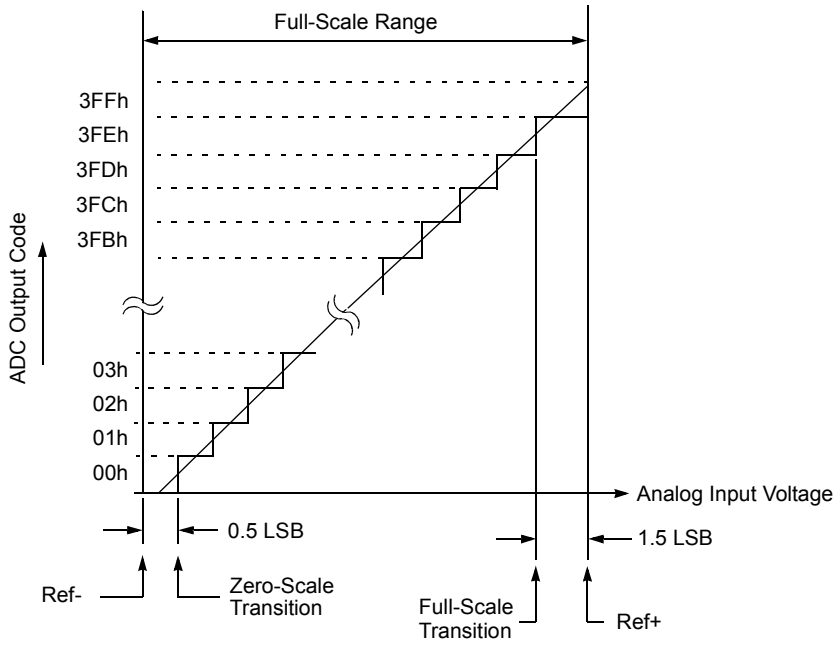


Legend:

CHOLD	= Sample/Hold Capacitance
CPIN	= Input Capacitance
I LEAKAGE	= Leakage current at the pin due to various junctions
RIC	= Interconnect Resistance
RSS	= Resistance of Sampling Switch
SS	= Sampling Switch
VT	= Threshold Voltage

Note 1: Refer to Table 36-4: I/O Ports (parameter D060).

FIGURE 16-5: ADC TRANSFER FUNCTION



18.7 Register Definitions: DAC Control

Long bit name prefixes for the 10-bit DAC peripherals are shown in Table 18-2. Refer to **Section 1.1 "Register and Bit naming conventions"** for more information

TABLE 18-2:

Peripheral	Bit Name Prefix
DAC1	DAC1
DAC2	DAC2
DAC5	DAC5
DAC6(1)	DAC6

Note 1: PIC16(L)F1777/9 only.

REGISTER 18-1: DACxCON0: DAC CONTROL REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **EN:** DAC Enable bit
- 1 = DACx is enabled
- 0 = DACx is disabled

bit 6 **FM:** DAC Reference Format bit
- 1 = DACx reference selection is left justified
- 0 = DACx reference selection is right justified

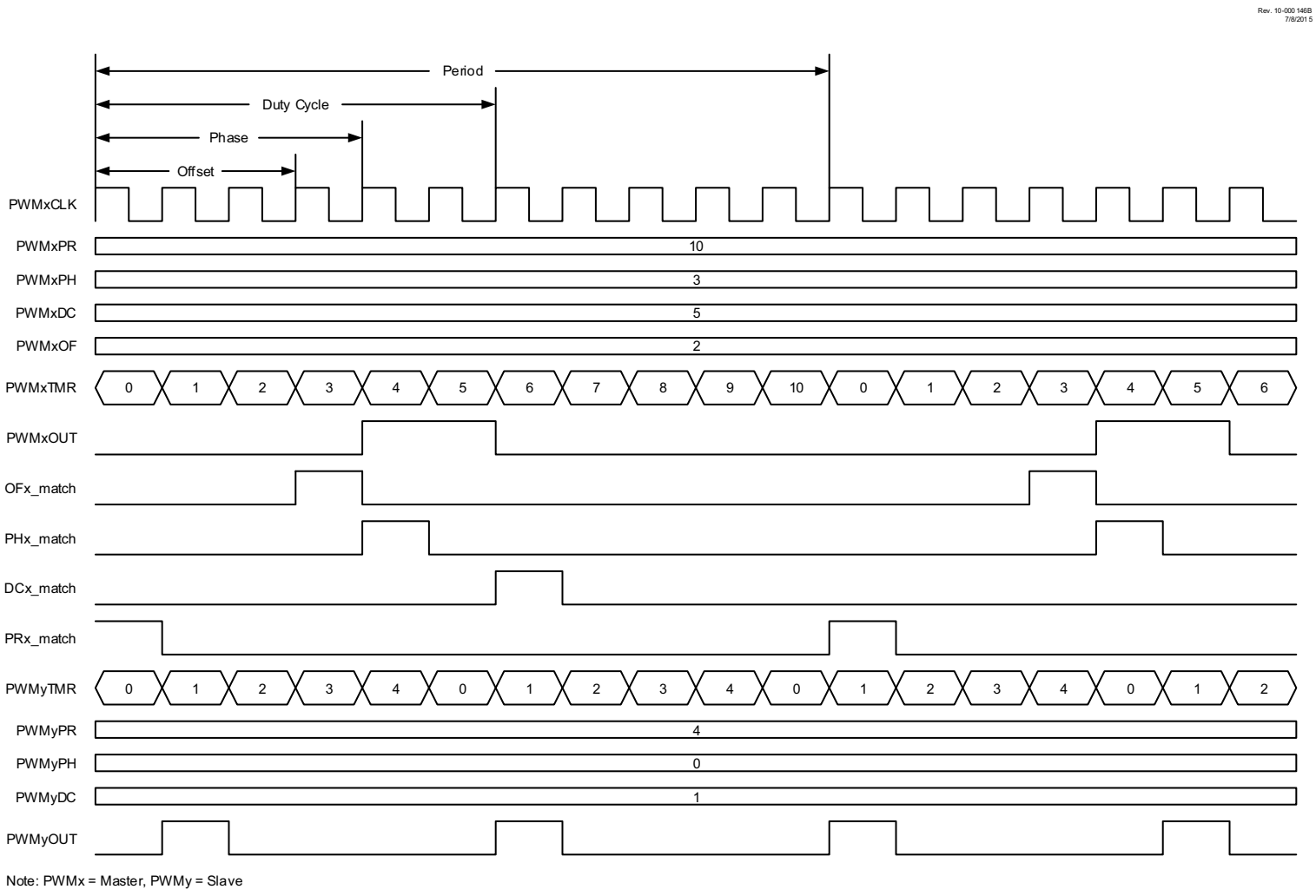
bit 5 **OE1:** DAC Voltage Output Enable bit
- 1 = DACx voltage level is also an output on the DACxOUT1 pin
- 0 = DACx voltage level is disconnected from the DACxOUT1 pin

bit 4 **OE2:** DAC Voltage Output Enable bit
- 1 = DACx voltage level is also an output on the DACxOUT2 pin
- 0 = DACx voltage level is disconnected from the DACxOUT2 pin

bit 3-2 **PSS<1:0>:** DAC Positive Source Select bits
- 11 = DACxREF1+ (DAC5/6) or Reserved (DAC1/2)
- 10 = FVR_buffer2
- 01 = DACxREF0+
- 00 = V_{DD}

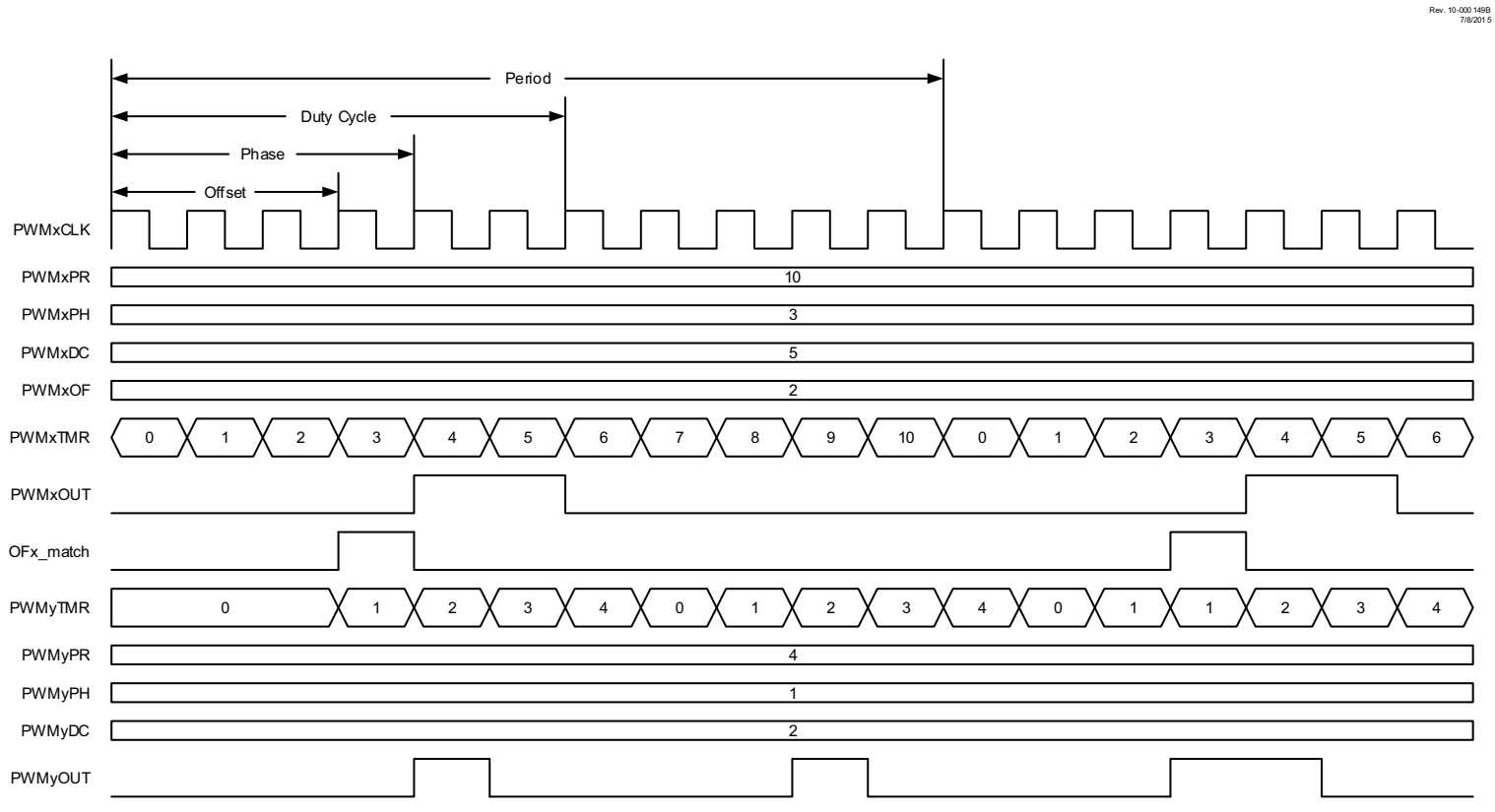
bit 1-0 **NSS<1:0>:** DAC Negative Source Select bit
- 11 = Reserved. Do not use.
- 10 = DACxREF1- (DAC5/6) or Reserved (DAC1/2)
- 01 = DACxREF0-
- 00 = A_{GND} (AV_{SS})

FIGURE 26-8: INDEPENDENT RUN MODE TIMING DIAGRAM



Note: PWMx = Master, PWMy = Slave

FIGURE 26-11: CONTINUOUS SLAVE RUN MODE WITH IMMEDIATE RESET AND SYNC START TIMING DIAGRAM



27.3 Modes of Operation

27.3.1 STEERED PWM MODES

In Steered PWM mode, the PWM signal derived from the input event sources is output as a single phase PWM which can be steered to any combination of the four COG outputs. Output steering takes effect on the instruction cycle following the write to the COGxSTR register.

Synchronous Steered PWM mode is identical to the Steered PWM mode except that changes to the output steering take effect on the first rising event after the COGxSTR register write. Static output data is not synchronized.

Steering mode configurations are shown in Figure 27-2 and Figure 27-3.

Steered PWM and Synchronous Steered PWM modes are selected by setting the MD<2:0> bits of the COGxCON0 register (Register 27-1) to '000' and '001', respectively.

27.3.2 FULL-BRIDGE MODES

In both Forward and Reverse Full-Bridge modes, two of the four COG outputs are active and the other two are inactive. Of the two active outputs, one is modulated by the PWM input signal and the other is on at 100% duty cycle. When the direction is changed, the dead-band time is inserted to delay the modulated output. This gives the unmodulated driver time to shut down, thereby, preventing shoot-through current in the series connected power devices.

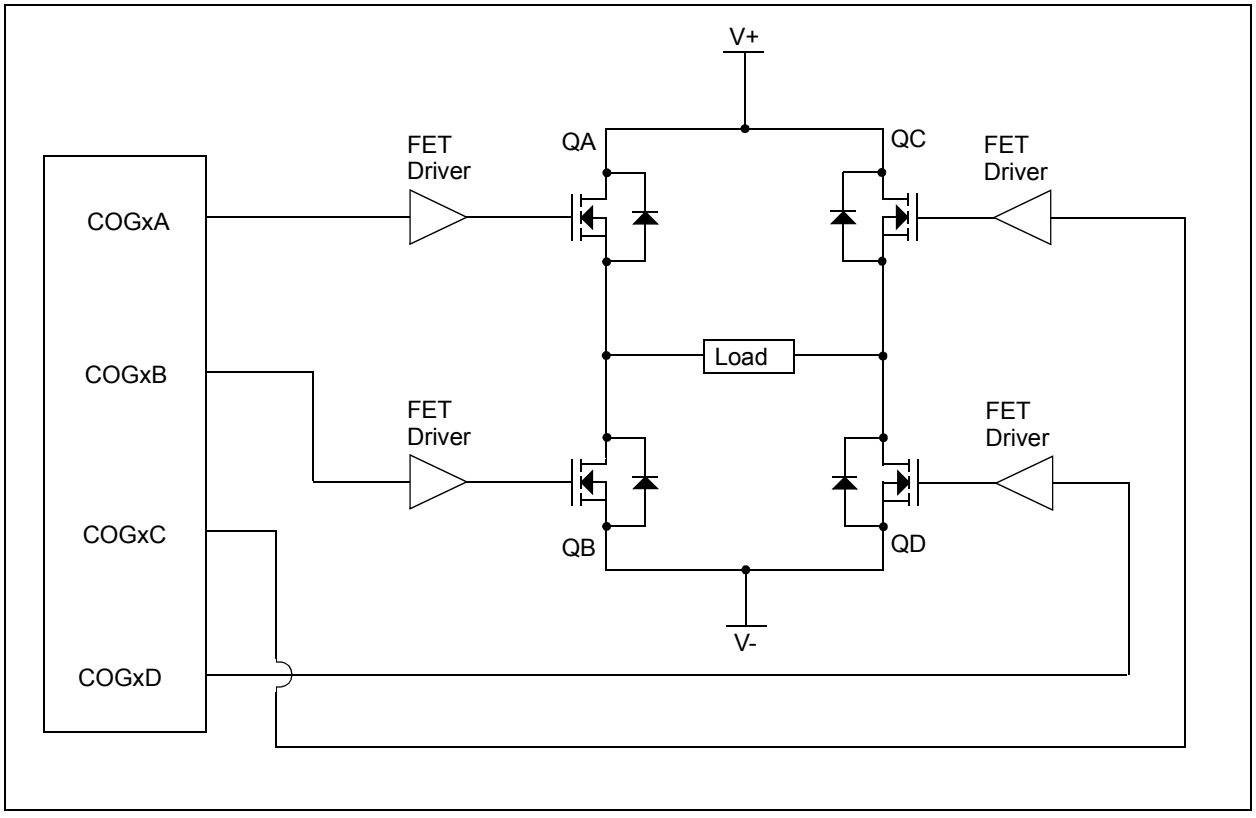
In Forward Full-Bridge mode, the PWM input modulates the COGxD output and drives the COGA output at 100%.

In Reverse Full-Bridge mode, the PWM input modulates the COGxB output and drives the COGxC output at 100%.

The full-bridge configuration is shown in Figure 27-4. Typical full-bridge waveforms are shown in Figure 27-12 and Figure 27-13.

Full-Bridge Forward and Full-Bridge Reverse modes are selected by setting the MD<2:0> bits of the COGxCON0 register to '010' and '011', respectively.

FIGURE 27-1: EXAMPLE OF FULL-BRIDGE APPLICATION



REGISTER 27-5: COGxRSIM0: COG RISING EVENT SOURCE INPUT MODE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
RSIM7	RSIM6	RSIM5	RSIM4	RSIM3	RSIM2	RSIM1	RSIM0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-0 **RSIM<7:0>:** Rising Event Input Source <n> Mode bits(1). See Table 27-5.
RIS<n> = 1:
1 = Source <n> output low-to-high transition will cause a rising event after rising event phase delay
0 = Source <n> output high level will cause an immediate rising event
RIS<n> = 0:
Source <n> output has no effect on rising event

Note 1: Any combination of <n> bits can be selected.

REGISTER 27-6: COGxRSIM1: COG RISING EVENT SOURCE INPUT MODE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
RSIM15	RSIM14	RSIM13	RSIM12	RSIM11	RSIM10	RSIM9	RSIM8
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 15-8 **RSIM<15:8>:** Rising Event Input Source <n> Mode bits(1). See Table 27-5.
RIS<n> = 1:
1 = Source <n> output low-to-high transition will cause a rising event after rising event phase delay
0 = Source <n> output high level will cause an immediate rising event
RIS<n> = 0:
Source <n> output has no effect on rising event

Note 1: Any combination of <n> bits can be selected.

REGISTER 27-16: COGxBLKR: COG RISING EVENT BLANKING COUNT REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
		BLKR<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **BLKR<5:0>:** Rising Event Blanking Count Value bits
= Number of COGx clock periods to inhibit falling event inputs

REGISTER 27-17: COGxBLKF: COG FALLING EVENT BLANKING COUNT REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
		BLKF<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **BLKF<5:0>:** Falling Event Blanking Count Value bits
= Number of COGx clock periods to inhibit rising event inputs

REGISTER 30-2: PRGxCON1: PROGRAMMABLE RAMP GENERATOR CONTROL 1 REGISTER

U-0	U-0	U-0	U-0	U-0	R-0	R/W-0/0	R/W-0/0
—	—	—	—	—	RDY	FPOL	RPOL
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = value depends on configuration bits

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **RDY:** Slope Generator Ready Status bit
1 = PRG is ready
0 = PRG is not ready

bit 1 **FPOL:** Fall Event Polarity Select bit
1 = Set_falling timing input is active-low
0 = Set_falling timing input is active-high

bit 0 **RPOL:** Rise Event Polarity Select bit
1 = Set_rising timing input is active-low
0 = Set_rising timing input is active-high

REGISTER 30-3: PRGxINS: VOLTAGE INPUT SELECT REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	INS<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = value depends on configuration bits

bit 7-4 **Unimplemented:** Read as '0'

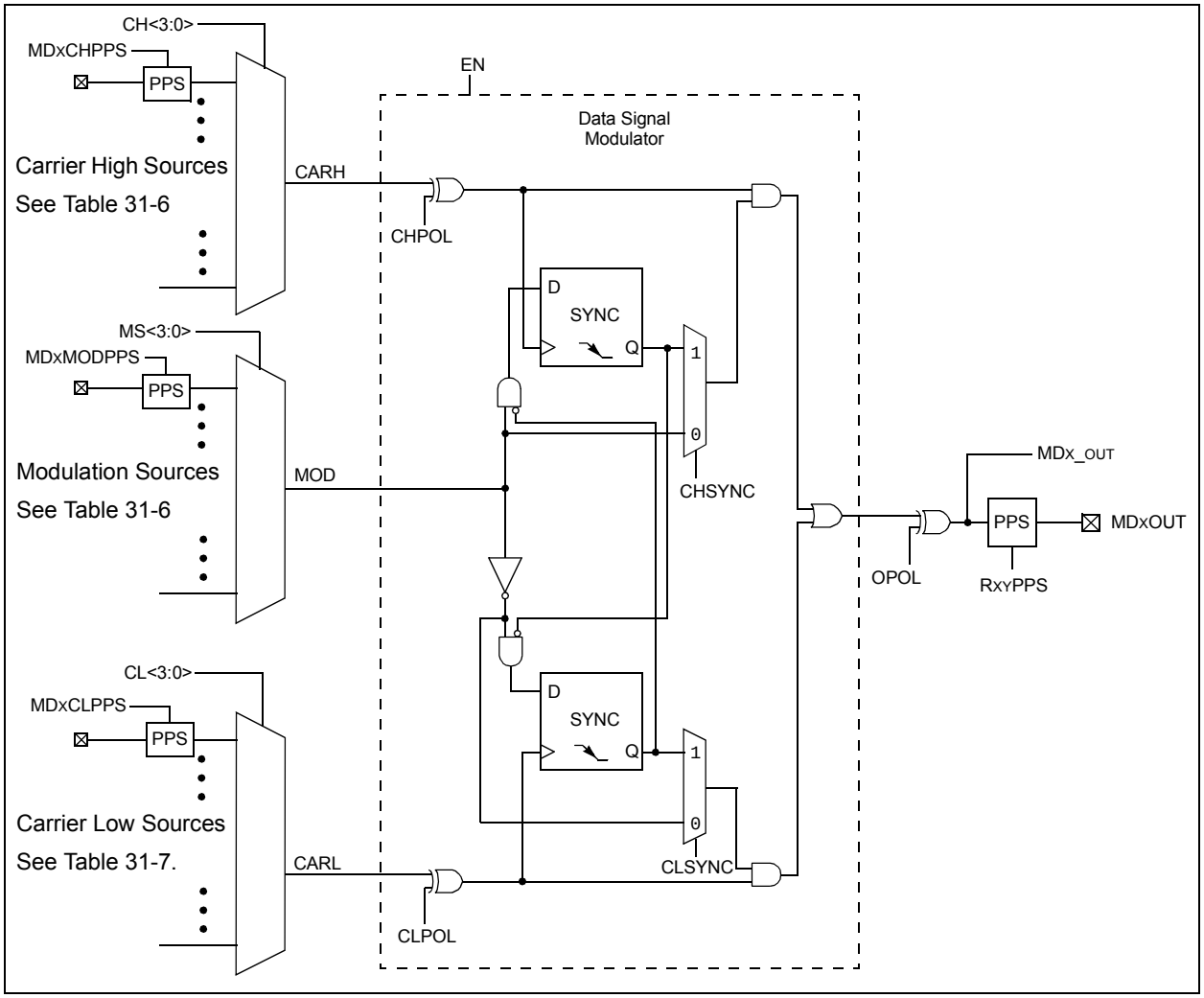
bit 3-0 **INS<3:0>:** Voltage Input Select bits
Selects source of voltage level at which the ramp starts. See Table 30-3.

TABLE 30-3: VOLTAGE INPUT SOURCES

INS<2:0>	PRG1 Voltage Source	PRG2 Voltage Source	PRG3 Voltage Source	PRG4 Voltage Source(2)
1010-1111	Reserved	Reserved	Reserved	Reserved
1001(1)	Switched PRG1IN1/OPA2OUT	Switched PRG1IN1/OPA2OUT	Switched PRG3IN1/OPA4OUT(2)	Switched PRG4IN1/OPA3OUT
1000(1)	Switched PRG1IN0/OPA1OUT	Switched PRG1IN0/OPA1OUT	Switched PRG3IN0/OPA3OUT	Switched PRG4IN0/OPA4OUT
0111	Reserved	Reserved	Reserved	Reserved
0110	DAC4_output	DAC4_output	DAC8_output(2)	DAC8_output
0101	DAC3_output	DAC3_output	DAC7_output	DAC7_output
0100	DAC2_output	DAC2_output	DAC6_output(2)	DAC6_output
0011	DAC1_output	DAC1_output	DAC5_output	DAC5_output
0010	FVR_buffer1	FVR_buffer1	FVR_buffer2	FVR_buffer2
0001	PRG1IN1/OPA2OUT	PRG2IN1/OPA1OUT	PRG3IN1/OPA4OUT(2)	PRG4IN1/OPA3OUT
0000	PRG1IN0/OPA1OUT	PRG2IN0/OPA2OUT	PRG3IN0/OPA3OUT	PRG4IN0/OPA4OUT

Note 1: Input source is switched off when op amp override is forcing tri-state. See **Section 29.3 "Override Control"**.
2: PIC16(L)F1777/9 only.

FIGURE 31-1: SIMPLIFIED BLOCK DIAGRAM OF THE DATA SIGNAL MODULATOR



32.5.2 SLAVE RECEPTION

When the R/$\overline{W}$ bit of a matching received address byte is clear, the R/$\overline{W}$ bit of the SSPxSTAT register is cleared. The received address is loaded into the SSPxBUF register and acknowledged.

When the overflow condition exists for a received address, then not Acknowledge is given. An overflow condition is defined as either bit BF of the SSPxSTAT register is set, or bit SSPOV of the SSPxCON1 register is set. The BOEN bit of the SSPxCON3 register modifies this operation. For more information see Register 32-4.

An MSSP interrupt is generated for each transferred data byte. Flag bit, SSPxIF, must be cleared by software.

When the SEN bit of the SSPxCON2 register is set, SCL will be held low (clock stretch) following each received byte. The clock must be released by setting the CKP bit of the SSPxCON1 register, except sometimes in 10-bit mode. See **Section 32.5.6.2 "10-bit Addressing Mode"** for more detail.

32.5.2.1 7-bit Addressing Reception

This section describes a standard sequence of events for the MSSP module configured as an I^2C slave in 7-bit Addressing mode. Figure 32-14 and Figure 32-15 is used as a visual reference for this description.

This is a step by step process of what typically must be done to accomplish I^2C communication.

1. Start bit detected.
2. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
3. Matching address with R/$\overline{W}$ bit clear is received.
4. The slave pulls SDA low sending an $\overline{ACK}$ to the master, and sets SSPxIF bit.
5. Software clears the SSPxIF bit.
6. Software reads received address from SSPxBUF clearing the BF flag.
7. If SEN = 1; Slave software sets CKP bit to release the SCL line.
8. The master clocks out a data byte.
9. Slave drives SDA low sending an $\overline{ACK}$ to the master, and sets SSPxIF bit.
10. Software clears SSPxIF.
11. Software reads the received byte from SSPxBUF clearing BF.
12. Steps 8-12 are repeated for all received bytes from the master.
13. Master sends Stop condition, setting P bit of SSPxSTAT, and the bus goes idle.

32.5.2.2 7-bit Reception with AHEN and DHEN

Slave device reception with AHEN and DHEN set operate the same as without these options with extra interrupts and clock stretching added after the eighth falling edge of SCL. These additional interrupts allow the slave software to decide whether it wants to $\overline{ACK}$ the receive address or data byte, rather than the hardware. This functionality adds support for PMBus™ that was not present on previous versions of this module.

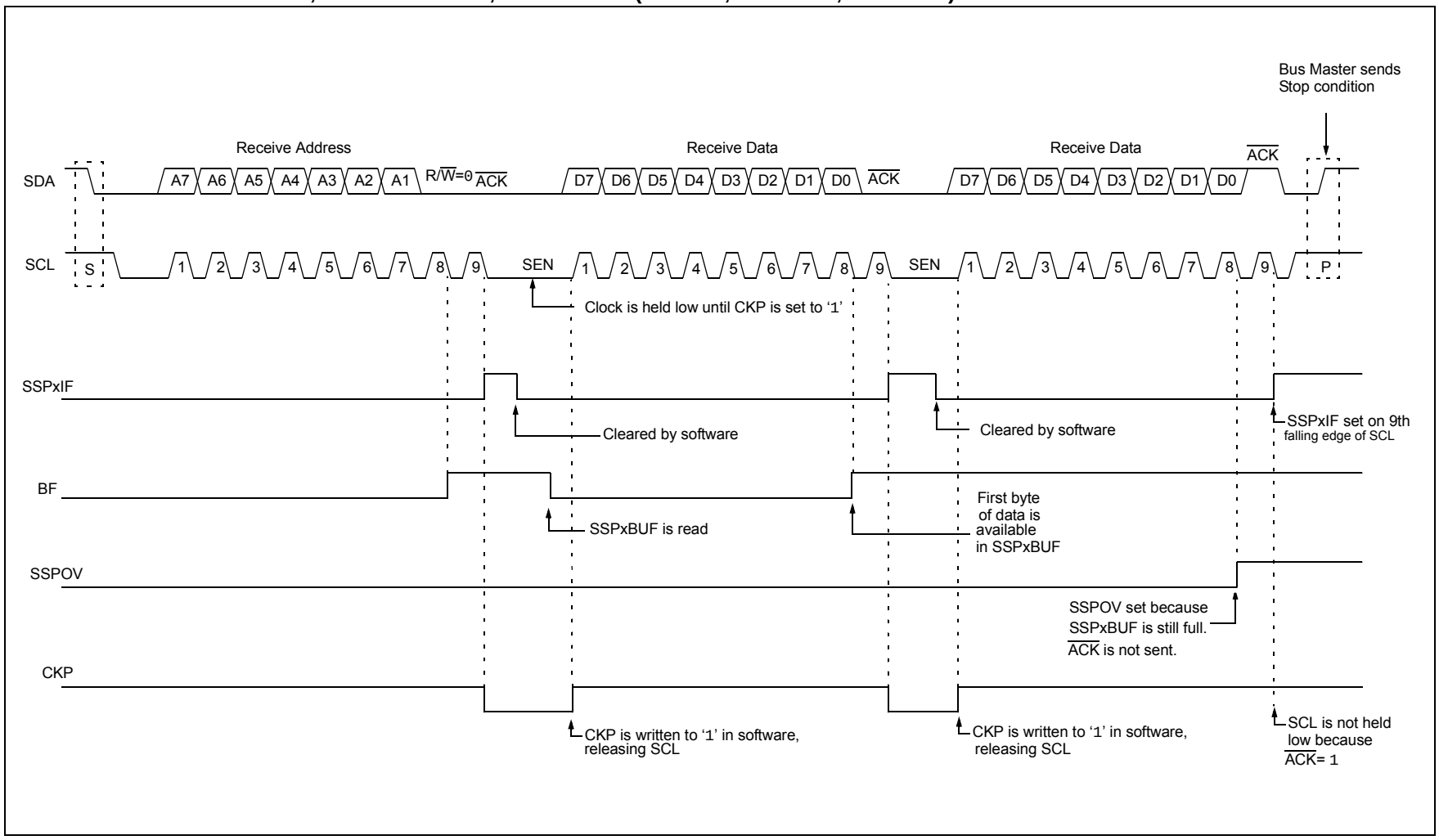
This list describes the steps that need to be taken by slave software to use these options for I^2C communication. Figure 32-16 displays a module using both address and data holding. Figure 32-17 includes the operation with the SEN bit of the SSPxCON2 register set.

1. S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
2. Matching address with R/$\overline{W}$ bit clear is clocked in. SSPxIF is set and CKP cleared after the eighth falling edge of SCL.
3. Slave clears the SSPxIF.
4. Slave can look at the ACKTIM bit of the SSPxCON3 register to determine if the SSPxIF was after or before the $\overline{ACK}$.
5. Slave reads the address value from SSPxBUF, clearing the BF flag.
6. Slave sets $\overline{ACK}$ value clocked out to the master by setting ACKDT.
7. Slave releases the clock by setting CKP.
8. SSPxIF is set after an $\overline{ACK}$, not after a NACK.
9. If SEN = 1 the slave hardware will stretch the clock after the $\overline{ACK}$.
10. Slave clears SSPxIF.

Note: SSPxIF is still set after the ninth falling edge of SCL even if there is no clock stretching and BF has been cleared. Only if NACK is sent to master is SSPxIF not set

11. SSPxIF set and CKP cleared after eighth falling edge of SCL for a received data byte.
12. Slave looks at ACKTIM bit of SSPxCON3 to determine the source of the interrupt.
13. Slave reads the received data from SSPxBUF clearing BF.
14. Steps 7-14 are the same for each received data byte.
15. Communication is ended by either the slave sending an $\overline{ACK}$ = 1, or the master sending a Stop condition. If a Stop is sent and interrupt on Stop detect is disabled, the slave will only know by polling the P bit of the SSTSTAT register.

FIGURE 32-15: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)



34.0 IN-CIRCUIT SERIAL PROGRAMMING™ (ICSP™)

ICSP™ programming allows customers to manufacture circuit boards with unprogrammed devices. Programming can be done after the assembly process, allowing the device to be programmed with the most recent firmware or a custom firmware. Five pins are needed for ICSP™ programming:

- ICSPCLK
- ICSPDAT
- $\overline{MCLR}$/VPP
- VDD
- VSS

In Program/Verify mode the program memory, User IDs and the Configuration Words are programmed through serial communications. The ICSPDAT pin is a bidirectional I/O used for transferring the serial data and the ICSPCLK pin is the clock input. For more information on ICSP™ refer to the **"***PIC16(L)F177X Memory Programming Specification***"** (DS40001792).

34.1 High-Voltage Programming Entry Mode

The device is placed into High-Voltage Programming Entry mode by holding the ICSPCLK and ICSPDAT pins low then raising the voltage on $\overline{MCLR}$/VPP to VIHH.

34.2 Low-Voltage Programming Entry Mode

The Low-Voltage Programming Entry mode allows the PIC® Flash MCUs to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Words is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'.

Entry into the Low-Voltage Programming Entry mode requires the following steps:

1. $\overline{MCLR}$ is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

Once the key sequence is complete, $\overline{MCLR}$ must be held at VIL for as long as Program/Verify mode is to be maintained.

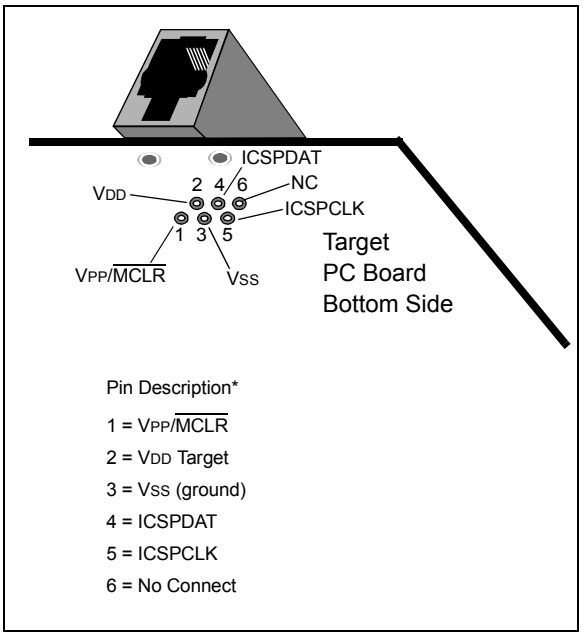
If low-voltage programming is enabled (LVP = 1), the $\overline{MCLR}$ Reset function is automatically enabled and cannot be disabled. See **Section 6.5 "MCLR"** for more information.

The LVP bit can only be reprogrammed to '0' by using the High-Voltage Programming mode.

34.3 Common Programming Interfaces

Connection to a target device is typically done through an ICSP™ header. A commonly found connector on development tools is the RJ-11 in the 6P6C (6-pin, 6-connector) configuration. See Figure 34-1.

FIGURE 34-1: ICD RJ-11 STYLE CONNECTOR INTERFACE



Another connector often found in use with the PICkit™ programmers is a standard 6-pin header with 0.1 inch spacing. Refer to Figure 34-2.

For additional interface recommendations, refer to your specific device programmer manual prior to PCB design.

It is recommended that isolation devices be used to separate the programming pins from other circuitry. The type of isolation is highly dependent on the specific application and may include devices such as resistors, diodes, or even jumpers. See Figure 34-3 for more information.

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

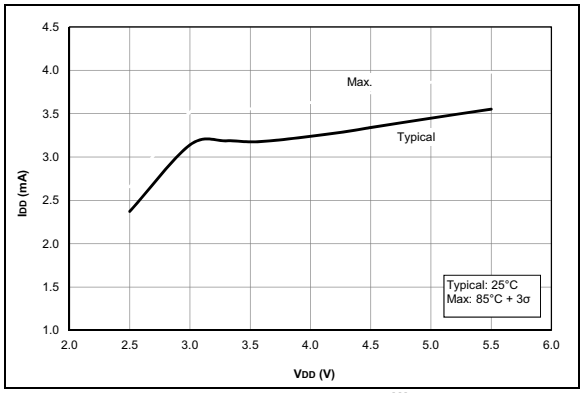


FIGURE 37-31: *IDD, HS Oscillator, 32 MHz (8 MHz + 4x PLL), PIC16F1777/8/9 Only.*

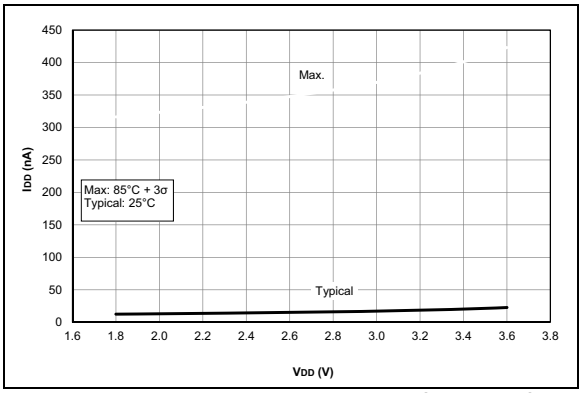


FIGURE 37-32: *IPD Base, LP Sleep Mode, PIC16LF1777/8/9 Only.*

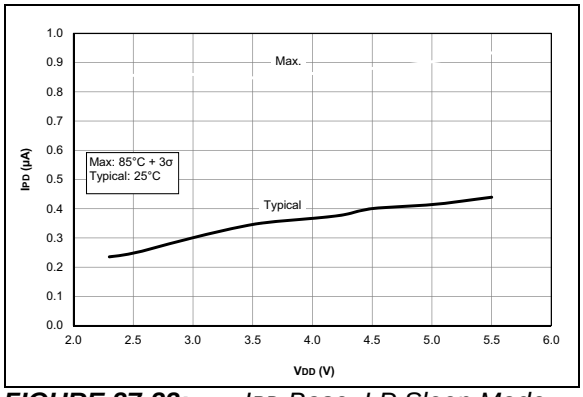


FIGURE 37-33: *IPD Base, LP Sleep Mode (VREGPM = 1), PIC16F1777/8/9 Only.*

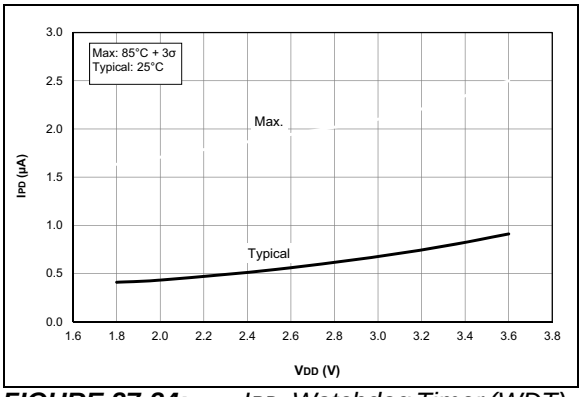


FIGURE 37-34: *IPD, Watchdog Timer (WDT), PIC16LF1777/8/9 Only.*

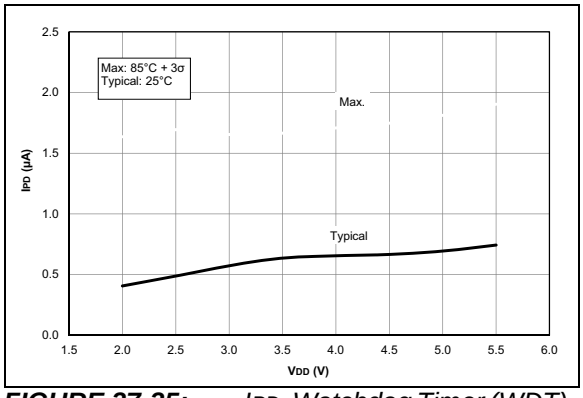


FIGURE 37-35: *IPD, Watchdog Timer (WDT), PIC16F1777/8/9 Only.*

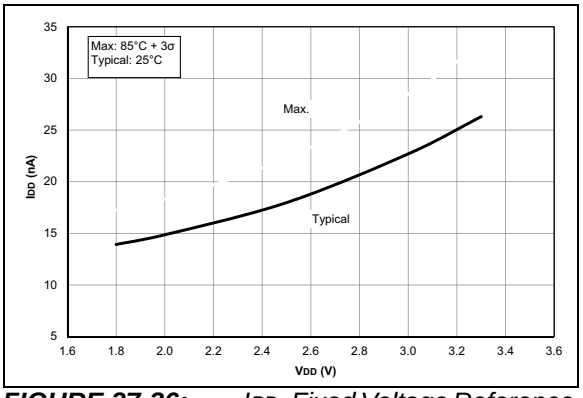


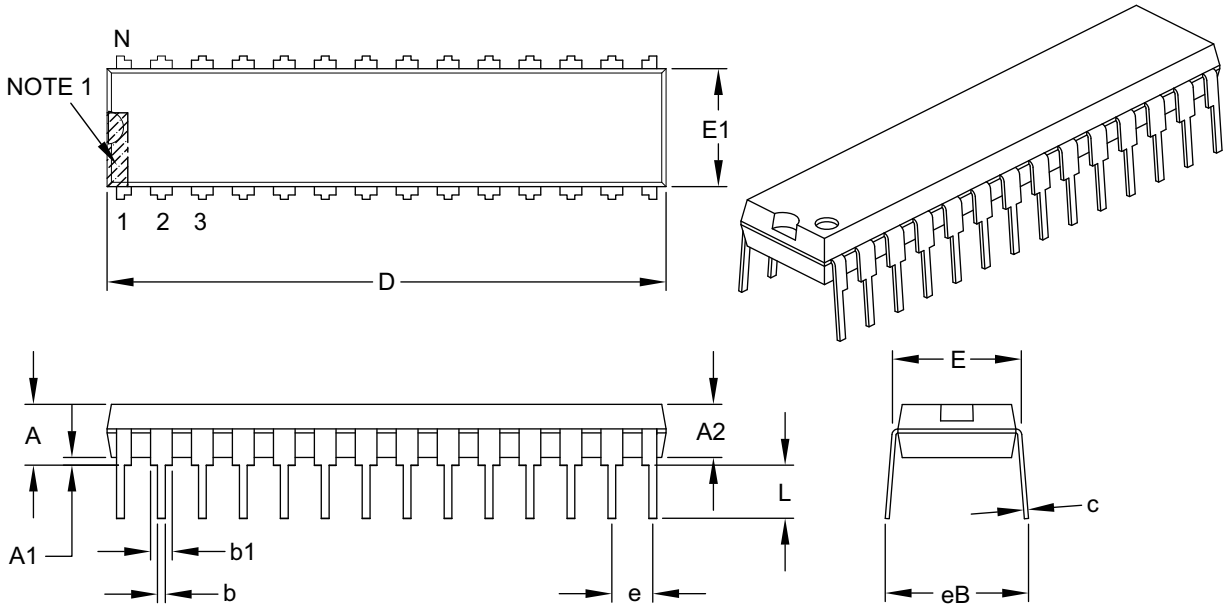
FIGURE 37-36: *IPD, Fixed Voltage Reference (FVR), ADC, PIC16LF1777/8/9 Only.*

39.2 Package Details

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B