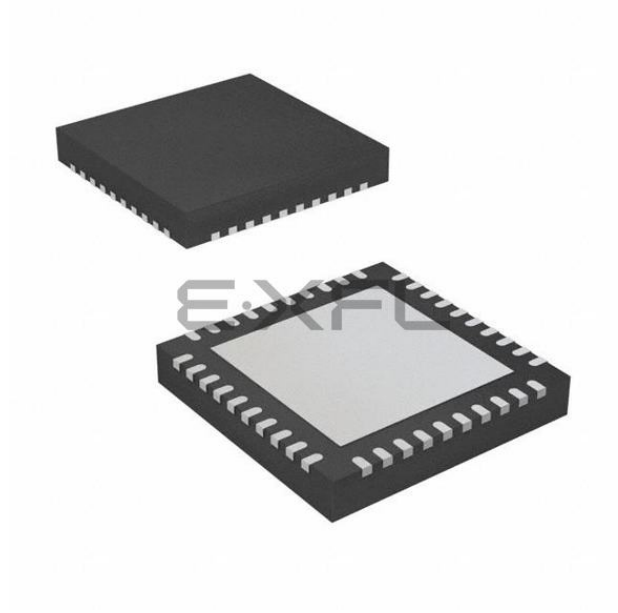


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 28x10b; D/A 4x5b, 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1777-i-mv

TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F1777/9)

I/O	40-Pin PDIP	40-Pin (U)QFN	44-Pin TQFP	44-Pin QFN	ADC	VREF	DAC	Op Amp	Comparator	ZCD	PRG	Timers	PWM	CCP	COG	CLC	Modulator	EUSART	MSSP	Interrupt	Pull-ups	High Current	Basic
RA0	2	17	19	19	AN0	—	—	—	C1IN0- C2IN0- C3IN0- C4IN0- C5IN0- C6IN0- C7IN0- C8IN0-	—	—	—	—	—	—	CLCIN0(1)	—	—	—	IOC	Y	—	—
RA1	3	18	20	20	AN1	—	—	OPA1OUT OPA2IN1+ OPA2IN1-	C1IN1- C2IN1- C3IN1- C4IN1-	—	PRG1IN0 PRG2IN1	—	—	—	—	CLCIN1(1)	—	—	—	IOC	Y	—	—
RA2	4	19	21	21	AN2	DAC1REF0- DAC2REF0- DAC3REF0- DAC4REF0- DAC5REF0- DAC6REF0- DAC7REF0- DAC8REF0-	DAC1OUT1	—	C1IN0+ C2IN0+ C3IN0+ C4IN0+ C5IN0+ C6IN0+ C7IN0+ C8IN0+	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	—
RA3	5	20	22	22	AN3	DAC1REF0+ DAC2REF0+ DAC3REF0+ DAC4REF0+ DAC5REF0+ DAC6REF0+ DAC7REF0+ DAC8REF0+	—	—	C1IN1+	—	—	—	—	—	—	—	MD1CL(1)	—	—	IOC	Y	—	—
RA4	6	21	23	23	—	—	—	OPA1IN0+	—	—	PRG1R(1)	—	—	—	—	—	MD1CH(1)	—	—	IOC	Y	—	—
RA5	7	22	24	24	AN4	—	DAC2OUT1	OPA1IN0-	—	—	PRG1F(1)	—	—	—	—	—	MD1MOD(1)	—	$\overline{SS}$	IOC	Y	—	—
RA6	14	29	31	33	—	—	—	—	C6IN1+	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	OSC2 CLKOUT
RA7	13	28	30	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	OSC1 CLKIN
RB0	33	8	8	9	AN12	—	—	—	C2IN1+	ZCD	—	—	—	CCP8(1)	COG1IN(1)	—	MD4CL(1)	—	—	IOC INT	Y	HIB0	—
RB1	34	9	9	10	AN10	—	—	OPA2OUT OPA1IN1+ OPA1IN1-	C1IN3- C2IN3- C3IN3- C4IN3-	—	PRG2IN0 PRG1IN1 PRG4R(1)	—	—	—	COG2IN(1)	—	MD4CH(1)	—	—	IOC	Y	HIB1	—
RB2	35	10	10	11	AN8	—	DAC3OUT1	OPA2IN0-	—	—	PRG4F(1)	—	—	—	COG3IN(1)	—	MD4MOD(1)	—	—	IOC	Y	—	—
RB3	36	11	11	12	AN9	—	—	OPA2IN0+	C1IN2- C2IN2- C3IN2-	—	—	—	—	—	—	—	MD3CL(1)	—	—	IOC	Y	—	—
RB4	37	12	14	14	AN11	—	—	—	C3IN1+	—	—	—	—	—	—	—	MD3CH(1)	—	—	IOC	Y	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection register.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

1.0 DEVICE OVERVIEW

The PIC16(L)F1777/8/9 are described within this data sheet. See Table 2 for available package configurations.

Figure 1-1 shows a block diagram of the PIC16(L)F1777/8/9 devices. Table 1-2 shows the pinout descriptions.

Refer to Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F1778	PIC16(L)F1777/9
Analog-to-Digital Converter (ADC)		●	●
Fixed Voltage Reference (FVR)		●	●
Zero-Cross Detection (ZCD)		●	●
Temperature Indicator		●	●
Complementary Output Generator (COG)			
	COG1	●	●
	COG2	●	●
	COG3	●	●
	COG4		●
Programmable Ramp Generator (PRG)			
	PRG1	●	●
	PRG2	●	●
	PRG3	●	●
	PRG4		●
10-bit Digital-to-Analog Converter (DAC)			
	DAC1	●	●
	DAC2	●	●
	DAC5	●	●
	DAC6		●
5-bit Digital-to-Analog Converter (DAC)			
	DAC3	●	●
	DAC4	●	●
	DAC7	●	●
	DAC8		●
Capture/Compare/PWM (CCP/ECCP) Modules			
	CCP1	●	●
	CCP2	●	●
	CCP7	●	●
	CCP8		●
Comparators			
	C1	●	●
	C2	●	●
	C3	●	●
	C4	●	●
	C5	●	●
	C6	●	●
	C7		●
	C8		●

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F1778	PIC16(L)F1777/9
Configurable Logic Cell (CLC)			
	CLC1	●	●
	CLC2	●	●
	CLC3	●	●
	CLC4	●	●
Data Signal Modulator (DSM)			
	DSM1	●	●
	DSM2	●	●
	DSM3	●	●
	DSM4		●
Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)			
	EUSART	●	●
Master Synchronous Serial Ports			
	MSSP	●	●
Op Amps			
	OPA1	●	●
	OPA2	●	●
	OPA3	●	●
	OPA4		●
10-bit Pulse-Width Modulator (PWM)			
	PWM3	●	●
	PWM4	●	●
	PWM9	●	●
	PWM10		●
16-bit Pulse-Width Modulator (PWM)			
	PWM5	●	●
	PWM6	●	●
	PWM11	●	●
	PWM12		●
8-bit Timers			
	Timer0	●	●
	Timer2	●	●
	Timer4	●	●
	Timer6	●	●
	Timer8	●	●
16-bit Timers			
	Timer1	●	●
	Timer3	●	●
	Timer5	●	●

TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 5											
28Ch	ODCONA	ODA7	ODA6	ODA5	ODA4	ODA3	ODA2	ODA1	ODA0	0000 0000	0000 0000
28Dh	ODCONB	ODB7	ODB6	ODB5	ODB4	ODB3	ODB2	ODB1	ODB0	0000 0000	0000 0000
28Eh	ODCONC	ODC7	ODC6	ODC5	ODC4	ODC3	ODC2	ODC1	ODC0	0000 0000	0000 0000
28Fh	ODCOND(3)	ODD7	ODD6	ODD5	ODD4	ODD3	ODD2	ODD1	ODD0	0000 0000	0000 0000
290h	ODCONE(3)	—	—	—	—	—	ODE2	ODE1	ODE0	---- -000	--- -000
291h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx	uuuu uuuu
292h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx	uuuu uuuu
293h	CCP1CON	EN	—	OUT	FMT	MODE<3:0>				0-00 0000	0-00 0000
294h	CCP1CAP	—	—	—	—	CTS<3:0>				---- 0000	---- 0000
295h	CCPR2L	Capture/Compare/PWM Register 2 (LSB)								xxxx xxxx	uuuu uuuu
296h	CCPR2H	Capture/Compare/PWM Register 2 (MSB)								xxxx xxxx	uuuu uuuu
297h	CCP2CON	EN	—	OUT	FMT	MODE<3:0>				0-00 0000	0-00 0000
298h	CCP2CAP	—	—	—	—	CTS<3:0>				---- 0000	---- 0000
299h	CCPR7L	Capture/Compare/PWM Register 7 (LSB)								xxxx xxxx	uuuu uuuu
29Ah	CCPR7H	Capture/Compare/PWM Register 7 (MSB)								xxxx xxxx	uuuu uuuu
29Bh	CCP7CON	EN	—	OUT	FMT	MODE<3:0>				0-00 0000	0-00 0000
29Ch	CCP7CAP	—	—	—	—	CTS<3:0>				---- 0000	---- 0000
29Dh	—	Unimplemented								—	—
29Eh	CCPTMRS1	C8TSEL<1:0>(3)		C7TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>		--00 0000	--00 0000
29Fh	CCPTMRS2	P10TSEL<1:0>(3)		P9TSEL<1:0>		P4TSEL<1:0>		P3TSEL<1:0>		--00 0000	--00 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

5.3 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bits of the OSCCON register. The following clock sources can be selected using the SCS bits:

- Default system oscillator determined by FOSC bits in Configuration Words
- Timer1 32 kHz crystal oscillator
- Internal Oscillator Block (INTOSC)

5.3.1 SYSTEM CLOCK SELECT (SCS) BITS

The System Clock Select (SCS) bits of the OSCCON register select the system clock source that is used for the CPU and peripherals.

- When the SCS bits of the OSCCON register = 00, the system clock source is determined by the value of the FOSC<2:0> bits in the Configuration Words.
- When the SCS bits of the OSCCON register = 01, the system clock source is the secondary oscillator.
- When the SCS bits of the OSCCON register = 1x, the system clock source is chosen by the internal oscillator frequency selected by the IRCF<3:0> bits of the OSCCON register. After a Reset, the SCS bits of the OSCCON register are always cleared.

Note:	Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, does not update the SCS bits of the OSCCON register. The user can monitor the OSTS bit of the OSCSTAT register to determine the current system clock source.

When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 5-1.

5.3.2 OSCILLATOR START-UP TIMER STATUS (OSTS) BIT

The Oscillator Start-up Timer Status (OSTS) bit of the OSCSTAT register indicates whether the system clock is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Words, or from the internal clock source. In particular, OSTS indicates that the Oscillator Start-up Timer (OST) has timed out for LP, XT or HS modes. The OST does not reflect the status of the secondary oscillator.

5.3.3 SECONDARY OSCILLATOR

The secondary oscillator is a separate crystal oscillator associated with the Timer1 peripheral. It is optimized for timekeeping operations with a 32.768 kHz crystal connected between the SOSCO and SOSCI device pins.

The secondary oscillator is enabled using the OSCEN control bit in the T1CON register. See **Section 22.0 "Timer1/3/5 Module with Gate Control"** for more information about the Timer1 peripheral.

5.3.4 SECONDARY OSCILLATOR READY (SOSCR) BIT

The user must ensure that the secondary oscillator is ready to be used before it is selected as a system clock source. The Secondary Oscillator Ready (SOSCR) bit of the OSCSTAT register indicates whether the secondary oscillator is ready to be used. After the SOSCR bit is set, the SCS bits can be configured to select the secondary oscillator.

5.3.5 CLOCK SWITCH BEFORE SLEEP

When a clock switch from an old clock to a new clock is requested just prior to entering Sleep mode, it is necessary to confirm that the switch is complete before the sleep instruction is executed. Failure to do so may result in an incomplete switch and consequential loss of the system clock altogether. Clock switching is confirmed by monitoring the clock status bits in the OSCSTAT register. Switch confirmation can be accomplished by sensing that the ready bit for the new clock is set or the ready bit for the old clock is cleared. For example, when switching between the internal oscillator with the PLL and the internal oscillator without the PLL, monitor the PLLR bit. When PLLR is set, the switch to 32 MHz operation is complete. Conversely, when PLLR is cleared the switch from 32 MHz operation to the selected internal clock is complete.

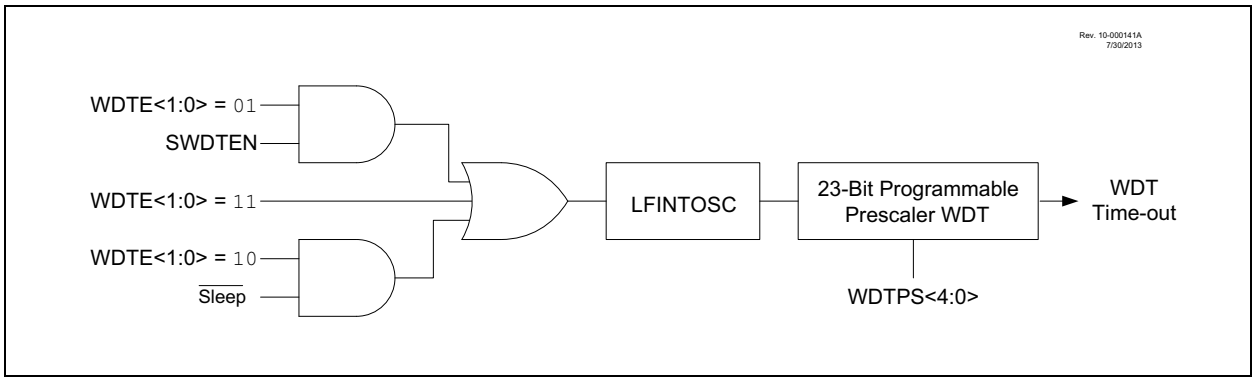
9.0 WATCHDOG TIMER (WDT)

The Watchdog Timer is a system timer that generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events.

The WDT has the following features:

- Independent clock source
- Multiple operating modes
  - WDT is always on
  - WDT is off when in Sleep
  - WDT is controlled by software
  - WDT is always off
- Configurable time-out period is from 1 ms to 256 seconds (nominal)
- Multiple Reset conditions
- Operation during Sleep

FIGURE 9-1: WATCHDOG TIMER BLOCK DIAGRAM



REGISTER 13-12: IOCEF: INTERRUPT-ON-CHANGE PORTE FLAG REGISTER

U-0	U-0	U-0	U-0	R/W/HS-0/0	U-0	U-0	U-0
—	—	—	—	IOCEF3	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **IOCEF3:** Interrupt-on-Change PORTE Flag bits
1 = An enabled change was detected on the associated pin.
Set when IOCEPx = 1 and a rising edge was detected on REx, or when IOCENx = 1 and a falling edge was detected on REx.
0 = No change was detected, or the user cleared the detected change.

bit 2-0 **Unimplemented:** Read as '0'

TABLE 13-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPT-ON-CHANGE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	177
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	182
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—	187
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	132
IOCAF	IOCAF7	IOCAF6	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	216
IOCAN	IOCAN7	IOCAN6	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	215
IOCAP	IOCAP7	IOCAP6	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	215
IOCBF	IOCBF7	IOCBF6	IOCBF5	IOCBF4	IOCBF3	IOCBF2	IOCBF1	IOCBF0	217
IOCBN	IOCBN7	IOCBN6	IOCBN5	IOCBN4	IOCBN3	IOCBN2	IOCBN1	IOCBN0	216
IOCBP	IOCBP7	IOCBP6	IOCBP5	IOCBP4	IOCBP3	IOCBP2	IOCBP1	IOCBP0	216
IOCCF	IOCCF7	IOCCF6	IOCCF5	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0	218
IOCCN	IOCCN7	IOCCN6	IOCCN5	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0	218
IOCCP	IOCCP7	IOCCP6	IOCCP5	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0	218
IOCEP	—	—	—	—	IOCEP3	—	—	—	219
IOCEN	—	—	—	—	IOCEN3	—	—	—	219
IOCEF	—	—	—	—	IOCEF3	—	—	—	220
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	176
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	181
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	186
TRISE	—	—	—	—	—(1)	TRISE2(2)	TRISE1(2)	TRISE0(2)	199

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by interrupt-on-change.

Note 1: Unimplemented, read as '1'.

2: Unimplemented on PIC16(L)F1778.

16.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- Port configuration
- Channel selection
- ADC voltage reference selection
- ADC conversion clock source
- Interrupt control
- Result formatting

16.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. Refer to **Section 11.0 "I/O Ports"** for more information.

Note:	Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

16.1.2 CHANNEL SELECTION

There are up to 27 channel selections available:

- AN<4:0> pins (PIC16(L)F1778 only)
- AN<11:8> pins (PIC16(L)F1778 only)
- AN<27:0> pins (PIC16(L)F1777/9 only)
- Temperature Indicator
- DAC1_output and DAC3_output
- DAC2_output and DAC4_output (PIC16(L)F1777/9 only)
- FVR_buffer1

The CHS bits of the ADCON0 register (Register 16-1) determine which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion. Refer to **Section 16.2 "ADC Operation"** for more information.

16.1.3 ADC POSITIVE VOLTAGE REFERENCE

The ADPREF bits of the ADCON1 register provide control of the positive voltage reference. The positive voltage reference can be:

- V_{REF}+ pin
- V_{DD}
- FVR 2.048V
- FVR 4.096V (Not available on LF devices)
- V_{SS}

See **Section 16.0 "Analog-to-Digital Converter (ADC) Module"** for more details on the Fixed Voltage Reference.

16.1.4 ADC NEGATIVE VOLTAGE REFERENCE

The ADNREF bit of the ADCON1 register provides control of the negative voltage reference. The negative voltage reference can be:

- V_{REF}- pin
- V_{SS}

16.1.5 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS bits of the ADCON1 register. There are seven possible clock options:

- F_{OSC}/2
- F_{OSC}/4
- F_{OSC}/8
- F_{OSC}/16
- F_{OSC}/32
- F_{OSC}/64
- FRC (internal RC oscillator)

The time to complete one bit conversion is defined as T_{AD}. One full 10-bit conversion requires 11.5 T_{AD} periods as shown in Figure 16-2.

For correct conversion, the appropriate T_{AD} specification must be met. Refer to Table 36-16: ADC Conversion Requirements for more information. Table 16-1 gives examples of appropriate ADC clock selections.

Note:	Unless using the FRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.

REGISTER 18-4: DACLD: DAC BUFFER LOAD REGISTER

U-0	U-0	U-0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
—	—	DAC6LD(1)	DAC5LD	—	—	DAC2LD	DAC1LD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = value depends on configuration bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **DAC6LD:** DAC6 Double Buffer Load bit(1)
- 1 = DAC6REFHL:DAC6REFL values are transfered to the double buffer. Bit is cleared automatically by hardware.
- 0 = DAC6REFHL:DAC6REFL double buffers remain unchanged.

bit 4 **DAC5LD:** DAC5 Double Buffer Load bit
- 1 = DAC5REFHL:DAC5REFL values are transfered to the double buffer. Bit is cleared automatically by hardware.
- 0 = DAC5REFHL:DAC5REFL double buffers remain unchanged.

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **DAC2LD:** DAC2 Double Buffer Load bit
- 1 = DAC2REFHL:DAC2REFL values are transfered to the double buffer. Bit is cleared automatically by hardware.
- 0 = DAC2REFHL:DAC2REFL double buffers remain unchanged.

bit 0 **DAC1LD:** DAC1 Double Buffer Load bit
- 1 = DAC1REFHL:DAC1REFL values are transfered to the double buffer. Bit is cleared automatically by hardware.
- 0 = DAC1REFHL:DAC1REFL double buffers remain unchanged.

Note 1: PIC16LF1777/9 only.

TABLE 18-3: SUMMARY OF REGISTERS ASSOCIATED WITH THE DACx MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
DAC1CON0	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC2CON0	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC5CON0	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC6CON0(1)	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC1REFH	REF<9:x> (x Depends on FM bit)								250
DAC2REFH	REF<9:x> (x Depends on FM bit)								250
DAC5REFH	REF<9:x> (x Depends on FM bit)								250
DAC6REFH(1)	REF<9:x> (x Depends on FM bit)								250
DAC1REFL	REF<x-1:0> (x Depends on FM bit)								250
DAC2REFL	REF<x-1:0> (x Depends on FM bit)								250
DAC5REFL	REF<x-1:0> (x Depends on FM bit)								250
DAC6REFL(1)	REF<x-1:0> (x Depends on FM bit)								250
DACLD	—	—	—	DAC5LD	—	—	DAC2LD	DAC1LD	251

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used with the DACx module.

Note 1: PIC16LF1777/9 only.

REGISTER 19-4: CMxPSEL: COMPARATOR Cx POSITIVE CHANNEL SELECT REGISTER 1

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	PCH<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **PCH<3:0>:** Comparator Positive Input Channel Select bits
CxVP connects to input source indicated by Table 19-5: Positive Input Sources

TABLE 19-5: POSITIVE INPUT SOURCES

PCH<3:0>	C1, C2, C3, C4	C5, C6, C7(1), C8(1)
1111	Reserved. Do not use	Reserved. Do not use
1110	Reserved. Do not use	Reserved. Do not use
1101	Reserved. Do not use	Reserved. Do not use
1100	Reserved. Do not use	Reserved. Do not use
1011	Reserved. Do not use	Reserved. Do not use
1010	Reserved. Do not use	Reserved. Do not use
1001	AGND	AGND
1000	DAC4_out	DAC8_out(1)
0111	DAC3_out	DAC7_out
0110	DAC2_out	DAC6_out(1)
0101	DAC1_out	DAC5_out
0100	PRG2_out	PRG4_out(1)
0011	PRG1_out	PRG3_out
0010	FVR_Buffer2	FVR_Buffer2
0001	CxIN1+ pin	CxIN1+ pin
0000	CxIN0+ pin	CxIN0+ pin

Note 1: PIC16(L)F1777/9 only.

24.0 CAPTURE/COMPARE/PWM MODULES

The Capture/Compare/PWM module is a peripheral which allows the user to time and control different events, and to generate Pulse-Width Modulation (PWM) signals. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate Pulse-Width Modulated signals of varying frequency and duty cycle.

TABLE 24-1: AVAILABLE CCP MODULES

Device	CCP1	CCP2	CCP7	CCP8
PIC16(L)F1778	●	●	●	
PIC16(L)F1777/9	●	●	●	●

Note 1: In devices with more than one CCP module, it is very important to pay close attention to the register names used. A number placed after the module acronym is used to distinguish between separate modules. For example, the CCP1CON and CCP2CON control the same operational aspects of two completely different CCP modules.

2: Throughout this section, generic references to a CCP module in any of its operating modes may be interpreted as being equally applicable to a CCPx module. Register names, module signals, I/O pins, and bit names may use the generic designator 'x' to indicate the use of a numeral to distinguish a particular module, when required.

24.1 Capture Mode

The Capture mode function described in this section is available and identical for all CCP modules.

Capture mode makes use of the 16-bit Timer1 resource. When an event occurs on the CCPx input, the 16-bit CCPRxH:CCPRxL register pair captures and stores the 16-bit value of the TMR1H:TMR1L register pair, respectively. An event is defined as one of the following and is configured by the MODE<3:0> bits of the CCPxCON register:

- Every edge (rising or falling)
- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

The CCPx capture input signal is configured by the CTS bits of the CCPxCAP register with the following options:

- CCPx pin
- Comparator 1 output (C1_OUT_sync)
- Comparator 2 output (C2_OUT_sync)
- Comparator 7 output (C7_OUT_sync)
- Comparator 8 output (C8_OUT_sync) (PIC16(L)F1777/9 only)
- LC2_output
- LC3_output
- Interrupt-on-change interrupt trigger (IOC_interrupt)

When a capture is made, the Interrupt Request Flag bit CCPxIF of the PIRx register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPRxH:CCPRxL register pair is read, the old captured value is overwritten by the new captured value.

Figure 24-1 shows a simplified diagram of the capture operation.

24.1.1 CCP PIN CONFIGURATION

In Capture mode, select the interrupt source using the CTS bits of the CCPxCAP register. If the CCPx pin is chosen, it should be configured as an input by setting the associated TRIS control bit.

Note: If the CCPx pin is configured as an output, a write to the port can cause a capture condition.

28.6 Register Definitions: CLC Control

Long bit name prefixes for the CLC peripherals are shown in Table 28-3. Refer to **Section 1.1 "Register and Bit naming conventions"** for more information

TABLE 28-3:

Peripheral	Bit Name Prefix
CLC1	LC1
CLC2	LC2
CLC3	LC3
CLC4	LC4

REGISTER 28-1: CLCxCON: CONFIGURABLE LOGIC CELL CONTROL REGISTER

R/W-0/0	U-0	R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EN	—	OUT	INTP	INTN	MODE<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **EN:** Configurable Logic Cell Enable bit
- 1 = Configurable logic cell is enabled and mixing input signals
- 0 = Configurable logic cell is disabled and has logic zero output

bit 6 **Unimplemented:** Read as '0'

bit 5 **OUT:** Configurable Logic Cell Data Output bit
Read-only: logic cell output data, after POL; sampled from lcx_out wire.

bit 4 **INTP:** Configurable Logic Cell Positive Edge Going Interrupt Enable bit
- 1 = CLCxIF will be set when a rising edge occurs on lcx_out
- 0 = CLCxIF will not be set

bit 3 **INTN:** Configurable Logic Cell Negative Edge Going Interrupt Enable bit
- 1 = CLCxIF will be set when a falling edge occurs on lcx_out
- 0 = CLCxIF will not be set

bit 2-0 **MODE<2:0>:** Configurable Logic Cell Functional Mode bits
- 111 = Cell is 1-input transparent latch with S and R
- 110 = Cell is J-K flip-flop with R
- 101 = Cell is 2-input D flip-flop with R
- 100 = Cell is 1-input D flip-flop with S and R
- 011 = Cell is S-R latch
- 010 = Cell is 4-input AND
- 001 = Cell is OR-XOR
- 000 = Cell is AND-OR

REGISTER 29-3: OPAxNCHS: OP AMP NEGATIVE CHANNEL SOURCE SELECT REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	NCH<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **NCH<3:0>:** Op Amp Inverting Input Channel Selection bits
See Table 29-4: Inverting Input Sources

TABLE 29-4: INVERTING INPUT SOURCES

NCH<3:0>	OPA1	OPA2	OPA3	OPA4(1)
1111	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use
1110	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use
1101	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use
1100	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use
1011	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use
1010	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use
1001	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use
1000	PRG2_out	PRG2_out	PRG4_out(1)	PRG4_out
0111	PRG1_out	PRG1_out	PRG3_out	PRG3_out
0110	FVR_Buffer1	FVR_Buffer1	FVR_Buffer2	FVR_Buffer2
0101	DAC4_out	DAC4_out	DAC8_out(1)	DAC8_out
0100	DAC3_out	DAC3_out	DAC7_out	DAC7_out
0011	DAC2_out	DAC2_out	DAC6_out(1)	DAC6_out
0010	DAC1_out	DAC1_out	DAC5_out	DAC5_out
0001	OPA1IN1-	OPA2IN1-	OPA3IN1-(1)	OPA4IN1-
0000	OPA1IN0-	OPA2IN0-	OPA3IN0-	OPA3IN0-

Note 1: PIC16(L)F1777/9 only.

sensitive timing inputs that occur during, and extend beyond, the one-shot period will be suspended until the end of the one-shot time.

30.1.2.2 Rising Ramp

The Rising Ramp mode is identical to the Slope Compensation mode except that the ramps have a rising slope instead of a falling slope. One side of the internal capacitor is connected to the voltage input source and the other side is connected to the internal current source. The internal current source charges this capacitor at a programmable rate. As the capacitor charges, the capacitor voltage is added to the voltage source, producing a linear voltage rise at the required rate (see Figure 30-5). The ramp terminates and the capacitor is discharged when the set_falling timing input goes true. The next ramp starts when the set_rising timing input goes true.

Enabling the optional one-shot by setting the OS bit of the PRGxCON0 register ensures that the capacitor is fully discharged by overriding the set_rising timing input and holding the shorting switch closed for at least the one-shot period, typically 50 ns. Edge sensitive timing inputs that occur during the one-shot period will be ignored. Level sensitive timing inputs that occur during, and extend beyond, the one-shot period will be suspended until the end of the one-shot time.

30.2 Enable, Ready, Go

The EN bit of the PRGxCON0 register enables the analog circuitry including the current sources. This permits preparing the PRG module for use and allowing it to become stable before putting it into operation. When the EN bit is set then the timing inputs are enabled so that initial ramp action can be determined before the GO bit is set. The capacitor shorting switch is closed when the EN bit is set and remains closed while the GO bit is zero.

The RDY bit of the PRGxCON1 register indicates that the analog circuits and current sources are stable.

The GO bit of the PRGxCON0 register enables the switch control circuits, thereby putting the PRG into operation. The GO transition from cleared to set triggers the one-shot, thereby extending the capacitor shorting switch closure for the one-shot period.

To ensure predictable operation, set the EN bit first then wait for the RDY bit to go high before setting the GO bit.

30.3 Independent Set_rising and Set_falling Timing Inputs

The timing inputs determine when the ramp starts and stops. In the Alternating Rising/Falling mode the ramp rises when the set_rising input goes true and falls when the set_falling input goes true. In the Slope Compensation and Rising Ramp modes the capacitor is discharged when the set_falling timing input goes true and the ramp starts when the set_rising timing input goes true. The set_falling input dominates the set_rising input.

30.4 Level and Edge Timing Sensitivity

The set_rising and set_falling timing inputs can be independently configured as either level or edge sensitive.

Level sensitive operation is useful when it is necessary to detect a timing input true state after an overriding condition ceases. For example, level sensitivity is useful for capacitor generated timing inputs that may be suppressed by the overriding action of the one-shot. With level sensitivity a capacitor output that changes during the one-shot period will be detected at the end of the one-shot time. With edge sensitivity the change would be ignored.

Edge sensitive operation is useful for periodic timing inputs such as those generated by PWMs and clocks. The duty cycle of a level sensitive periodic signal may interfere with the other timing input. Consider an Alternating Ramp mode with a level sensitive 50% PWM as the set_rising timing source and a level sensitive comparator as the set_falling timing source. If the comparator output reverses the ramp while the PWM signal is still high then the ramp will improperly reverse again when the comparator signal goes low. That same scenario with the set_rising timing input set for edge sensitivity would properly change the ramp output to rising only on the rising edge of the PWM signal.

Set_rising and set_falling timing input edge sensitivity is selected with the respective REDG and FEDG bits of the PRGxCON1 register.

30.5 One-Shot Minimum Timing

The one-shot timer ensures a minimum capacitor discharge time in the Slope Compensation and Rising Ramp modes, and a minimum rising or falling ramp duration in the Alternating Ramp mode. Setting the OS bit of the PRGxCON0 register enables the one-shot timer.

30.6 DAC Voltage Sources

When using any of the DACs as the voltage source expect a voltage offset equal to the current setting times the DAC equivalent resistance. This will be a constant offset in the Slope Compensation and Ramp modes and a positive/negative step offset in the Alternating mode. To avoid this limitation, feed the DAC output to the PRG input through one of the op amps set for unity gain.

30.7 Operation During Sleep

The RG module is unaffected by Sleep.

30.8 Effects of a Reset

The RG module resets to a disabled condition.

TABLE 32-3: SUMMARY OF REGISTERS ASSOCIATED WITH I^2C OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	177
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	182
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—	187
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	132
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	133
PIE2	OSFIE	C2IE	C1IE	COG1IE	BCL1IE	C4IE	C3IE	CCP2IE	134
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	139
PIR2	OSFIF	C2IF	C1IF	COG1IF	BCL1IF	C4IF	C3IF	CCP2IF	140
RxyPPS	—	—	RxyPPS<5:0>						205
SSPCLKPPS	—	—	SSPCLKPPS<5:0>						205, 207
SSPDATPPS	—	—	SSPDATPPS<5:0>						205, 207
SSPSSPPS	—	—	SSPSSPPS<5:0>						205, 207
SSP1ADD	ADD<7:0>								492
SSP1BUF	Synchronous Serial Port Receive Buffer/Transmit Register								444*
SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				489
SSP1CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	490
SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	491
SSP1MSK	MSK<7:0>								492
SSP1STAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	488
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	176
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	181
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	186

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by the MSSP module in I^2C mode.

* Page provides register information.

TABLE 33-3: BAUD RATE FORMULAS

Configuration Bits			BRG/EUSART Mode	Baud Rate Formula
SYNC	BRG16	BRGH		
0	0	0	8-bit/Asynchronous	FOSC/[64 (n+1)]
0	0	1	8-bit/Asynchronous	FOSC/[16 (n+1)]
0	1	0	16-bit/Asynchronous	
0	1	1	16-bit/Asynchronous	FOSC/[4 (n+1)]
1	0	x	8-bit/Synchronous	
1	1	x	16-bit/Synchronous	

Legend: x = Don't care, n = value of SPxBRGH:SPxBRGL register pair.

TABLE 33-4: SUMMARY OF REGISTERS ASSOCIATED WITH THE BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BAUD1CON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	505
RC1STA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	504
SP1BRGL	SP1BRG<7:0>								506
SP1BRGH	SP1BRG<15:8>								506
TX1STA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	503

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for the Baud Rate Generator.

* Page provides register information.

TABLE 36-3: POWER-DOWN CURRENTS (I_{PD})(1,2) (CONTINUED)

PIC16LF1777/8/9		Operating Conditions: (unless otherwise stated) Low-Power Sleep Mode						
PIC16F1777/8/9		Low-Power Sleep Mode, VREGPM = 1						
Param No.	Device Characteristics	Min.	Typ†	Max. +85°C	Max. +125°C	Units	Conditions	
							V_{DD}	Note
D029		—	0.05	2	9	μA	1.8	ADC Current **(Note 3)**, no conversion in progress
		—	0.08	3	10	μA	3.0	
D029		—	0.3	4	12	μA	2.3	ADC Current **(Note 3)**, no conversion in progress
		—	0.4	5	13	μA	3.0	
		—	0.5	7	16	μA	5.0	
D030		—	250	—	—	μA	1.8	ADC Current **(Note 3)**, conversion in progress
		—	250	—	—	μA	3.0	
D030		—	280	—	—	μA	2.3	ADC Current **(Note 3)**, conversion in progress
		—	280	—	—	μA	3.0	
		—	280	—	—	μA	5.0	
D031		—	250	650	—	μA	3.0	Op Amp (High power)
D031		—	250	650	—	μA	3.0	Op Amp (High power)
		—	350	850	—	μA	5.0	
D032		—	250	600	—	μA	1.8	Comparator, CxSP = 0
		—	300	650	—	μA	3.0	
D032		—	280	600	—	μA	2.3	Comparator, CxSP = 0 VREGPM = 0
		—	300	650	—	μA	3.0	
		—	310	650	—	μA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base I_{PD} and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base I_{DD} or I_{PD} current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{SS}.

3: ADC clock source is FRC.

TABLE 36-4: I/O PORTS (CONTINUED) (CONTINUED)

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
		Capacitive Loading Specs on Output Pins					
D101*	COSC2	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101A*	CIO	All I/O pins	—	—	50	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in EXTRC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: Including OSC2 in CLKOUT mode.

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

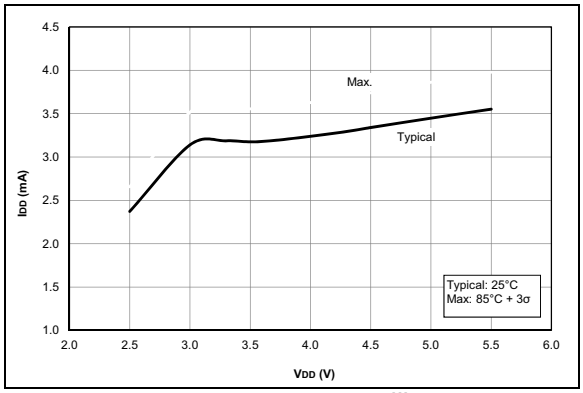


FIGURE 37-31: *IDD, HS Oscillator, 32 MHz (8 MHz + 4x PLL), PIC16F1777/8/9 Only.*

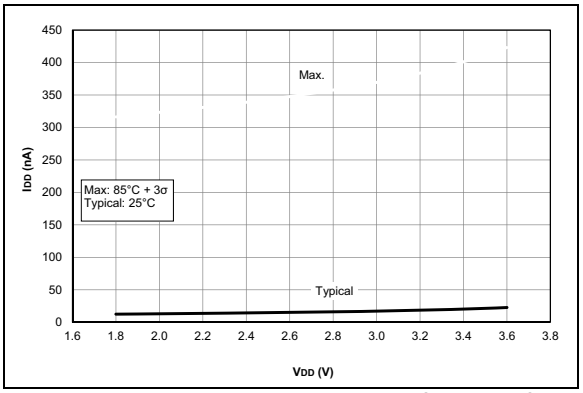


FIGURE 37-32: *IPD Base, LP Sleep Mode, PIC16LF1777/8/9 Only.*

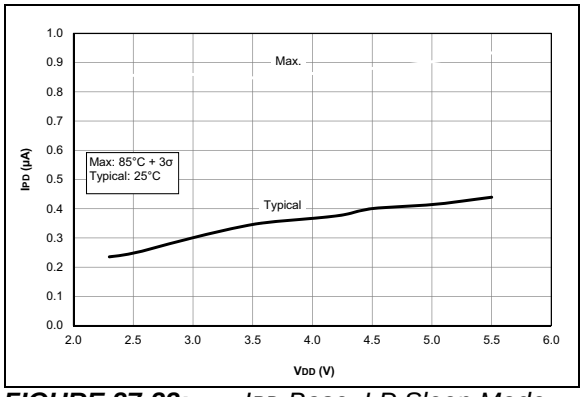


FIGURE 37-33: *IPD Base, LP Sleep Mode (VREGPM = 1), PIC16F1777/8/9 Only.*

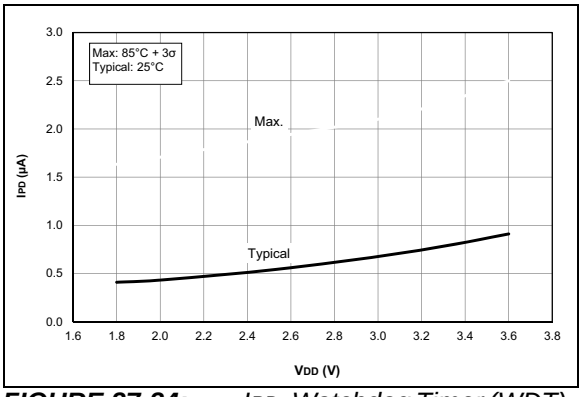


FIGURE 37-34: *IPD, Watchdog Timer (WDT), PIC16LF1777/8/9 Only.*

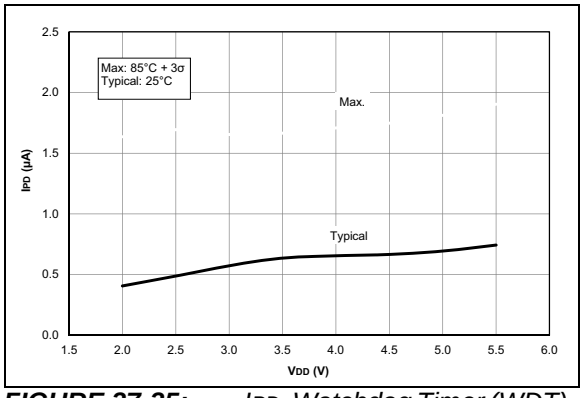


FIGURE 37-35: *IPD, Watchdog Timer (WDT), PIC16F1777/8/9 Only.*

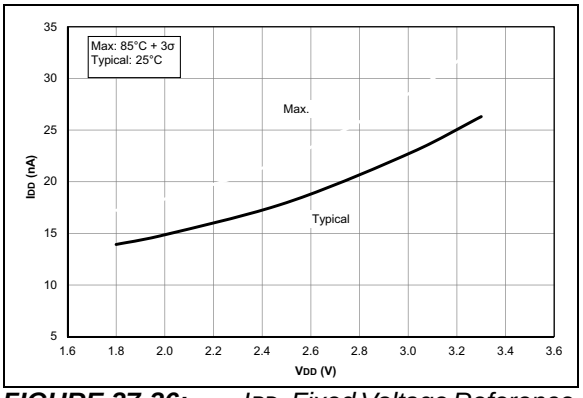


FIGURE 37-36: *IPD, Fixed Voltage Reference (FVR), ADC, PIC16LF1777/8/9 Only.*

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

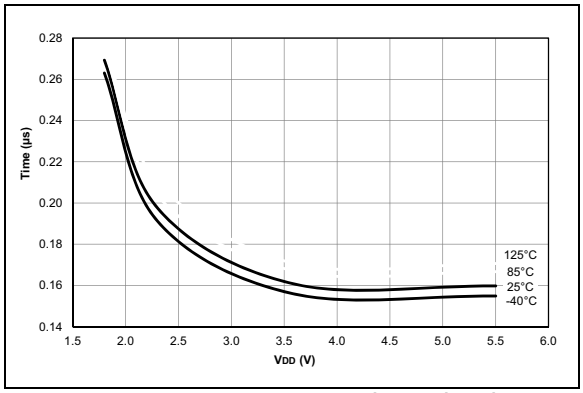


FIGURE 37-133: *COG Dead-Band Delay, DBR/DBF = 32, Typical Measured Values.*

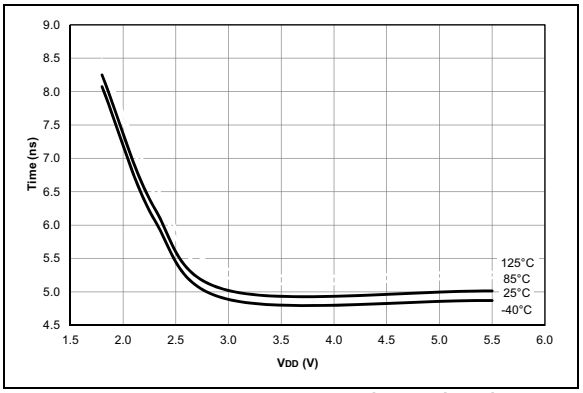


FIGURE 37-134: *COG Dead-Band Delay, DBR/DBF Delay per Step, Typical Measured Values.*

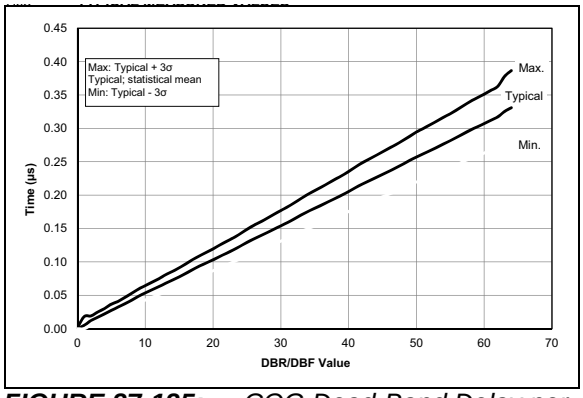


FIGURE 37-135: *COG Dead-Band Delay per Step, Typical Measured Values.*

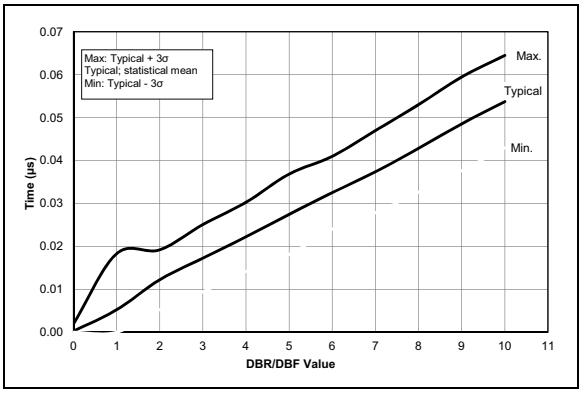


FIGURE 37-136: *COG Dead-Band Delay per Step, Zoomed to First 10 Codes, Typical Measured Values.*

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
═ ISO/TS 16949 ═

Trademarks

ISBN: 978-1-5224-1016-4