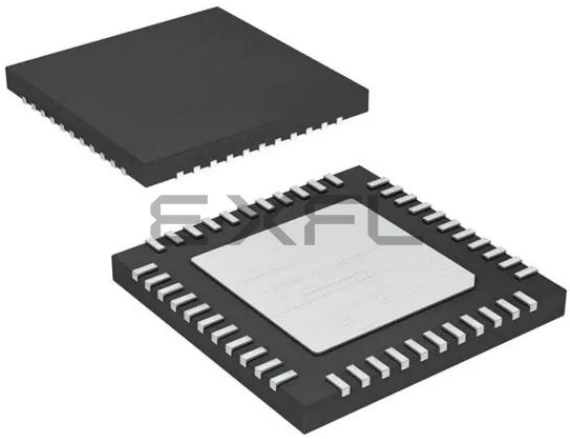

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 28x10b; D/A 4x5b, 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1777t-i-ml

TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 27 (Continued)											
DC1h	PWM12PHL(3)	PH<7:0>								xxxx xxxx	uuuu uuuu
DC2h	PWM12PHH(3)	PH<15:8>								xxxx xxxx	uuuu uuuu
DC3h	PWM12DCL(3)	DC<7:0>								xxxx xxxx	uuuu uuuu
DC4h	PWM12DCH(3)	DC<15:8>								xxxx xxxx	uuuu uuuu
DC5h	PWM12PRL(3)	PR<7:0>								xxxx xxxx	uuuu uuuu
DC6h	PWM12PRH(3)	PR<15:8>								xxxx xxxx	uuuu uuuu
DC7h	PWM12OFL(3)	OF<7:0>								xxxx xxxx	uuuu uuuu
DC8h	PWM12OFH(3)	OF<15:8>								xxxx xxxx	uuuu uuuu
DC9h	PWM12TMRL(3)	TMR<7:0>								0000 0000	0000 0000
DCAh	PWM12TMRH(3)	TMR<15:8>								0000 0000	0000 0000
DCBh	PWM12CON(3)	EN	—	OUT	POL	MODE<1:0>		—	—	0-00 00--	0-00 00--
DCCh	PWM12INTE(3)	—	—	—	—	OFIE	PHIE	DCIE	PRIE	---- 0000	---- 0000
DCDh	PWM12INTF(3)	—	—	—	—	OFIF	PHIF	DCIF	PRIF	---- 0000	---- 0000
DCEh	PWM12CLKCON(3)	—	PS<2:0>			—	—	CS<1:0>		-000 --00	-000 --00
DCFh	PWM12LDCON(3)	LDA	LDT	—	—	—	—	LDS<1:0>		00-- --00	00-- --00
DD0h	PWM12OFCON(3)	—	OFM<1:0>		OFO	—	—	OFS<1:0>		-000 --00	-000 --00
DD1h to DEFh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

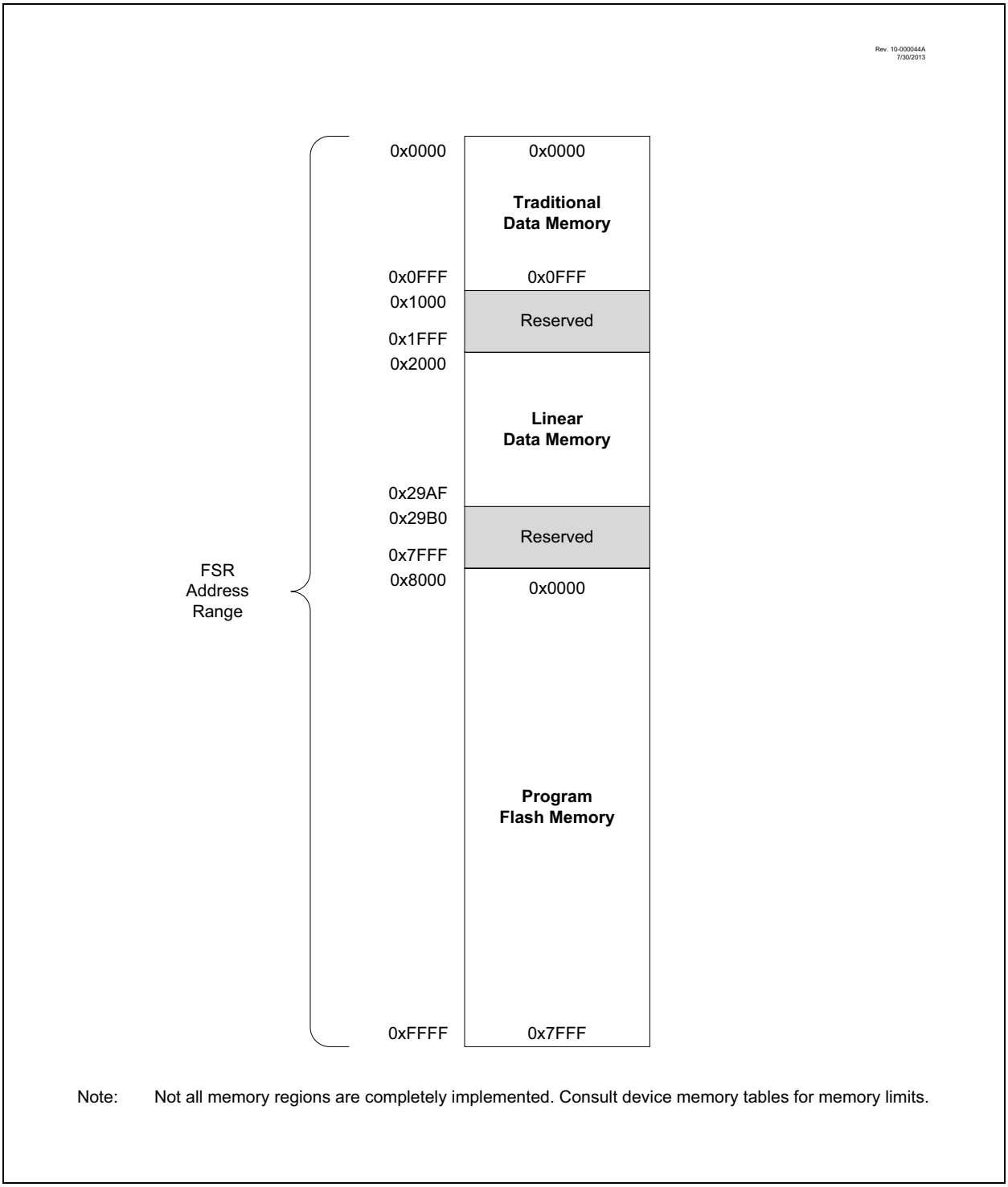
TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 30											
F0Ch — F0Eh	—	Unimplemented								—	—
F0Fh	CLCDATA	—	—	—	—	MLC4OUT	MLC3OUT	MLC2OUT	MLC1OUT	---- x000	---- u000
F10h	CLC1CON	EN	—	OUT	INTP	INTN	MODE<2:0>			0-00 0000	0-00 0000
F11h	CLC1POL	POL	—	—	—	G4POL	G3POL	G2POL	G1POL	0--- xxxx	0--- uuuu
F12h	CLC1SEL0	—	—	D1S<5:0>						--xx xxxx	--uu uuuu
F13h	CLC1SEL1	—	—	D2S<5:0>						--xx xxxx	--uu uuuu
F14h	CLC1SEL2	—	—	D3S<5:0>						--xx xxxx	--uu uuuu
F15h	CLC1SEL3	—	—	D4S<5:0>						--xx xxxx	--uu uuuu
F16h	CLC1GLS0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	xxxx xxxx	uuuu uuuu
F17h	CLC1GLS1	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	xxxx xxxx	uuuu uuuu
F18h	CLC1GLS2	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	xxxx xxxx	uuuu uuuu
F19h	CLC1GLS3	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	xxxx xxxx	uuuu uuuu
F1Ah	CLC2CON	EN	—	OUT	INTP	INTN	MODE<2:0>			0-00 0000	0-00 0000
F1Bh	CLC2POL	POL	—	—	—	G4POL	G3POL	G2POL	G1POL	0--- xxxx	0--- uuuu
F1Ch	CLC2SEL0	—	—	D1S<5:0>						--xx xxxx	--uu uuuu
F1Dh	CLC2SEL1	—	—	D2S<5:0>						--xx xxxx	--uu uuuu
F1Eh	CLC2SEL2	—	—	D3S<5:0>						--xx xxxx	--uu uuuu
F1Fh	CLC2SEL3	—	—	D4S<5:0>						--xx xxxx	--uu uuuu
F20h	CLC2GLS0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	xxxx xxxx	uuuu uuuu
F21h	CLC2GLS1	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	xxxx xxxx	uuuu uuuu
F22h	CLC2GLS2	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	xxxx xxxx	uuuu uuuu
F23h	CLC2GLS3	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	xxxx xxxx	uuuu uuuu
F24h	CLC3CON	EN	—	OUT	INTP	INTN	MODE<2:0>			0-00 0000	0-00 0000
F25h	CLC3POL	POL	—	—	—	G4POL	G3POL	G2POL	G1POL	0--- xxxx	0--- uuuu
F26h	CLC3SEL0	—	—	D1S<5:0>						--xx xxxx	--uu uuuu
F27h	CLC3SEL1	—	—	D2S<5:0>						--xx xxxx	--uu uuuu
F28h	CLC3SEL2	—	—	D3S<5:0>						--xx xxxx	--uu uuuu
F29h	CLC3SEL3	—	—	D4S<5:0>						--xx xxxx	--uu uuuu
F2Ah	CLC3GLS0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

FIGURE 3-9: INDIRECT ADDRESSING



Note: Not all memory regions are completely implemented. Consult device memory tables for memory limits.

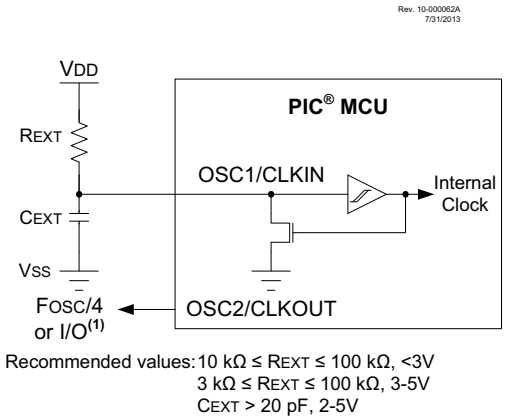
5.2.1.6 External RC Mode

The external Resistor-Capacitor (EXTRC) mode supports the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required.

The RC circuit connects to OSC1. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. The function of the OSC2/CLKOUT pin is determined by the $\overline{\text{CLKOUTEN}}$ bit in Configuration Words.

Figure 5-6 shows the external RC mode connections.

FIGURE 5-6: EXTERNAL RC MODES



Note 1: Output depends upon the $\overline{\text{CLKOUTEN}}$ bit of the Configuration Words.

The RC oscillator frequency is a function of the supply voltage, the resistor (R_{EXT}) and capacitor (C_{EXT}) values and the operating temperature. Other factors affecting the oscillator frequency are:

- threshold voltage variation
- component tolerances
- packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

5.2.2 INTERNAL CLOCK SOURCES

The device may be configured to use the internal oscillator block as the system clock by performing one of the following actions:

- Program the FOSC<2:0> bits in Configuration Words to select the INTOSC clock source, which will be used as the default system clock upon a device Reset.
- Write the SCS<1:0> bits in the OSCCON register to switch the system clock source to the internal oscillator during run-time. See **Section 5.3 "Clock Switching"** for more information.

In **INTOSC** mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT is available for general purpose I/O or CLKOUT.

The function of the OSC2/CLKOUT pin is determined by the $\overline{\text{CLKOUTEN}}$ bit in Configuration Words.

The internal oscillator block has two independent oscillators and a dedicated Phase Lock Loop, HFPLL, that can produce one of three internal system clock sources.

1. The **HFINTOSC** (High-Frequency Internal Oscillator) is factory calibrated and operates at 16 MHz. The HFINTOSC source is generated from the 500 kHz MFINTOSC source and the dedicated Phase Lock Loop, HFPLL. The frequency of the HFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 5-3).
2. The **MFINTOSC** (Medium-Frequency Internal Oscillator) is factory calibrated and operates at 500 kHz. The frequency of the MFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 5-3).
3. The **LFINTOSC** (Low-Frequency Internal Oscillator) is uncalibrated and operates at 31 kHz.

REGISTER 7-6: PIE5: PERIPHERAL INTERRUPT ENABLE REGISTER 5

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
CCP8IE(1)	CCP7IE	COG4IE	COG3IE	C8IE(1)	C7IE(1)	C6IE	C5IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **CCP8IE:** CCP8 Interrupt Enable bit(1)
- 1 = Enables the CCP8 interrupt
- 0 = Disables the CCP8 interrupt

bit 6 **CCP7IE:** CCP7 Interrupt Enable bit
- 1 = Enables the CCP7 interrupt
- 0 = Disables the CCP7 interrupt

bit 5 **COG4IE:** COG4 Auto-Shutdown Interrupt Enable bit
- 1 = COG4 interrupt enabled
- 0 = COG4 interrupt disabled

bit 4 **COG3IE:** COG3 Auto-Shutdown Interrupt Enable bit
- 1 = COG3 interrupt enabled
- 0 = COG3 interrupt disabled

bit 3 **C8IE:** Comparator C8 Interrupt Enable bit(1)
- 1 = Enables the Comparator C8 interrupt
- 0 = Disables the Comparator C8 interrupt

bit 2 **C7IE:** Comparator C7 Interrupt Enable bit(1)
- 1 = Enables the Comparator C7 interrupt
- 0 = Disables the Comparator C7 interrupt

bit 1 **C6IE:** Comparator C6 Interrupt Enable bit
- 1 = Enables the Comparator C6 interrupt
- 0 = Disables the Comparator C6 interrupt

bit 0 **C5IE:** Comparator C5 Interrupt Enable bit
- 1 = Enables the Comparator C5 interrupt
- 0 = Disables the Comparator C5 interrupt

Note 1: PIC16(L)F1777/9 only.

TABLE 7-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	132
OPTION_REG	$\overline{\text{WPUEN}}$	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			274
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	133
PIE2	OSFIE	C2IE	C1IE	COG1IE	BCL1IE	C4IE	C3IE	CCP2IE	134
PIE3	—	—	COG2IE	ZCDIE	CLC4IE	CLC3IE	CLC2IE	CLC1IE	135
PIE4	—	TMR8IE	TMR5GIE	TMR5IE	TMR3GIE	TMR3IE	TMR6IE	TRM4IE	136
PIE5	CCP8IE(1)	CCP7IE	COG4IE(1)	COG3IE	C8IE(1)	C7IE(1)	C6IE	C5IE	137
PIE6	—	—	—	—	PWM12IE(1)	PWM11IE	PWM6IE	PWM5IE	138
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	139
PIR2	OSFIF	C2IF	C1IF	COG1IF	BCL1IF	C4IF	C3IF	CCP2IF	140
PIR3	—	—	COG2IF	ZCDIF	CLC4IF	CLC3IF	CLC2IF	CLC1IF	141
PIR4	—	TMR8IF	TMR5GIF	TMR5IF	TMR3GIF	TMR3IF	TMR6IF	TRM4IF	142
PIR5	CCP8IF(1)	CCP7IF	COG4IF(1)	COG3IF	C8IF(1)	C7IF(1)	C6IF	C5IF	143
PIR6	—	—	—	—	PWM12IF(1)	PWM11IF	PWM6IF	PWM5IF	144

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by interrupts.

Note 1: PIC16(L)F1777/9 only.

TABLE 12-2: AVAILABLE PORTS FOR OUTPUT BY PERIPHERAL(2) (CONTINUED)

RxyPPS<5:0>	Output Signal	PIC16(L)F1778			PIC16(L)F1777/9				
		A	B	C	A	B	C	D	E
001001	COG2A(1)		●	●		●	●		
001000	COG1D(1)		●	●		●		●	
000111	COG1C(1)		●	●		●		●	
000110	COG1B(1)		●	●		●		●	
000101	COG1A(1)		●	●		●	●		
000100	LC4_out		●	●		●		●	
000011	LC3_out		●	●		●		●	
000010	LC2_out	●		●	●		●		
000001	LC1_out	●		●	●		●		
000000	LATxy	●	●	●	●	●	●	●	●

Note 1: TRIS control is overridden by the peripheral as required.
2: Unsupported peripherals will output a '0'.
3: PIC16(L)F1777/9 only.

19.11 Register Definitions: Comparator Control

Long bit name prefixes for the Comparator peripherals are shown in Table 19-3. Refer to **Section 1.1.2.2 "Long Bit Names"** for more information

TABLE 19-3:

Peripheral	Bit Name Prefix
Comparator 1	C1
Comparator 2	C2
Comparator 3	C3
Comparator 4	C4
Comparator 5	C5
Comparator 6	C6
Comparator 7(1)	C7
Comparator 8(1)	C8

Note 1: PIC16(L)F1777/9 only.

REGISTER 19-1: CMxCON0: COMPARATOR Cx CONTROL REGISTER 0

R/W-0/0	R-0/0	U-0	R/W-0/0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-0/0
ON	OUT	—	POL	ZLF	—	HYS	SYNC
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **ON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled and consumes no active power

bit 6 **OUT:** Comparator Output bit
If POL = 1 (inverted polarity):
1 = CxVP < CxVN
0 = CxVP > CxVN
If POL = 0 (non-inverted polarity):
1 = CxVP > CxVN
0 = CxVP < CxVN

bit 5 **Reserved:** Read as '1'. Maintain this bit set.

bit 4 **POL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 3 **ZLF:** Comparator Zero Latency Filter Enable bit
1 = Comparator output is filtered
0 = Comparator output is unfiltered

bit 2 **Reserved:** Read as '1'. Maintain this bit set.

bit 1 **HYS:** Comparator Hysteresis Enable bit
1 = Comparator hysteresis enabled
0 = Comparator hysteresis disabled

bit 0 **SYNC:** Comparator Output Synchronous Mode bit
1 = Comparator output to Timer1 and I/O pin is synchronous to changes on Timer1 clock source. Output updated on the falling edge of Timer1 clock source.
0 = Comparator output to Timer1 and I/O pin is asynchronous

FIGURE 27-2: SIMPLIFIED COG BLOCK DIAGRAM (STEERED PWM MODE, MD = 0)

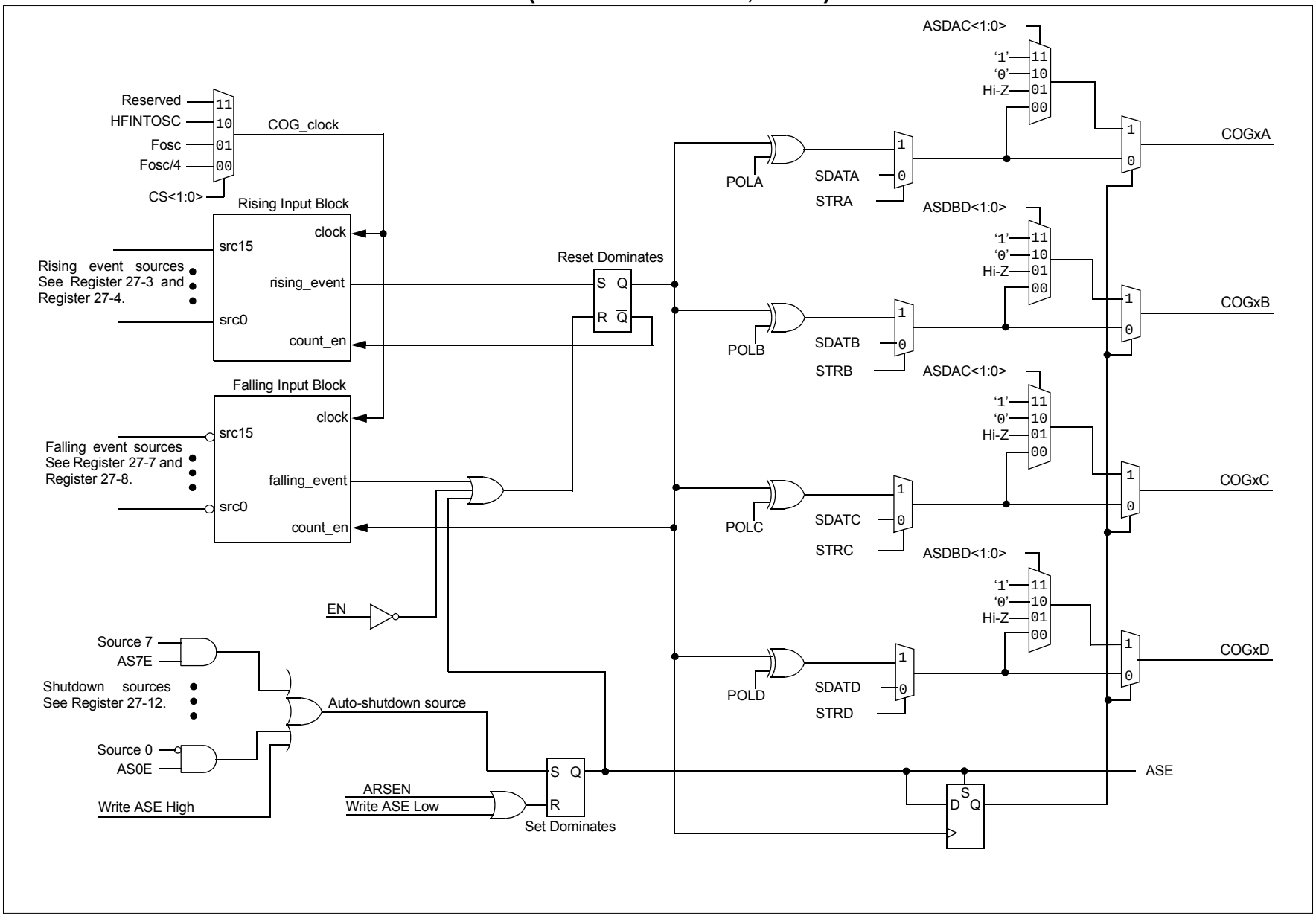


FIGURE 27-7: COG (RISING/FALLING) INPUT BLOCK

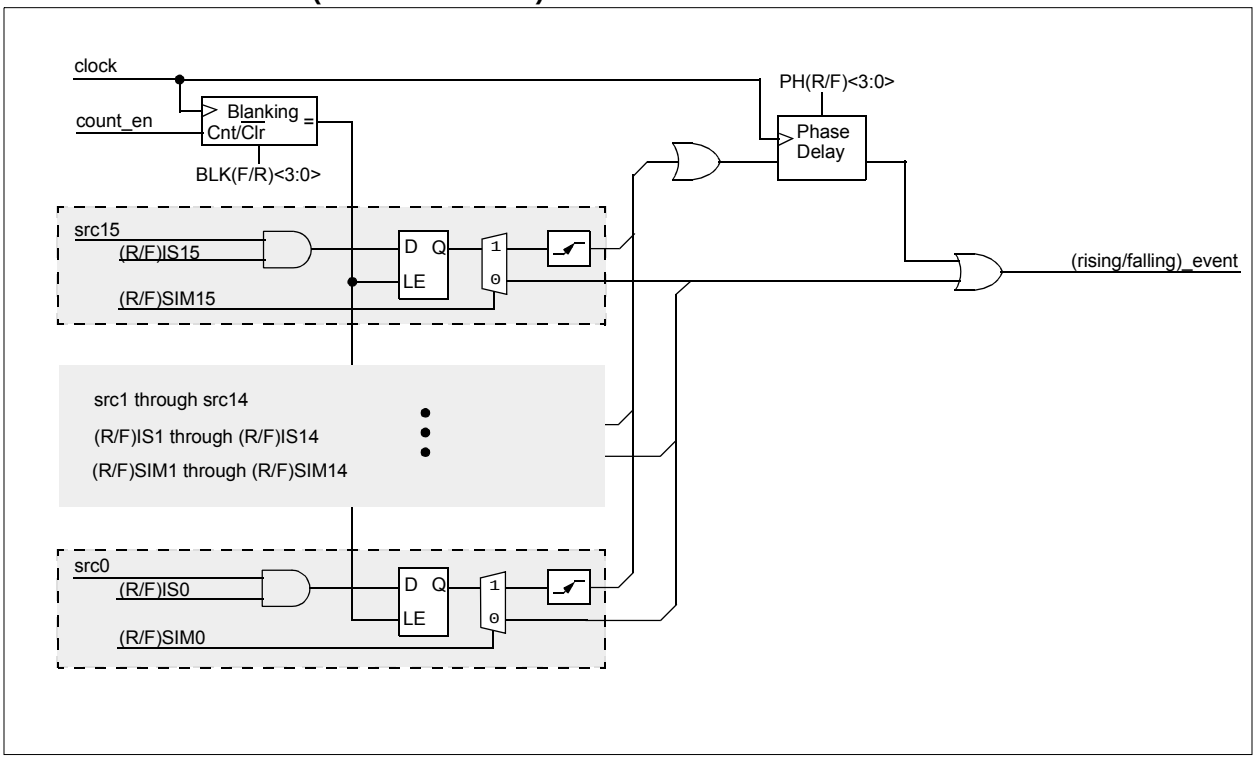


FIGURE 27-8: COG (RISING/FALLING) DEAD-BAND BLOCK

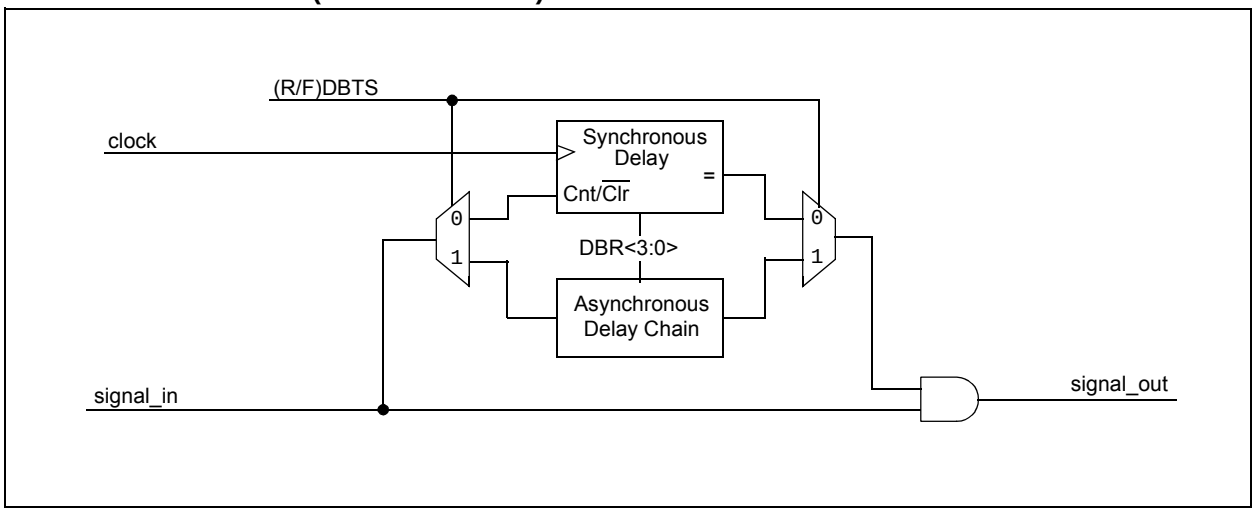


FIGURE 27-9: TYPICAL HALF-BRIDGE MODE COG OPERATION WITH CCP1

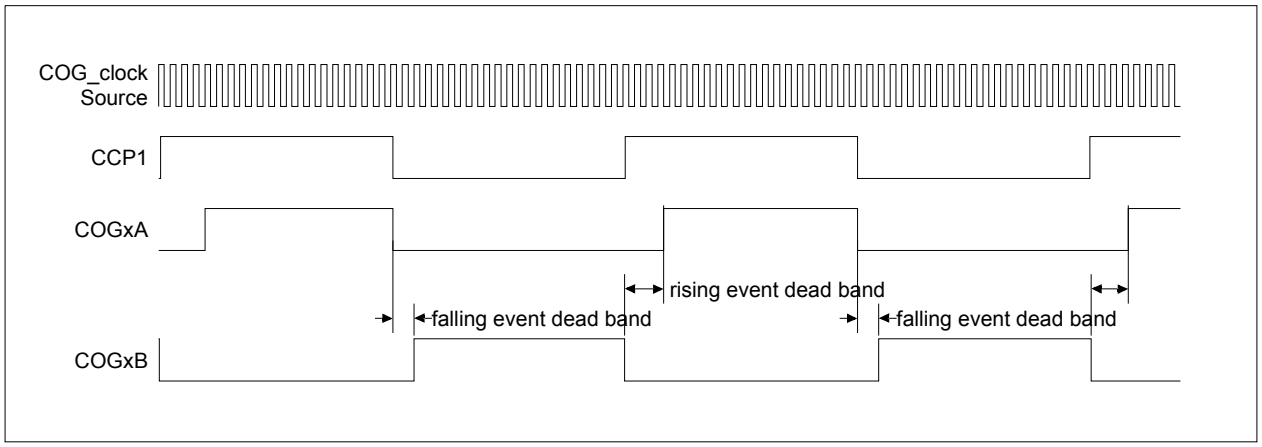


FIGURE 27-10: HALF-BRIDGE MODE COG OPERATION WITH CCP1 AND PHASE DELAY

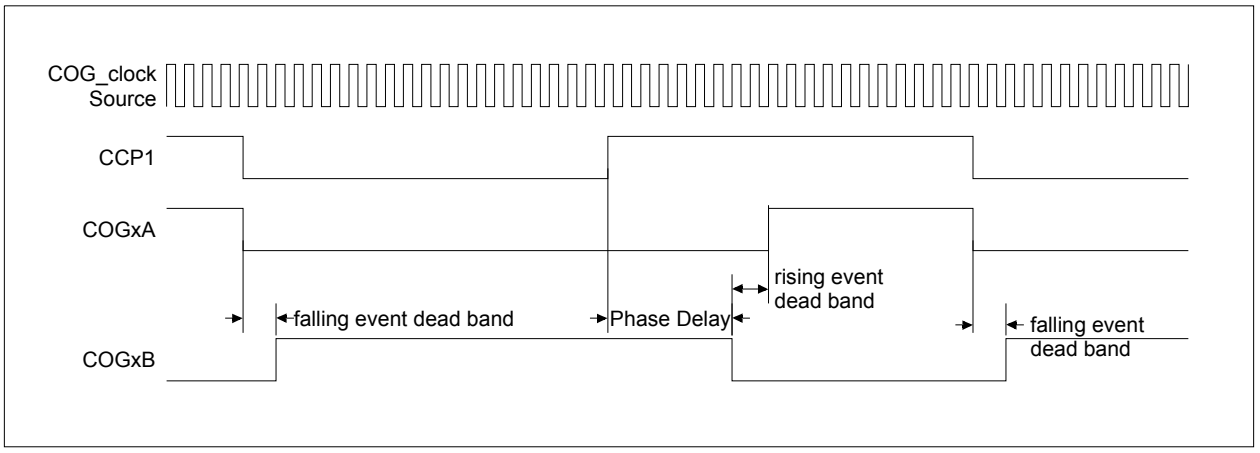
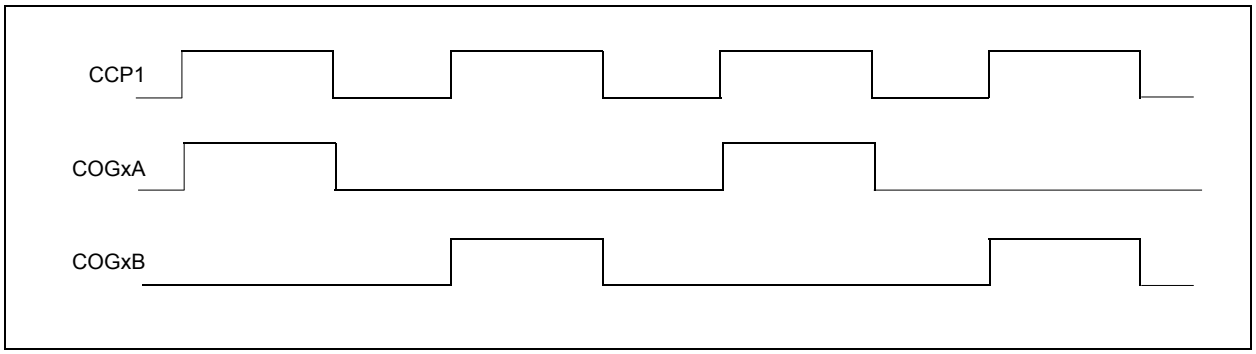


FIGURE 27-11: PUSH-PULL MODE COG OPERATION WITH CCP1



27.8.1 FALLING EVENT BLANKING OF RISING EVENT INPUTS

The falling event blanking counter inhibits rising event inputs from triggering a rising event. The falling event blanking time starts when the rising_event output drive goes false.

The falling event blanking time is set by the value contained in the COGxBLKF register (Register 27-17). Blanking times are calculated using the formula shown in Equation 27-1.

When the COGxBLKF value is zero, falling event blanking is disabled and the blanking counter output is true, thereby, allowing the event signal to pass straight through to the event trigger circuit.

27.8.2 RISING EVENT BLANKING OF FALLING EVENT INPUTS

The rising event blanking counter inhibits falling event inputs from triggering a falling event. The rising event blanking time starts when the falling_event output drive goes false.

The rising event blanking time is set by the value contained in the COGxBLKR register (Register 27-16).

When the COGxBLKR value is zero, rising event blanking is disabled and the blanking counter output is true, thereby, allowing the event signal to pass straight through to the event trigger circuit.

27.8.3 BLANKING TIME UNCERTAINTY

When the rising and falling sources that trigger the blanking counters are asynchronous to the COG_clock, it creates uncertainty in the blanking time. The maximum uncertainty is equal to one COG_clock period. Refer to Equation 27-1 and Example 27-1 for more detail.

27.9 Phase Delay

It is possible to delay the assertion of either or both the rising event and falling events. This is accomplished by placing a non-zero value in COGxPHR or COGxPHF phase-delay count registers, respectively (Register 27-18 and Register 27-19). Refer to Figure 27-10 for COG operation with CCP1 and phase delay. The delay from the input rising event signal switching to the actual assertion of the events is calculated the same as the dead-band and blanking delays. Refer to Equation 27-1.

When the phase-delay count value is zero, phase delay is disabled and the phase-delay counter output is true, thereby, allowing the event signal to pass straight through to the complementary output driver flop.

27.9.1 CUMULATIVE UNCERTAINTY

It is not possible to create more than one COG_clock of uncertainty by successive stages. Consider that the phase-delay stage comes after the blanking stage, the dead-band stage comes after either the blanking or phase-delay stages, and the blanking stage comes after the dead-band stage. When the preceding stage is enabled, the output of that stage is necessarily synchronous with the COG_clock, which removes any possibility of uncertainty in the succeeding stage.

EQUATION 27-1: PHASE, DEAD-BAND, AND BLANKING TIME CALCULATION

$$T_{\min} = \frac{\text{Count}}{F_{COG\_\text{clock}}}$$

$$T_{\max} = \frac{\text{Count} + 1}{F_{COG\_\text{clock}}}$$

$$T_{\text{uncertainty}} = T_{\max} - T_{\min}$$

Also:

$$T_{\text{uncertainty}} = \frac{1}{F_{COG\_\text{clock}}}$$

Where:

T	Count
Rising Phase Delay	COGxPHR
Falling Phase Delay	COGxPHF
Rising dead band	COGxDBR
Falling dead band	COGxDBF
Rising Event Blanking	COGxBLKR
Falling Event Blanking	COGxBLKF

29.1 OPA Module Performance

Common AC and DC performance specifications for the OPA module:

- Common-Mode Voltage Range
- Leakage Current
- Input Offset Voltage
- Open-Loop Gain
- Gain Bandwidth Product

Common-mode voltage range is the specified voltage range for the OPA+ and OPA- inputs, for which the OPA module will perform to within its specifications. The OPA module is designed to operate with input voltages between VSS and VDD. Behavior for common-mode voltages greater than VDD, or below VSS, are not guaranteed.

Leakage current is a measure of the small source or sink currents on the OPA+ and OPA- inputs. To minimize the effect of leakage currents, the effective impedances connected to the OPA+ and OPA- inputs should be kept as small as possible and equal.

Input offset voltage is a measure of the voltage difference between the OPA+ and OPA- inputs in a closed loop circuit with the OPA in its linear region. The offset voltage will appear as a DC offset in the output equal to the input offset voltage, multiplied by the gain of the circuit. The input offset voltage is also affected by the common-mode voltage. The OPA is factory calibrated to minimize the input offset voltage of the module.

Open-loop gain is the ratio of the output voltage to the differential input voltage, (OPA+) - (OPA-). The gain is greatest at DC and falls off with frequency.

Gain Bandwidth Product or GBWP is the frequency at which the open-loop gain falls off to 0 dB.

29.2 OPA Module Control

The OPA module is enabled by setting the OPAxEN bit of the OPAxCON register (Register 29-1). When enabled, the OPA forces the output driver of the OPAxOUT pin into tri-state to prevent contention between the driver and the OPA output.

Note:	When the OPA module is enabled, the OPAxOUT pin is driven by the op amp output, not by the PORT digital driver. Refer to Table 36-17: Operational Amplifier (OPA) for the op amp output drive capability.

29.2.1 UNITY GAIN MODE

The OPAxUG bit of the OPAxCON register (Register 29-1) selects the Unity Gain mode. When unity gain is selected, the OPA output is connected to the inverting input and the OPAxIN pin is relinquished, releasing the pin for general purpose input and output.

29.2.2 PROGRAMMABLE SOURCE SELECTIONS

The inverting and non-inverting sources are selected with the OPAxNCHS (Register 29-3) and OPAxPCHS (Register 29-4) registers, respectively. Sources include:

- Internal DACs
- Device pins
- Internal slope compensation ramp generator
- Other op amps in the device

29.3 Override Control

29.3.1 OVERRIDE MODE

The op amp operation can be overridden in two ways:

- Forced tri-state output
- Force unity gain

The Override mode is selected with the ORM<1:0> bits of the OPxCON register (Register 29-1). The override is in effect when the mode is selected and the override source is true.

29.3.2 OVERRIDE SOURCES

The override source is selected with the OPAxORS register (Register 29-2). Sources are from internal peripherals including:

- CCP outputs
- PWM outputs
- Comparator outputs
- Zero-cross detect output
- Configurable Logic Cell outputs
- COG outputs

29.3.3 OVERRIDE SOURCE POLARITY

The override source polarity can be inverted so that the override will occur on either the high or low level of the selected source. Override polarity is controlled by the ORPOL bit of the OPAxCON register (Register 29-1).

29.4 Effects of Reset

A device Reset forces all registers to their Reset state. This disables the OPA module.

29.5 Effects of Sleep

The operational amplifier continues to operate when the device is put in Sleep mode.

sensitive timing inputs that occur during, and extend beyond, the one-shot period will be suspended until the end of the one-shot time.

30.1.2.2 Rising Ramp

The Rising Ramp mode is identical to the Slope Compensation mode except that the ramps have a rising slope instead of a falling slope. One side of the internal capacitor is connected to the voltage input source and the other side is connected to the internal current source. The internal current source charges this capacitor at a programmable rate. As the capacitor charges, the capacitor voltage is added to the voltage source, producing a linear voltage rise at the required rate (see Figure 30-5). The ramp terminates and the capacitor is discharged when the set_falling timing input goes true. The next ramp starts when the set_rising timing input goes true.

Enabling the optional one-shot by setting the OS bit of the PRGxCON0 register ensures that the capacitor is fully discharged by overriding the set_rising timing input and holding the shorting switch closed for at least the one-shot period, typically 50 ns. Edge sensitive timing inputs that occur during the one-shot period will be ignored. Level sensitive timing inputs that occur during, and extend beyond, the one-shot period will be suspended until the end of the one-shot time.

30.2 Enable, Ready, Go

The EN bit of the PRGxCON0 register enables the analog circuitry including the current sources. This permits preparing the PRG module for use and allowing it to become stable before putting it into operation. When the EN bit is set then the timing inputs are enabled so that initial ramp action can be determined before the GO bit is set. The capacitor shorting switch is closed when the EN bit is set and remains closed while the GO bit is zero.

The RDY bit of the PRGxCON1 register indicates that the analog circuits and current sources are stable.

The GO bit of the PRGxCON0 register enables the switch control circuits, thereby putting the PRG into operation. The GO transition from cleared to set triggers the one-shot, thereby extending the capacitor shorting switch closure for the one-shot period.

To ensure predictable operation, set the EN bit first then wait for the RDY bit to go high before setting the GO bit.

30.3 Independent Set_rising and Set_falling Timing Inputs

The timing inputs determine when the ramp starts and stops. In the Alternating Rising/Falling mode the ramp rises when the set_rising input goes true and falls when the set_falling input goes true. In the Slope Compensation and Rising Ramp modes the capacitor is discharged when the set_falling timing input goes true and the ramp starts when the set_rising timing input goes true. The set_falling input dominates the set_rising input.

30.4 Level and Edge Timing Sensitivity

The set_rising and set_falling timing inputs can be independently configured as either level or edge sensitive.

Level sensitive operation is useful when it is necessary to detect a timing input true state after an overriding condition ceases. For example, level sensitivity is useful for capacitor generated timing inputs that may be suppressed by the overriding action of the one-shot. With level sensitivity a capacitor output that changes during the one-shot period will be detected at the end of the one-shot time. With edge sensitivity the change would be ignored.

Edge sensitive operation is useful for periodic timing inputs such as those generated by PWMs and clocks. The duty cycle of a level sensitive periodic signal may interfere with the other timing input. Consider an Alternating Ramp mode with a level sensitive 50% PWM as the set_rising timing source and a level sensitive comparator as the set_falling timing source. If the comparator output reverses the ramp while the PWM signal is still high then the ramp will improperly reverse again when the comparator signal goes low. That same scenario with the set_rising timing input set for edge sensitivity would properly change the ramp output to rising only on the rising edge of the PWM signal.

Set_rising and set_falling timing input edge sensitivity is selected with the respective REDG and FEDG bits of the PRGxCON1 register.

30.5 One-Shot Minimum Timing

The one-shot timer ensures a minimum capacitor discharge time in the Slope Compensation and Rising Ramp modes, and a minimum rising or falling ramp duration in the Alternating Ramp mode. Setting the OS bit of the PRGxCON0 register enables the one-shot timer.

30.6 DAC Voltage Sources

When using any of the DACs as the voltage source expect a voltage offset equal to the current setting times the DAC equivalent resistance. This will be a constant offset in the Slope Compensation and Ramp modes and a positive/negative step offset in the Alternating mode. To avoid this limitation, feed the DAC output to the PRG input through one of the op amps set for unity gain.

30.7 Operation During Sleep

The RG module is unaffected by Sleep.

30.8 Effects of a Reset

The RG module resets to a disabled condition.

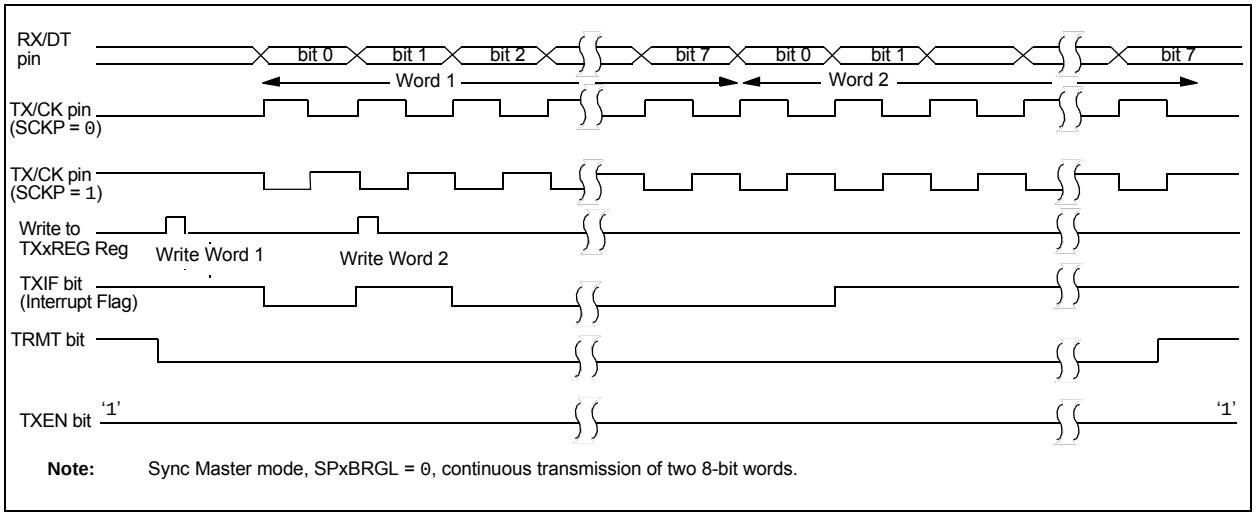
TABLE 30-6: SUMMARY OF REGISTERS ASSOCIATED WITH THE PRG MODULE(1)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PRGxCON0	EN	—	FEDG	REDG	MODE<1:0>		OS	GO	421
PRGxCON1	—	—	—	—	—	RDY	FPOL	RPOL	422
PRGxCON2	—	—	—	ISET<4:0>					423
PRGxINS	—	—	—	—	INS<3:0>				422
PRGxRPPS	—	—	PRGxRPPS<5:0>						424
PRGxFPPS	—	—	PRGxFPPS<5:0>						424
PRGxRTSS	—	—	—	—	RTSS<3:0>				205, 207
PRGxFTSS	—	—	—	—	FTSS<3:0>				205, 207
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	186
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	186
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—	187
WPUC	WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	188

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the PRG module.

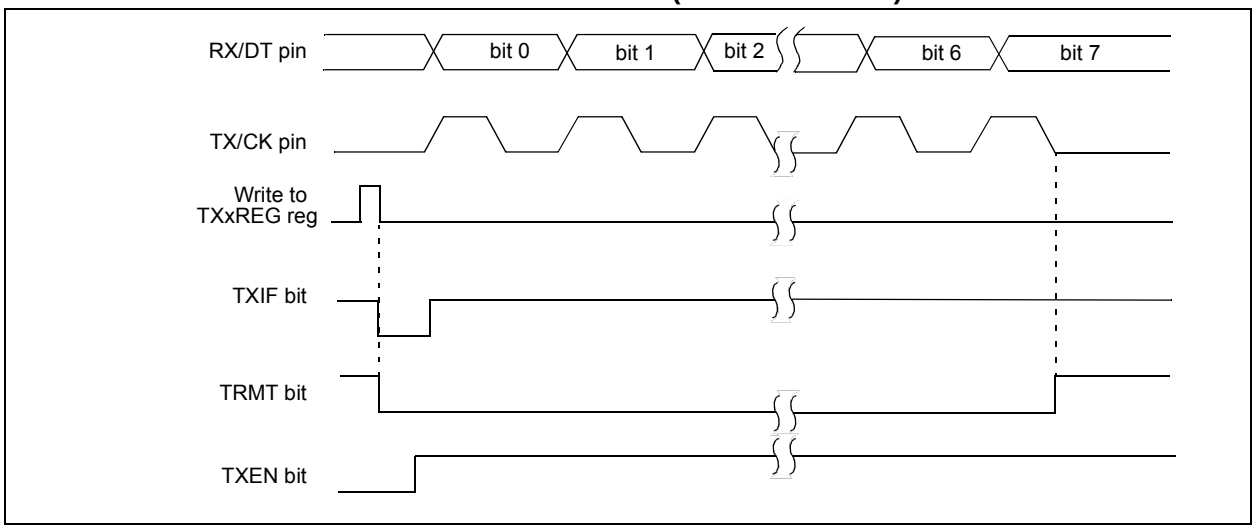
Note 1: PRG4 available on PIC16(L)F1777/9 only.

FIGURE 33-10: SYNCHRONOUS TRANSMISSION



Note: Sync Master mode, SPxBRGL = 0, continuous transmission of two 8-bit words.

FIGURE 33-11: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)



34.0 IN-CIRCUIT SERIAL PROGRAMMING™ (ICSP™)

ICSP™ programming allows customers to manufacture circuit boards with unprogrammed devices. Programming can be done after the assembly process, allowing the device to be programmed with the most recent firmware or a custom firmware. Five pins are needed for ICSP™ programming:

- ICSPCLK
- ICSPDAT
- $\overline{MCLR}$/VPP
- VDD
- VSS

In Program/Verify mode the program memory, User IDs and the Configuration Words are programmed through serial communications. The ICSPDAT pin is a bidirectional I/O used for transferring the serial data and the ICSPCLK pin is the clock input. For more information on ICSP™ refer to the **"***PIC16(L)F177X Memory Programming Specification***"** (DS40001792).

34.1 High-Voltage Programming Entry Mode

The device is placed into High-Voltage Programming Entry mode by holding the ICSPCLK and ICSPDAT pins low then raising the voltage on $\overline{MCLR}$/VPP to VIHH.

34.2 Low-Voltage Programming Entry Mode

The Low-Voltage Programming Entry mode allows the PIC® Flash MCUs to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Words is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'.

Entry into the Low-Voltage Programming Entry mode requires the following steps:

1. $\overline{MCLR}$ is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

Once the key sequence is complete, $\overline{MCLR}$ must be held at VIL for as long as Program/Verify mode is to be maintained.

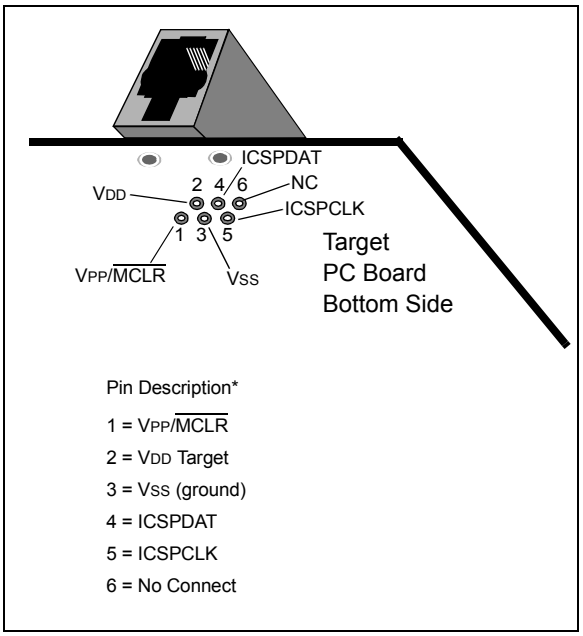
If low-voltage programming is enabled (LVP = 1), the $\overline{MCLR}$ Reset function is automatically enabled and cannot be disabled. See **Section 6.5 "MCLR"** for more information.

The LVP bit can only be reprogrammed to '0' by using the High-Voltage Programming mode.

34.3 Common Programming Interfaces

Connection to a target device is typically done through an ICSP™ header. A commonly found connector on development tools is the RJ-11 in the 6P6C (6-pin, 6-connector) configuration. See Figure 34-1.

FIGURE 34-1: ICD RJ-11 STYLE CONNECTOR INTERFACE



Another connector often found in use with the PICkit™ programmers is a standard 6-pin header with 0.1 inch spacing. Refer to Figure 34-2.

For additional interface recommendations, refer to your specific device programmer manual prior to PCB design.

It is recommended that isolation devices be used to separate the programming pins from other circuitry. The type of isolation is highly dependent on the specific application and may include devices such as resistors, diodes, or even jumpers. See Figure 34-3 for more information.

36.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:

Operating Voltage: $V_{DDMIN} \leq V_{DD} \leq V_{DDMAX}$
Operating Temperature: $T_{A\_MIN} \leq T_A \leq T_{A\_MAX}$

V_{DD} — Operating Supply Voltage(1)

PIC16LF1777/8/9

- V_{DDMIN} (Fosc ≤ 16 MHz) ..... +1.8V
- V_{DDMIN} (Fosc > 16 MHz) ..... +2.5V
- V_{DDMAX} ..... +3.6V

PIC16F1777/8/9

- V_{DDMIN} (Fosc ≤ 16 MHz) ..... +2.3V
- V_{DDMIN} (Fosc > 16 MHz) ..... +2.5V
- V_{DDMAX} ..... +5.5V

T_A — Operating Ambient Temperature Range

Industrial Temperature

- T_{A_MIN} ..... -40°C
- T_{A_MAX} ..... +85°C

Extended Temperature

- T_{A_MIN} ..... -40°C
- T_{A_MAX} ..... +125°C

Note 1: See Parameter D001, DS Characteristics: Supply Voltage.

TABLE 36-4: I/O PORTS (CONTINUED) (CONTINUED)

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
		Capacitive Loading Specs on Output Pins					
D101*	COSC2	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101A*	CIO	All I/O pins	—	—	50	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in EXTRC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: Including OSC2 in CLKOUT mode.

NOTES: