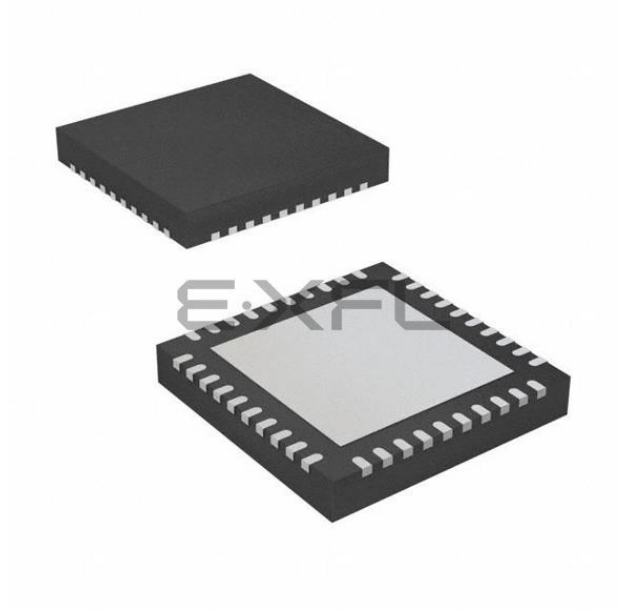

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 28x10b; D/A 4x5b, 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1777t-i-mv

TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F1777/9) (CONTINUED)

I/O	40-Pin PDIP	40-Pin (U)QFN	44-Pin TQFP	44-Pin QFN	ADC	VREF	DAC	Op Amp	Comparator	ZCD	PRG	Timers	PWM	CCP	COG	CLC	Modulator	EUSART	MSSP	Interrupt	Pull-ups	High Current	Basic
RB5	38	13	15	15	AN13	DAC5REF1- DAC7REF1-	—	—	C4IN2-	—	—	—	—	CCP7(1)	—	—	MD3MOD(1)	—	—	IOC	Y	—	—
RB6	39	14	16	16	—	DAC5REF1+ DAC7REF1+	—	—	C4IN1+	—	—	—	—	—	—	CLCIN2(1)	—	—	—	IOC	Y	—	ICSPCLK
RB7	40	15	17	17	—	—	DAC1OUT2 DAC2OUT2 DAC3OUT2 DAC4OUT2 DAC5OUT2 DAC6OUT2 DAC7OUT2 DAC8OUT2	—	C5IN1+	—	—	T6IN(1)	—	—	—	CLCIN3(1)	—	—	—	IOC	Y	—	ICSPDAT
RC0	15	30	32	34	—	—	DAC5OUT1	—	—	—	—	T1CKI(1) T3CKI(1) T3G(1) SOSCO	—	—	—	—	—	—	—	IOC	Y	—	—
RC1	16	31	35	35	—	—	DAC7OUT1	—	—	—	PRG2R(1)	SOSCI	—	CCP2(1)	—	—	—	—	—	IOC	Y	—	—
RC2	17	32	36	36	AN14	—	—	—	C5IN2- C6IN2-	—	PRG2F(1)	—	—	CCP1(1)	—	—	—	—	—	IOC	Y	—	—
RC3	18	33	37	37	AN15	—	—	—	—	—	—	T2IN(1)	—	—	—	—	MD2CL(1)	—	SCL	IOC	Y	—	—
RC4	23	38	42	42	AN16	—	—	—	C5IN3- C6IN3-	—	PRG3R(1)	T8IN(1)	—	—	—	—	MD2CH(1)	—	SDA	IOC	Y	—	—
RC5	24	39	43	43	AN17	—	—	OPA3IN0+	—	—	PRG3F(1)	T4IN(1)	—	—	—	—	MD2MOD(1)	—	—	IOC	Y	—	—
RC6	25	40	44	44	AN18	—	—	OPA3OUT OPA4IN1+ OPA4IN1-	C5IN1- C6IN1- C7IN1- C8IN1-	—	PRG3IN0 PRG4IN1	—	—	—	—	—	—	—	—	IOC	Y	—	—
RC7	26	1	1	1	AN19	—	—	OPA3IN0-	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	—
RD0	19	34	38	38	AN20	—	—	OPA4IN0+	—	—	—	—	—	—	—	—	—	—	—	—	Y	—	—
RD1	20	35	39	39	AN21	—	—	OPA4OUT OPA3IN1+ OPA3IN1-	C1IN4- C2IN4- C3IN4- C4IN4- C5IN4- C6IN4- C7IN4- C8IN4-	—	PRG3IN1 PRG4IN0	—	—	—	—	—	—	—	—	—	Y	—	—
RD2	21	36	40	40	AN22	—	DAC4OUT1	OPA4IN0-	—	—	—	—	—	—	—	—	—	—	—	—	Y	—	—
RD3	22	37	41	41	AN23	—	—	—	C8IN2-	—	—	—	—	—	—	—	—	—	—	—	Y	—	—
RD4	27	2	2	2	AN24	—	—	—	C7IN2-	—	—	—	—	—	—	—	—	—	—	—	Y	—	—
RD5	28	3	3	3	AN25	—	—	—	C7IN3- C8IN3-	—	—	—	—	—	—	—	—	—	—	—	Y	—	—
RD6	29	4	4	4	AN26	—	—	—	C7IN1+	—	—	—	—	—	—	—	—	—	—	—	Y	—	—
RD7	30	5	5	5	AN27	—	—	—	C8IN1+	—	—	—	—	—	—	—	—	—	—	—	Y	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection register.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-4: PERIPHERAL CONNECTION MATRIX

	Peripheral Input																							
Peripheral Output	**ADC Trigger**	**COG Clock**	**COG Rising/Falling**	**COG Shutdown**	**10-bit DAC**	**5-bit DAC**	**PRG Analog Input**	**PRG Rising/Falling**	**Comparator +**	**Comparator -**	**CLC**	**DSM CH**	**DSM CL**	**DSM Mod**	**Op Amp +**	**Op Amp -**	**Op Amp Override**	**10-bit PWM**	**16-bit PWM**	**CCP Capture**	**CCP Clock**	**Timer2/4/6/8 Clock**	**Timer2/4/6/8 Reset**	**Timer1/3/5 Gate**	**Timer0 Clock**
FVR					●	●	●		●	●					●	●									
ZCD											●						●					●			
PRG									●						●	●									
10-bit DAC							●		●						●	●									
5-bit DAC							●		●						●	●									
CCP	●		●					●			●	●	●	●			●						●		
Comparator (sync)	●							●			●						●			●			●	●	
Comparator (async)			●	●										●											
CLC	●		●	●							●	●	●	●			●			●		●	●		
DSM																									
COG																	●								
EUSART TX/CK											●			●											
EUSART DT											●			●											
MSSP SCK/SCL											●			●											
MSSP SDO/SDA											●			●											
Op Amp							●																		
10-bit PWM	●		●					●			●	●	●	●			●						●		
16-bit PWM	●		●					●			●	●	●	●			●						●		
Timer0 overflow	●										●													●	
Timer2 = T2PR				●							●							●			●		●		
Timer4 = T4PR				●							●							●			●		●		
Timer6 = T6PR				●							●							●			●		●		
Timer8 = T8PR				●							●							●			●		●		
Timer2 Postscale	●			●							●							●			●		●		
Timer4 Postscale	●			●							●							●			●		●		
Timer6 Postscale	●			●							●							●			●		●		
Timer8 Postscale	●			●							●							●			●		●		
Timer1 overflow	●										●							●			●				
Timer3 overflow	●										●							●			●				
Timer5 overflow	●										●							●			●				
SOSC																			●			●			
FOSC/4		●																				●			
FOSC		●									●	●	●						●			●			
HFINTOSC		●									●	●	●						●			●			
LFINTOSC											●								●			●			
MFINTOSC																						●			
IOCIF											●									●	●				
PPS Input pin			●	●				●				●	●	●						●	●	●	●	●	●

TABLE 3-8: PIC16(L)F1778 MEMORY MAP, BANK 16-23

BANK 16		BANK 17		BANK 18		BANK 19		BANK 20		BANK 21		BANK 22		BANK 23	
800h	Core Registers (Table 3-2)	880h	Core Registers (Table 3-2)	900h	Core Registers (Table 3-2)	980h	Core Registers (Table 3-2)	A00h	Core Registers (Table 3-2)	A80h	Core Registers (Table 3-2)	B00h	Core Registers (Table 3-2)	B80h	Core Registers (Table 3-2)
80Bh		88Bh		90Bh		98Bh		A0Bh		A8Bh		B0Bh		B8Bh	
80Ch	—	88Ch	Unimplemented Read as '0'	90Ch	CM4CON0	98Ch	Unimplemented Read as '0'	A0Ch	Unimplemented Read as '0'	A8Ch	Unimplemented Read as '0'	B0Ch	Unimplemented Read as '0'	B8Ch	Unimplemented Read as '0'
80Dh	COG3PHR			90Dh	CM4CON1										
80Eh	COG3PHF			90Eh	CM4NSEL										
80Fh	COG3BLKR			90Fh	CM4PSEL										
810h	COG3BLKF			910h	CM5CON0										
811h	COG3DBR			911h	CM5CON1										
812h	COG3DBF			912h	CM5NSEL										
813h	COG3CON0			913h	CM5PSEL										
814h	COG3CON1			914h	CM6CON0										
815h	COG3RIS0			915h	CM6CON1										
816h	COG3RIS1			916h	CM6NSEL										
817h	COG3RSIM0			917h	CM6PSEL										
818h	COG3RSIM1			918h	Unimplemented Read as '0'										
819h	COG3FIS0														
81Ah	COG3FIS1														
81Bh	COG3FSIM0														
81Ch	COG3FSIM1														
81Dh	COG3ASD0														
81Eh	COG3ASD1														
81Fh	COG3STR	89Fh		91Fh		99Fh		A1Fh		A9Fh		B1Fh		B9Fh	
820h	General Purpose Register 48 Bytes	8A0h	General Purpose Register 48 Bytes	920h	General Purpose Register 48 Bytes	9A0h	General Purpose Register 48 Bytes	A20h	General Purpose Register 48 Bytes	AA0h	General Purpose Register 48 Bytes	B20h	General Purpose Register 48 Bytes	BA0h	General Purpose Register 48 Bytes
86Fh		8EFh		96Fh		9EFh		A6Fh		AEFh		B6Fh		BEFh	
870h	Accesses 70h – 7Fh	8F0h	Accesses 70h – 7Fh	970h	Accesses 70h – 7Fh	9F0h	Accesses 70h – 7Fh	A70h	Accesses 70h – 7Fh	AF0h	Accesses 70h – 7Fh	B70h	Accesses 70h – 7Fh	BF0h	Accesses 70h – 7Fh
87Fh		8FFh		97Fh		9FFh		A7Fh		AFFh		B7Fh		BFFh	

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 9											
48Ch to 48Dh	—	Unimplemented								—	—
48Eh	ADRESL	ADC Result Register Low								xxxx xxxx	uuuu uuuu
48Fh	ADRESH	ADC Result Register High								xxxx xxxx	uuuu uuuu
490h	ADCON0	CHS<5:0>						GO/$\overline{\text{DONE}}$	ADON	0000 0000	0000 0000
491h	ADCON1	ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>		0000 -000	0000 -000
492h	ADCON2	—	—	TRIGSEL<5:0>						--00 0000	--00 0000
493h	T2TMR	Holding Register for the 8-bit TMR2 Register								0000 0000	0000 0000
494h	T2PR	TMR2 Period Register								1111 1111	1111 1111
495h	T2CON	ON	CKPS<2:0>			OUTPS<3:0>				0000 0000	0000 0000
496h	T2HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					0000 0000	0000 0000
497h	T2CLKCON	—	—	—	—	CS<3:0>				---- 0000	---- 0000
498h	T2RST	—	—	—	RSEL<4:0>					---0 0000	---0 0000
499h	—	Unimplemented								—	—
49Ah	T8TMR	Holding Register for the 8-bit TMR8 Register								0000 0000	0000 0000
49Bh	T8PR	TMR8 Period Register								1111 1111	1111 1111
49Ch	T8CON	ON	CKPS<2:0>			OUTPS<3:0>				0000 0000	0000 0000
49Dh	T8HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					0000 0000	0000 0000
49Eh	T8CLKCON	—	—	—	—	CS<3:0>				---- 0000	---- 0000
49Fh	T8RST	—	—	—	RSEL<4:0>					---0 0000	---0 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

5.6 Register Definitions: Oscillator Control

REGISTER 5-1: OSCCON: OSCILLATOR CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-1/1	R/W-1/1	R/W-1/1	U-0	R/W-0/0	R/W-0/0
SPLLEN	IRCF<3:0>				—	SCS<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **SPLLEN:** Software PLL Enable bit
If PLLEN in Configuration Words = 1:
SPLLEN bit is ignored. 4x PLL is always enabled (subject to oscillator requirements)
If PLLEN in Configuration Words = 0:
1 = 4x PLL Is enabled
0 = 4x PLL is disabled

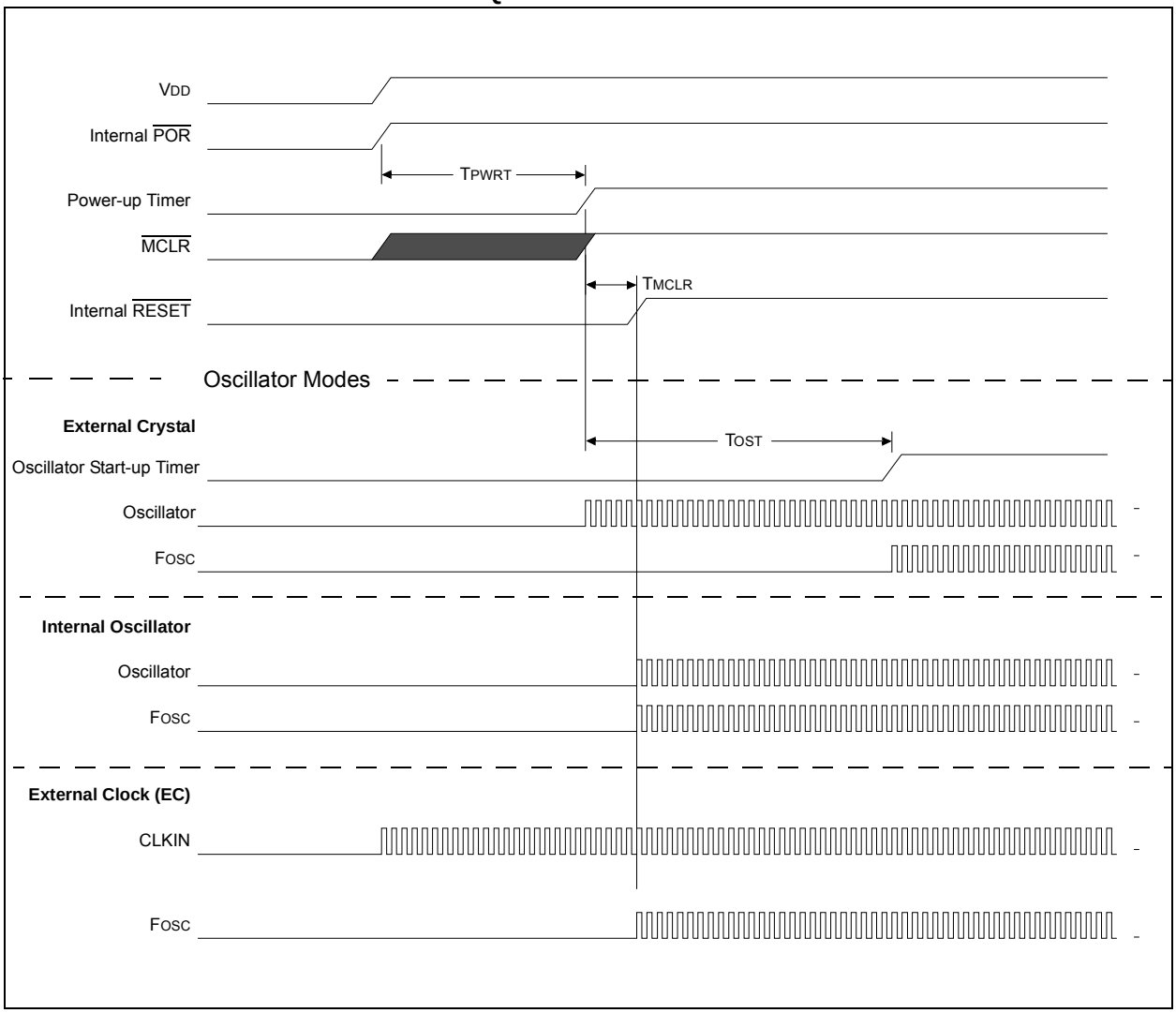
bit 6-3 **IRCF<3:0>:** Internal Oscillator Frequency Select bits
1111 = 16 MHz HF
1110 = 8 MHz or 32 MHz HF(2)
1101 = 4 MHz HF
1100 = 2 MHz HF
1011 = 1 MHz HF
1010 = 500 kHz HF(1)
1001 = 250 kHz HF(1)
1000 = 125 kHz HF(1)
0111 = 500 kHz MF (default upon Reset)
0110 = 250 kHz MF
0101 = 125 kHz MF
0100 = 62.5 kHz MF
0011 = 31.25 kHz HF(1)
0010 = 31.25 kHz MF
000x = 31 kHz LF

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **SCS<1:0>:** System Clock Select bits
1x = Internal oscillator block
01 = Secondary oscillator
00 = Clock determined by FOSC<2:0> in Configuration Words

Note 1: Duplicate frequency derived from HFINTOSC.
2: 32 MHz when SPLLEN bit is set. Refer to **Section 5.2.2.6 "32 MHz Internal Oscillator Frequency Selection"**.

FIGURE 6-3: RESET START-UP SEQUENCE



10.6 Register Definitions: Flash Program Memory Control

REGISTER 10-1: PMDATL: PROGRAM MEMORY DATA LOW BYTE REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
PMDAT<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **PMDAT<7:0>**: Read/write value for Least Significant bits of program memory

REGISTER 10-2: PMDATH: PROGRAM MEMORY DATA HIGH BYTE REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	PMDAT<13:8>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **PMDAT<13:8>**: Read/write value for Most Significant bits of program memory

REGISTER 10-3: PMADRL: PROGRAM MEMORY ADDRESS LOW BYTE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PMADR<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **PMADR<7:0>**: Specifies the Least Significant bits for program memory address

REGISTER 11-4: ANSELA: PORTA ANALOG SELECT REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **ANSA<5:0>**: Analog Select between Analog or Digital Function on pins RA<5:0>
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.
0 = Digital I/O. Pin is assigned to port or digital special function.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 11-5: WPUA: WEAK PULL-UP PORTA REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
WPUA7	WPUA6	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **WPUA<7:0>**: Weak Pull-up Register bits(1),(2)
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: Global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is configured as an output.

REGISTER 11-14: ODCONB: PORTB OPEN-DRAIN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ODB7	ODB6	ODB5	ODB4	ODB3	ODB2	ODB1	ODB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **ODB<7:0>:** PORTB Open-Drain Enable bits
For RB<7:0> pins
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

REGISTER 11-15: SLRCONB: PORTB SLEW RATE CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
SLRB7	SLRB6	SLRB5	SLRB4	SLRB3	SLRB2	SLRB1	SLRB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SLRB<7:0>:** PORTB Slew Rate Enable bits
For RB<7:0> pins
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

REGISTER 11-16: INLVLB: PORTB INPUT LEVEL CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
INLVLB7	INLVLB6	INLVLB5	INLVLB4	INLVLB3	INLVLB2	INLVLB1	INLVLB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **INLVLB<7:0>:** PORTB Input Level Select bits
For RB<7:0> pins
1 = Port pin digital input operates with ST thresholds
0 = Port pin digital input operates with TTL thresholds

12.3 Bidirectional Pins

PPS selections for peripherals with bidirectional signals on a single pin must be made so that the PPS input and PPS output select the same pin. Peripherals that have bidirectional signals include:

- EUSART (synchronous operation)
- MSSP (I^2C)

Note:	The I^2C default input pins are I^2C and SMBus compatible and are the only pins on the device with this compatibility.

12.4 PPS Lock

The PPS includes a mode in which all input and output selections can be locked to prevent inadvertent changes. PPS selections are locked by setting the PPSLOCKED bit of the PPSLOCK register. Setting and clearing this bit requires a special sequence as an extra precaution against inadvertent changes. Examples of setting and clearing the PPSLOCKED bit are shown in Example 12-1.

EXAMPLE 12-1: PPS LOCK/UNLOCK SEQUENCE

```
; suspend interrupts
    bcf     INTCON,GIE
;   BANKSEL PPSLOCK     ; set bank
; required sequence, next 5 instructions
    movlw   0x55
    movwf   PPSLOCK
    movlw   0xAA
    movwf   PPSLOCK
; Set PPSLOCKED bit to disable writes or
; Clear PPSLOCKED bit to enable writes
    bsf     PPSLOCK,PPSLOCKED
; restore interrupts
    bsf     INTCON,GIE
```

12.5 PPS Permanent Lock

The PPS can be permanently locked by setting the PPS1WAY Configuration bit. When this bit is set, the PPSLOCKED bit can only be cleared and set one time after a device Reset. This allows for clearing the PPSLOCKED bit so that the input and output selections can be made during initialization. When the PPSLOCKED bit is set after all selections have been made, it will remain set and cannot be cleared until after the next device Reset event.

12.6 Operation During Sleep

PPS input and output selections are unaffected by Sleep.

12.7 Effects of a Reset

A device Power-on Reset (POR) clears all PPS input and output selections to their default values. All other Resets leave the selections unchanged. Default input selections are shown in Table 12-1.

REGISTER 13-10: IOCEP: INTERRUPT-ON-CHANGE PORTE POSITIVE EDGE REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	U-0	U-0	U-0
—	—	—	—	IOCEP3	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3 **IOCEP3:** Interrupt-on-Change PORTE Positive Edge Enable bits
1 = Interrupt-on-Change enabled on the pin for a positive going edge. IOCEFx bit and IOCIF flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin.

bit 2-0 **Unimplemented:** Read as ‘0’

REGISTER 13-11: IOCEN: INTERRUPT-ON-CHANGE PORTE NEGATIVE EDGE REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	U-0	U-0	U-0
—	—	—	—	IOCEN3	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3 **IOCEN3:** Interrupt-on-Change PORTE Negative Edge Enable bits
1 = Interrupt-on-Change enabled on the pin for a negative going edge. IOCEFx bit and IOCIF flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin.

bit 2-0 **Unimplemented:** Read as ‘0’

19.3 Comparator Hysteresis

A selectable amount of separation voltage can be added to the input pins of each comparator to provide a hysteresis function to the overall operation. Hysteresis is enabled by setting the HYS bit of the CMxCON0 register.

See Comparator Specifications in Table 36-19: Comparator Specifications for more information.

19.4 Timer1 Gate Operation

The output resulting from a comparator operation can be used as a source for gate control of Timer1. See **Section 22.6 "Timer1 Gate"** for more information. This feature is useful for timing the duration or interval of an analog event.

It is recommended that the comparator output be synchronized to Timer1. This ensures that Timer1 does not increment while a change in the comparator is occurring.

19.4.1 COMPARATOR OUTPUT SYNCHRONIZATION

The output from a comparator can be synchronized with Timer1 by setting the SYNC bit of the CMxCON0 register.

Once enabled, the comparator output is latched on the falling edge of the Timer1 source clock. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 19-2) and the Timer1 Block Diagram (Figure 22-1) for more information.

19.5 Comparator Interrupt

An interrupt can be generated upon a change in the output value of the comparator for each comparator, a rising edge detector and a falling edge detector are present.

When either edge detector is triggered and its associated enable bit is set (INTP and/or INTN bits of the CMxCON1 register), the Corresponding Interrupt Flag bit (CxIF bit of the PIR2 register) will be set.

To enable the interrupt, you must set the following bits:

- ON and POL bits of the CMxCON0 register
- CxIE bit of the PIE2 register
- INTP bit of the CMxCON1 register (for a rising edge detection)
- INTN bit of the CMxCON1 register (for a falling edge detection)
- PEIE and GIE bits of the INTCON register

The associated interrupt flag bit, CxIF bit of the PIR2 register, must be cleared in software. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

Note:	Although a comparator is disabled, an interrupt can be generated by changing the output polarity with the POL bit of the CMxCON0 register, or by switching the comparator on or off with the ON bit of the CMxCON0 register.

19.6 Comparator Positive Input Selection

Configuring the PCH<3:0> bits of the CMxPSEL register directs an internal voltage reference or an analog pin to the non-inverting input of the comparator:

- CxIN+ analog pin
- Programmable ramp generator output
- DAC output
- FVR (Fixed Voltage Reference)
- VSS (Ground)

See **Section 14.0 "Fixed Voltage Reference (FVR)"** for more information on the Fixed Voltage Reference module.

See **Section 17.0 "5-Bit Digital-to-Analog Converter (DAC) Module"** for more information on the DAC input signal.

Any time the comparator is disabled (CxON = 0), all comparator inputs are disabled.

19.7 Comparator Negative Input Selection

The NCH<3:0> bits of the CMxNSEL register direct an analog input pin and internal reference voltage or analog ground to the inverting input of the comparator:

- CxIN- pin
- FVR (Fixed Voltage Reference)
- Analog Ground

Some inverting input selections share a pin with the operational amplifier output function. Enabling both functions at the same time will direct the operational amplifier output to the comparator inverting input.

Note:	To use CxINy+ and CxINy- pins as analog input, the appropriate bits must be set in the ANSEL register and the corresponding TRIS bits must also be set to disable the output drivers.

REGISTER 23-4: TxRST: TIMERx EXTERNAL RESET SIGNAL SELECTION REGISTER

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	RSEL<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RSEL<4:0>:** TimerX External Reset Signal Source Selection bits
See Table 23-4.

TABLE 23-4: EXTERNAL RESET SOURCES

RSEL<4:0>	Timer2	Timer4	Timer6	Timer8
11111	Reserved	Reserved	Reserved	Reserved
11110	Reserved	Reserved	Reserved	Reserved
11101	LC4_out	LC4_out	LC4_out	LC4_out
11100	LC3_out	LC3_out	LC3_out	LC3_out
11011	LC2_out	LC2_out	LC2_out	LC2_out
11010	LC1_out	LC1_out	LC1_out	LC1_out
11001	ZCD_out	ZCD_out	ZCD_out	ZCD_out
11000(1)	sync_C8OUT	sync_C8OUT	sync_C8OUT	sync_C8OUT
10111(1)	sync_C7OUT	sync_C7OUT	sync_C7OUT	sync_C7OUT
10110	sync_C6OUT	sync_C6OUT	sync_C6OUT	sync_C6OUT
10101	sync_C5OUT	sync_C5OUT	sync_C5OUT	sync_C5OUT
10100	sync_C4OUT	sync_C4OUT	sync_C4OUT	sync_C4OUT
10011	sync_C3OUT	sync_C3OUT	sync_C3OUT	sync_C3OUT
10010	sync_C2OUT	sync_C2OUT	sync_C2OUT	sync_C2OUT
10001	sync_C1OUT	sync_C1OUT	sync_C1OUT	sync_C1OUT
10000(1)	PWM12_out	PWM12_out	PWM12_out	PWM12_out
01111	PWM11_out	PWM11_out	PWM11_out	PWM11_out
01110	PWM6_out	PWM6_out	PWM6_out	PWM6_out
01101	PWM5_out	PWM5_out	PWM5_out	PWM5_out
01100(1)	PWM10_out	PWM10_out	PWM10_out	PWM10_out
01011	PWM9_out	PWM9_out	PWM9_out	PWM9_out
01010	PWM4_out	PWM4_out	PWM4_out	PWM4_out
01001	PWM3_out	PWM3_out	PWM3_out	PWM3_out
01000(1)	CCP8_out	CCP8_out	CCP8_out	CCP8_out
00111	CCP7_out	CCP7_out	CCP7_out	CCP7_out
00110	CCP2_out	CCP2_out	CCP2_out	CCP2_out
00101	CCP1_out	CCP1_out	CCP1_out	CCP1_out
00100	TMR8_postscaled	TMR8_postscaled	TMR8_postscaled	Reserved
00011	TMR6_postscaled	TMR6_postscaled	Reserved	TMR6_postscaled
00010	TMR4_postscaled	Reserved	TMR4_postscaled	TMR4_postscaled
00001	Reserved	TMR2_postscaled	TMR2_postscaled	TMR2_postscaled
00000	Pin selected byT2INPPS	Pin selected by T4INPPS	Pin selected by T6INPPS	Pin selected by T6INPPS

Note 1: PIC16LF1777/9 only.

REGISTER 27-7: COGxFIS0: COG FALLING EVENT INPUT SELECTION REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
FIS7	FIS6	FIS5	FIS4	FIS3	FIS2	FIS1	FIS0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-0 **FIS<7:0>:** Falling Event Input Source <n> Enable bits(1). See Table 27-5.
1 = Source <n> output is enabled as a falling event input
0 = Source <n> output has no effect on the falling event

Note 1: Any combination of <n> bits can be selected.

REGISTER 27-8: COGxFIS1: COG FALLING EVENT INPUT SELECTION REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
FIS15	FIS14	FIS13	FIS12	FIS11	FIS10	FIS9	FIS8
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 15-8 **FIS<15:8>:** Falling Event Input Source <n> Enable bits(1). See Table 27-5.
1 = Source <n> output is enabled as a falling event input
0 = Source <n> output has no effect on the falling event

Note 1: Any combination of <n> bits can be selected.

TABLE 31-7: LOW CARRIER SOURCE

CH<4:0>	Carrier Source PIC16(L)F1778	Carrier Source PIC16(L)F1777/9
11111	Reserved	Reserved
11110	Reserved	Reserved
11101	Reserved	Reserved
11100	Reserved	Reserved
11011	Reserved	Reserved
11010	Reserved	Reserved
11001	Reserved	Reserved
11000	Reserved	Reserved
10111	Reserved	Reserved
10110	Reserved	Reserved
10101	Reserved	Reserved
10100	Reserved	Reserved
10011	Reserved	Reserved
10010	LC4_out	LC4_out
10001	LC3_out	LC3_out
10000	LC2_out	LC2_out
01111	LC1_out	LC1_out
01110	Reserved	PWM12_out
01101	PWM11_out	PWM11_out
01100	PWM6_out	PWM6_out
01011	PWM5_out	PWM5_out
01010	Reserved	PWM10_out
01001	PWM9_out	PWM9_out
01000	PWM4_out	PWM4_out
00111	PWM3_out	PWM3_out
00110	Reserved	CCP8_out
00101	CCP7_out	CCP7_out
00100	CCP2_out	CCP2_out
00011	CCP1_out	CCP1_out
00010	HFINTOSC	HFINTOSC
00001	FOSC	FOSC
00000	MDxMODPPS pin selection	MDxMODPPS pin selection

TABLE 31-8: SUMMARY OF REGISTERS ASSOCIATED WITH DATA SIGNAL MODULATOR MODE(1)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
MDxCARH	—	—	—	CH<4:0>					436
MDxCARL	—	—	—	CL<4:0>					438
MDxSRC	—	—	—	MS<4:0>					434
MDxCON0	EN	—	OUT	OPOL	—	—	—	BIT	433
MDxCON1	—	—	CHPOL	CHSYNC	—	—	CLPOL	CLSYNC	433

Legend: — = unimplemented, read as '0'. Shaded cells are not used in the Data Signal Modulator mode.

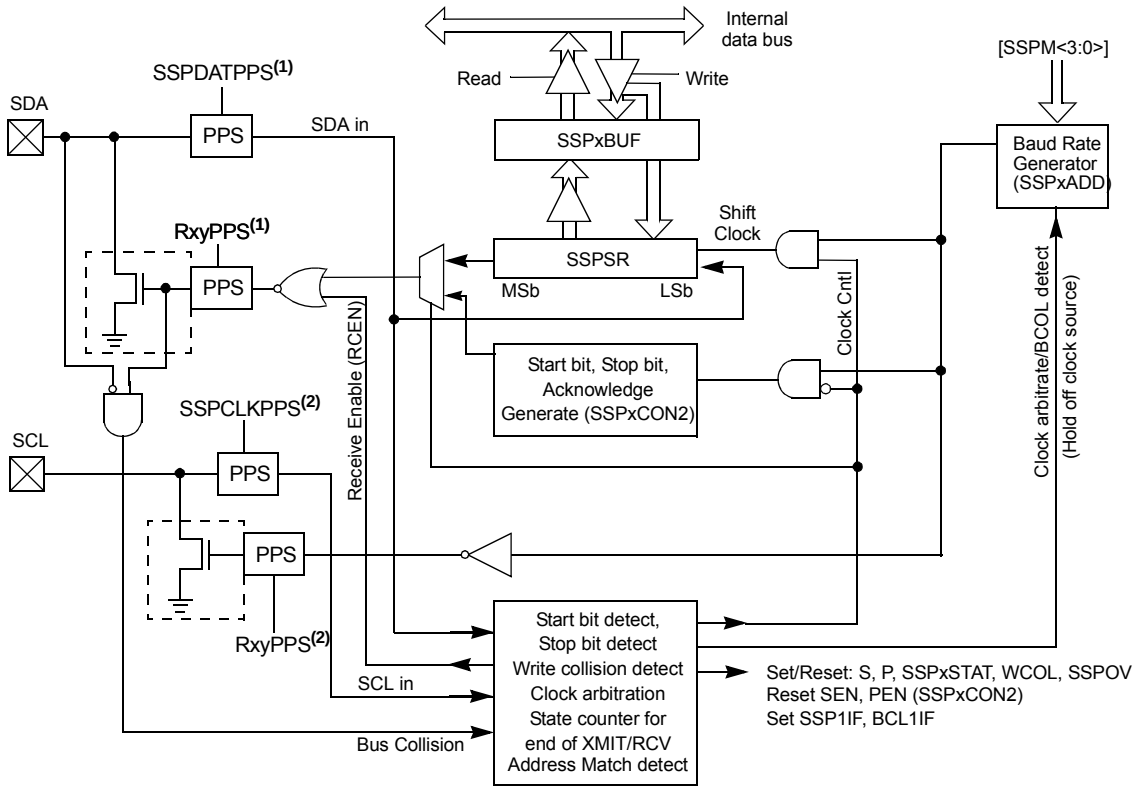
Note 1: DSM4 available on PIC16LF1777/9 only.

The I^2C interface supports the following modes and features:

- Master mode
- Slave mode
- Byte NACKing (Slave mode)
- Limited multi-master support
- 7-bit and 10-bit addressing
- Start and Stop interrupts
- Interrupt masking
- Clock stretching
- Bus collision detection
- General call address matching
- Address masking
- Address Hold and Data Hold modes
- Selectable SDA hold times

Figure 32-2 is a block diagram of the I^2C interface module in Master mode. Figure 32-3 is a diagram of the I^2C interface module in Slave mode.

FIGURE 32-2: MSSP BLOCK DIAGRAM (I^2C MASTER MODE)



Note 1: SDA pin selections must be the same for input and output

2: SCL pin selections must be the same for input and output

32.4.5 START CONDITION

The I^2C specification defines a Start condition as a transition of SDA from a high to a low state while SCL line is high. A Start condition is always generated by the master and signifies the transition of the bus from an Idle to an Active state. Figure 32-12 shows wave forms for Start and Stop conditions.

A bus collision can occur on a Start condition if the module samples the SDA line low before asserting it low. This does not conform to the I^2C Specification that states no bus collision can occur on a Start.

32.4.6 STOP CONDITION

A Stop condition is a transition of the SDA line from low-to-high state while the SCL line is high.

Note: At least one SCL low time must appear before a Stop is valid, therefore, if the SDA line goes low then high again while the SCL line stays high, only the Start condition is detected.

32.4.7 RESTART CONDITION

A Restart is valid any time that a Stop would be valid. A master can issue a Restart if it wishes to hold the bus after terminating the current transfer. A Restart has the same effect on the slave that a Start would, resetting all slave logic and preparing it to clock in an address. The master may want to address the same or another slave. Figure 32-13 shows the wave form for a Restart condition.

In 10-bit Addressing Slave mode a Restart is required for the master to clock data out of the addressed slave. Once a slave has been fully addressed, matching both high and low address bytes, the master can issue a Restart and the high address byte with the R/$\overline{W}$ bit set. The slave logic will then hold the clock and prepare to clock out data.

After a full match with R/$\overline{W}$ clear in 10-bit mode, a prior match flag is set and maintained until a Stop condition, a high address with R/$\overline{W}$ clear, or high address match fails.

32.4.8 START/STOP CONDITION INTERRUPT MASKING

The SCIE and PCIE bits of the SSPxCON3 register can enable the generation of an interrupt in Slave modes that do not typically support this function. Slave modes where interrupt on Start and Stop detect are already enabled, these bits will have no effect.

FIGURE 32-12: I^2C START AND STOP CONDITIONS

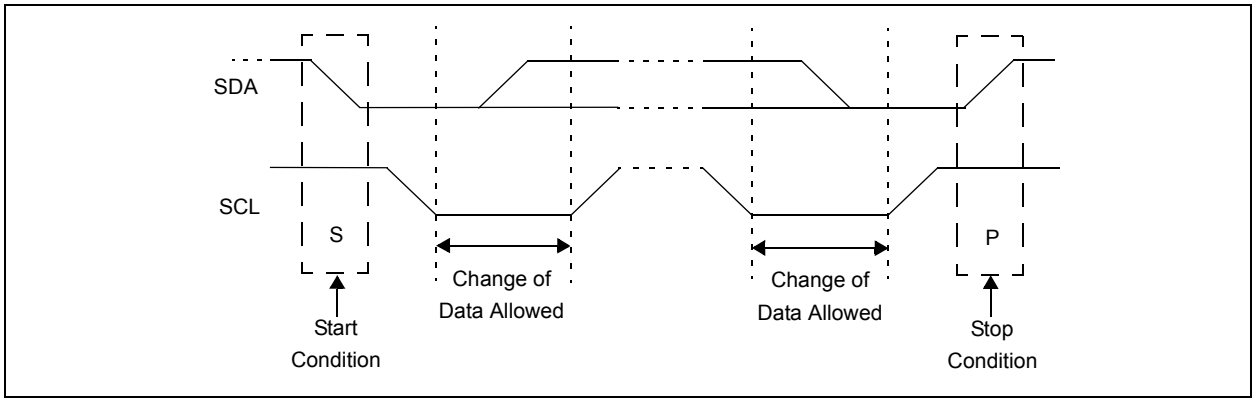


FIGURE 32-13: I^2C RESTART CONDITION

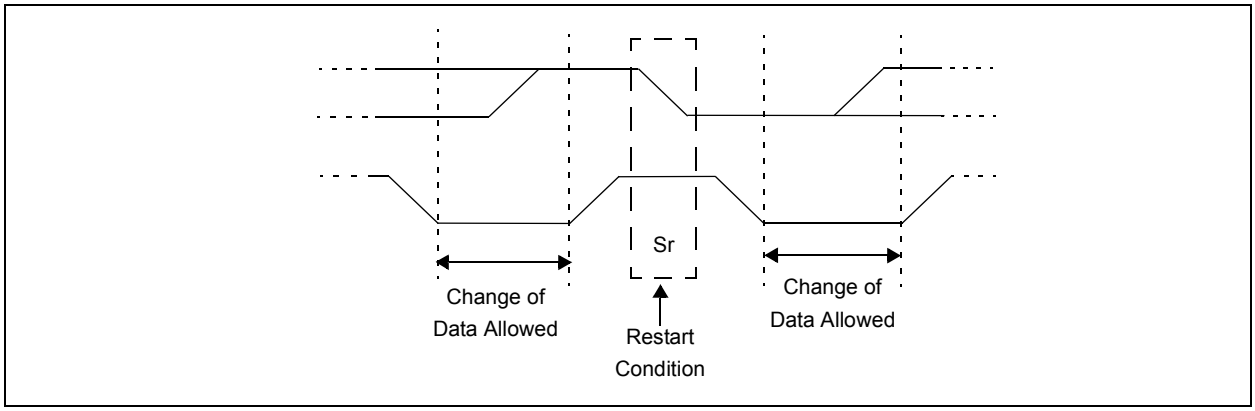


FIGURE 32-14: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 0, DHEN = 0)

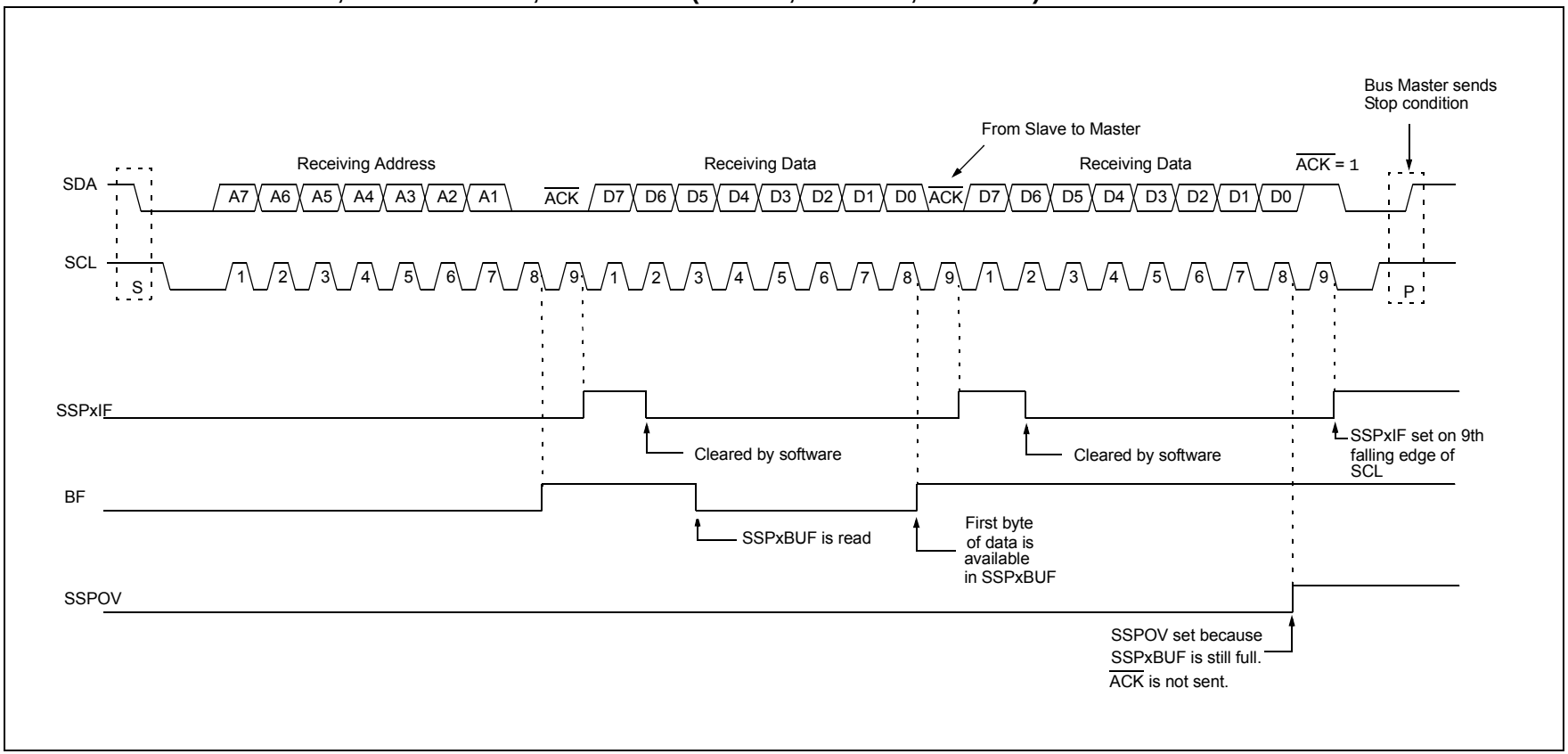


FIGURE 35-1: GENERAL FORMAT FOR INSTRUCTIONS

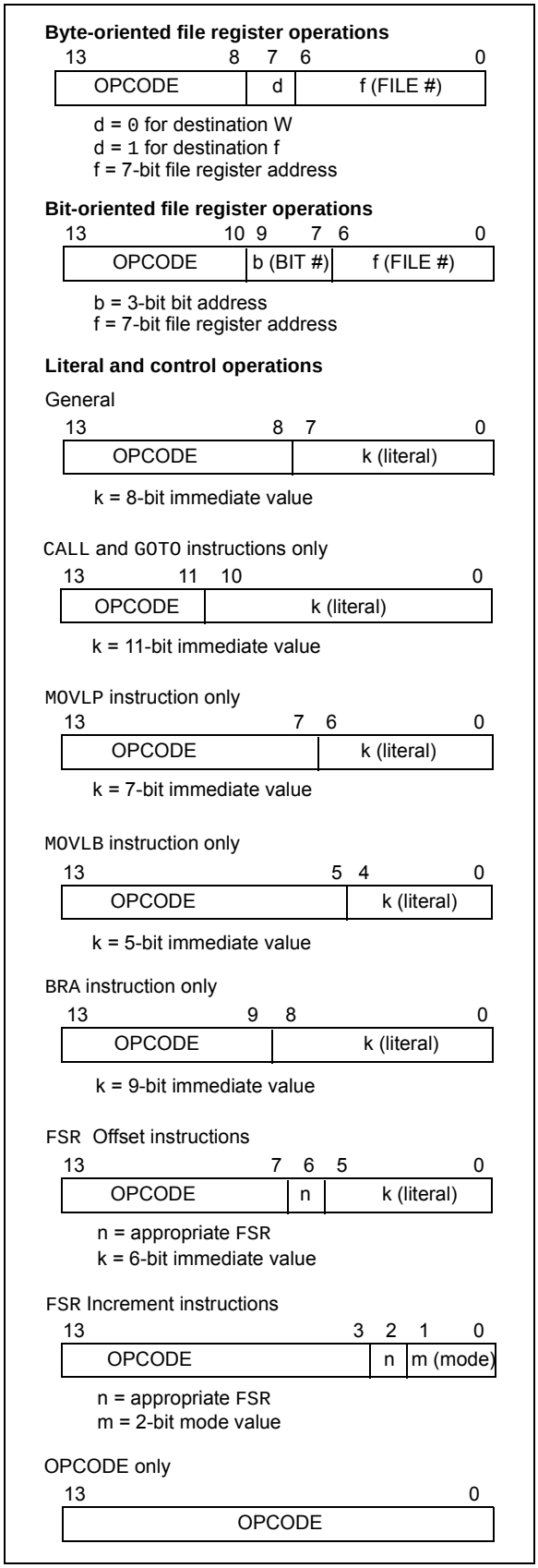


TABLE 36-6: THERMAL CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)					
Param No.	**Sym.**	**Characteristic**	**Typ.**	**Units**	**Conditions**
TH01	θ_{JA}	Thermal Resistance Junction to Ambient	60.0	°C/W	28-pin SPDIP package
			80.0	°C/W	28-pin SOIC package
			90.0	°C/W	28-pin SSOP package
			48	°C/W	28-pin UQFN 4x4mm package
			47.2	°C/W	40-pin PDIP package
			46.0	°C/W	44-pin TQFP package
			41.0	°C/W	40-pin UQFN 5x5mm package
TH02	θ_{JC}	Thermal Resistance Junction to Case	31.4	°C/W	28-pin SPDIP package
			24	°C/W	28-pin SOIC package
			24	°C/W	28-pin SSOP package
			12	°C/W	28-pin UQFN 4x4mm package
			24.70	°C/W	40-pin PDIP package
			14.5	°C/W	44-pin TQFP package
			5.5	°C/W	40-pin UQFN 5x5mm package
TH03	T_{JMAX}	Maximum Junction Temperature	150	°C	
TH04	PD	Power Dissipation	—	W	$PD = P_{INTERNAL} + P_{I/O}$
TH05	$P_{INTERNAL}$	Internal Power Dissipation	—	W	$P_{INTERNAL} = I_{DD} \times V_{DD}$ (1)
TH06	$P_{I/O}$	I/O Power Dissipation	—	W	$P_{I/O} = \Sigma (I_{OL} * V_{OL}) + \Sigma (I_{OH} * (V_{DD} - V_{OH}))$
TH07	P_{DER}	Derated Power	—	W	$P_{DER} = P_{DMAX} (T_J - T_A)/\theta_{JA}$ (2)

Note 1: I_{DD} is current to run the chip alone without driving any load on the output pins.

2: T_A = Ambient Temperature, T_J = Junction Temperature