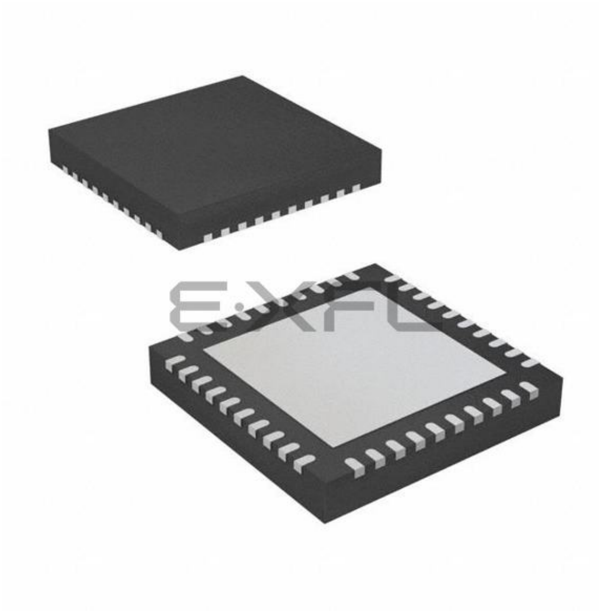
Microchip Technology - PIC16F1779-E/MV Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 28x10b; D/A 4x5b, 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1779-e-mv

TABLE 1-3: PIC16(L)F1777/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RE1/AN6/DAC6OUT1/ DAC6REF1-/DAC8REF1-	RE1	TTL/ST	CMOS	General purpose I/O.
	AN6	AN	—	ADC Channel 6 input.
	DAC6OUT1	—	AN	DAC6 voltage output.
	DAC6REF1-	AN	—	DAC6 negative reference.
	DAC8REF1-	AN	—	DAC8 negative reference.
RE2/AN7/DAC8OUT1	RE2	TTL/ST	CMOS	General purpose I/O.
	AN7	AN	—	ADC Channel 7 input.
	DAC8OUT1	—	AN	DAC8 voltage output.
RE3/$\overline{\text{MCLR}}$/VPP	RE3	TTL/ST	CMOS	General purpose input.
	$\overline{\text{MCLR}}$	ST	—	Master clear input.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.
OUT(2)	C1OUT		CMOS	Comparator 1 output.
	C2OUT		CMOS	Comparator 2 output.
	C3OUT		CMOS	Comparator 3 output.
	C4OUT		CMOS	Comparator 4 output.
	C5OUT		CMOS	Comparator 5 output.
	C6OUT		CMOS	Comparator 6 output.
	C7OUT		CMOS	Comparator 7 output.
	C8OUT		CMOS	Comparator 8 output.
	CCP1		CMOS	Compare/PWM1 output.
	CCP2		CMOS	Compare/PWM2 output.
	CCP7		CMOS	Compare/PWM7 output.
	CCP8		CMOS	Compare/PWM8 output.
	MD1OUT		CMOS	Data signal modulator 1 output.
	MD2OUT		CMOS	Data signal modulator 2 output.
	MD3OUT		CMOS	Data signal modulator 3 output.
	MD4OUT		CMOS	Data signal modulator 4 output.
	PWM3OUT		CMOS	PWM3 output.
	PWM4OUT		CMOS	PWM4 output.
	PWM5OUT		CMOS	PWM5 output.
	PWM6OUT		CMOS	PWM6 output.
	PWM9OUT		CMOS	PWM9 output.
	PWM10OUT		CMOS	PWM10 output.
	PWM11OUT		CMOS	PWM11 output.
	PWM12OUT		CMOS	PWM12 output.
	COG1A		CMOS	Complementary output generator 1 output A.
	COG1B		CMOS	Complementary output generator 1 output B.
	COG1C		CMOS	Complementary output generator 1 output C.
	COG1D		CMOS	Complementary output generator 1 output D.
	COG2A		CMOS	Complementary output generator 2 output A.

Legend:	AN = Analog input or output	CMOS = CMOS compatible input or output	OD = Open-Drain
	TTL = TTL compatible input	ST = Schmitt Trigger input with CMOS levels	I^{2}C = Schmitt Trigger input with I^{2}C
	HP = High Power	XTAL = Crystal levels	

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 12											
60Ch to 613h	—	Unimplemented								—	—
60Ch	DAC8CON0[(3)]	EN	—	OE1	OE2	PSS<1:0>		NSS1	NSS0	0-00 0000	0-00 0000
60Dh	DAC8REF[(3)]	—	—	—	REF<4:0>					---0 0000	0000 0000
60Eh	PRG4RTSS[(3)]	—	—	—	—	RTSS<3:0>				---- 0000	---- 0000
60Fh	PRG4FTSS[(3)]	—	—	—	—	FTSS<3:0>				---- 0000	---- 0000
610h	PRG4INS[(3)]	—	—	—	—	INS<3:0>				---- 0000	---- 0000
611h	PRG4CON0[(3)]	EN	—	FEDG	REDG	MODE<1:0>		OS	GO	0-000 0000	0-00 0000
612h	PRG4CON1[(3)]	—	—	—	—	—	RDY	FPOL	RPOL	---- -000	---- -000
613h	PRG4CON2[(3)]	—	—	—	ISET<4:0>					---0 0000	---0 0000
614h	PWM3DCL	DC<1:0>		—	—	—	—	—	—	xx-- ----	uu-- ----
615h	PWM3DCH	DC<9:2>								xxxx xxxx	uuuu uuuu
616h	PWM3CON	EN	—	OUT	POL	—	—	—	—	0-00 ----	0-00 ----
617h	PWM4DCL	DC<1:0>		—	—	—	—	—	—	xx-- ----	uu-- ----
618h	PWM4DCH	DC<9:2>								xxxx xxxx	uuuu uuuu
619h	PWM4CON	EN	—	OUT	POL	—	—	—	—	0-00 ----	0-00 ----
61Ah	PWM9DCL	DC<1:0>		—	—	—	—	—	—	xx-- ----	uu-- ----
61Bh	PWM9DCH	DC<9:2>								xxxx xxxx	uuuu uuuu
61Ch	PWM9CON	EN	—	OUT	POL	—	—	—	—	0-00 ----	0-00 ----
61Dh	PWM10DCL[(3)]	DC<1:0>		—	—	—	—	—	—	xx-- ----	uu-- ----
61Eh	PWM10DCH[(3)]	DC<9:2>								xxxx xxxx	uuuu uuuu
61Fh	PWM10CON[(3)]	EN	—	OUT	POL	—	—	—	—	0-00 ----	0-00 ----

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

4.2 Register Definitions: Configuration Words

REGISTER 4-1: CONFIG1: CONFIGURATION WORD 1

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
FCMEN	IESO	$\overline{\text{CLKOUTEN}}$	BOREN<1:0>		—
bit 13					bit 8

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
$\overline{\text{CP}}$(1)	MCLRE	$\overline{\text{PWRTE}}$	WDTE<1:0>		FOSC<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘1’
‘0’ = Bit is cleared	‘1’ = Bit is set	-n = Value when blank or after Bulk Erase

bit 13 **FCMEN:** Fail-Safe Clock Monitor Enable bit
1 = ON Fail-Safe Clock Monitor and internal/external switchover are both enabled
0 = OFF Fail-Safe Clock Monitor is disabled

bit 12 **IESO:** Internal External Switchover bit
1 = ON Internal/External Switchover mode is enabled
0 = OFF Internal/External Switchover mode is disabled

bit 11 **$\overline{\text{CLKOUTEN}}$:** Clock Out Enable bit
If FOSC Configuration bits are set to LP, XT, HS modes:
This bit is ignored, CLKOUT function is disabled. Oscillator function on the CLKOUT pin.
All other FOSC modes:
1 = ON CLKOUT function is disabled. I/O function on the CLKOUT pin.
0 = OFF CLKOUT function is enabled on the CLKOUT pin.

bit 10-9 **BOREN<1:0>:** Brown-out Reset Enable bits
11 = ON BOR enabled
10 = NSLEEP BOR enabled during operation and disabled in Sleep
01 = SBODEN BOR controlled by SBOREN bit of the BORCON register
00 = OFF BOR disabled

bit 8 **Unimplemented:** Read as ‘1’

bit 7 **$\overline{\text{CP}}$:** Code Protection bit(1)
1 = OFF Program memory code protection is disabled
0 = ON Program memory code protection is enabled

bit 6 **MCLRE:** $\overline{\text{MCLR}}$/VPP Pin Function Select bit
If LVP bit = 1:
This bit is ignored.
If LVP bit = 0:
1 = ON $\overline{\text{MCLR}}$/VPP pin function is $\overline{\text{MCLR}}$; Weak pull-up enabled.
0 = OFF $\overline{\text{MCLR}}$/VPP pin function is digital input; $\overline{\text{MCLR}}$ internally disabled; Weak pull-up under control of WPUA3 bit.

bit 5 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit
1 = OFF PWRT disabled
0 = ON PWRT enabled

bit 4-3 **WDTE<1:0>:** Watchdog Timer Enable bit
11 = ON WDT enabled
10 = NSLEEP WDT enabled while running and disabled in Sleep
01 = SWDTEN WDT controlled by the SWDTEN bit in the WDTCON register
00 = OFF WDT disabled

5.2.2.7 Internal Oscillator Clock Switch Timing

When switching between the HFINTOSC, MFINTOSC and the LFINTOSC, the new oscillator may already be shut down to save power (see Figure 5-7). If this is the case, there is a delay after the IRCF<3:0> bits of the OSCCON register are modified before the frequency selection takes place. The OSCSTAT register will reflect the current active status of the HFINTOSC, MFINTOSC and LFINTOSC oscillators. The sequence of a frequency selection is as follows:

1. IRCF<3:0> bits of the OSCCON register are modified.
2. If the new clock is shut down, a clock start-up delay is started.
3. Clock switch circuitry waits for a falling edge of the current clock.
4. The current clock is held low and the clock switch circuitry waits for a rising edge in the new clock.
5. The new clock is now active.
6. The OSCSTAT register is updated as required.
7. Clock switch is complete.

See Figure 5-7 for more details.

If the internal oscillator speed is switched between two clocks of the same source, there is no start-up delay before the new frequency is selected. Clock switching time delays are shown in Table 5-1.

Start-up delay specifications are located in the oscillator tables of **Section 36.0 “Electrical Specifications”**.

REGISTER 5-3: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	TUN<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **TUN<5:0>:** Frequency Tuning bits
100000 = Minimum frequency
•
•
•
111111 =
000000 = Oscillator module is running at the factory-calibrated frequency
000001 =
•
•
•
011110 =
011111 = Maximum frequency

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	SPLLEN	IRCF<3:0>				—	SCS<1:0>		116
OSCSTAT	SOSCR	PLLR	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS	117
OSCTUNE	—	—	TUN<5:0>						118
PIR2	OSFIF	C2IF	C1IF	COG1IF	BCL1IF	C4IF	C3IF	CCP2IF	140
PIE2	OSFIE	C2IE	C1IE	COG1IE	BCL1IE	C4IE	C3IE	CCP2IE	134
T1CON	CS<1:0>		CKPS<1:0>		OSCEN	$\overline{\text{SYNC}}$	—	ON	283

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used by clock sources.

TABLE 5-3: SUMMARY OF CONFIGURATION WORD WITH CLOCK SOURCES

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	IESO	$\overline{\text{CLKOUTEN}}$	BOREN<1:0>		—	95
	7:0	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE<1:0>		FOSC<2:0>			

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used by clock sources.

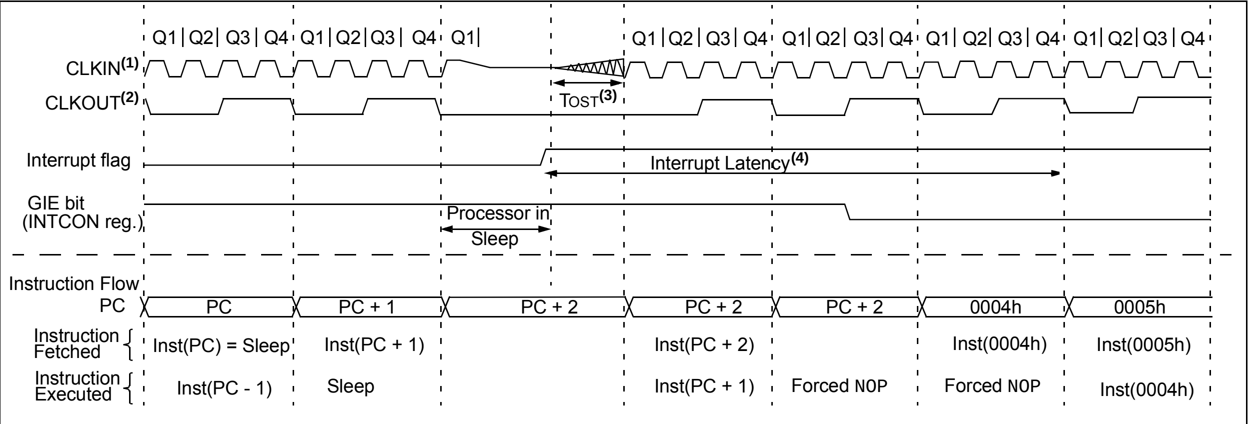
8.1.1 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction
  - SLEEP instruction will execute as a NOP
  - WDT and WDT prescaler will not be cleared
  - $\overline{\text{TO}}$ bit of the STATUS register will not be set
  - $\overline{\text{PD}}$ bit of the STATUS register will not be cleared
- If the interrupt occurs **during or after** the execution of a SLEEP instruction
  - SLEEP instruction will be completely executed
  - Device will immediately wake-up from Sleep
  - WDT and WDT prescaler will be cleared
  - $\overline{\text{TO}}$ bit of the STATUS register will be set
  - $\overline{\text{PD}}$ bit of the STATUS register will be cleared

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the $\overline{\text{PD}}$ bit. If the $\overline{\text{PD}}$ bit is set, the SLEEP instruction was executed as a NOP.

FIGURE 8-1: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: External clock. High, Medium, Low mode assumed.

2: CLKOUT is shown here for timing reference.

3: TOST = 1024 TOSC. This delay does not apply to EC, RC and INTOSC Oscillator modes or Two-Speed Start-up (see **Section 5.4 “Two-Speed Clock Start-up Mode”**.

4: GIE = 1 assumed. In this case after wake-up, the processor calls the ISR at 0004h. If GIE = 0, execution will continue in-line.

11.1.7 PORTA FUNCTIONS AND OUTPUT PRIORITIES

Each PORTA pin is multiplexed with other functions.

Each pin defaults to the PORT latch data after reset. Other functions are selected with the peripheral pin select logic. See **Section 12.0 “Peripheral Pin Select (PPS) Module”** for more information.

Analog input functions, such as ADC and comparator inputs are not shown in the peripheral pin select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELA register. Digital output functions may continue to control the pin when it is in Analog mode.

REGISTER 11-20: LATC: PORTC DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **LATC<7:0>**: PORTC Output Latch Value bits

REGISTER 11-21: ANSELC: PORTC ANALOG SELECT REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	U-0	U-0
ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-2 **ANSC<7:2>**: Analog Select between Analog or Digital Function on pins RC<7:2>[(1)]
1 = Analog input. Pin is assigned as analog input[(1)]. Digital input buffer disabled.
0 = Digital I/O. Pin is assigned to port or digital special function.

bit 1-0 **Unimplemented:** Read as ‘0’

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 13-7: IOCCP: INTERRUPT-ON-CHANGE PORTC POSITIVE EDGE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
IOCCP7	IOCCP6	IOCCP5	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **IOCCP<7:0>:** Interrupt-on-Change PORTC Positive Edge Enable bits
1 = Interrupt-on-Change enabled on the pin for a positive going edge. IOCCFx bit and IOCIF flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 13-8: IOCCN: INTERRUPT-ON-CHANGE PORTC NEGATIVE EDGE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
IOCCN7	IOCCN6	IOCCN5	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **IOCCN<7:0>:** Interrupt-on-Change PORTC Negative Edge Enable bits
1 = Interrupt-on-Change enabled on the pin for a negative going edge. IOCCFx bit and IOCIF flag will be set upon detecting an edge.
0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 13-9: IOCCF: INTERRUPT-ON-CHANGE PORTC FLAG REGISTER

R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
IOCCF7	IOCCF6	IOCCF5	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HS - Bit is set in hardware

bit 7-0 **IOCCF<7:0>:** Interrupt-on-Change PORTC Flag bits
1 = An enabled change was detected on the associated pin.
Set when IOCCPx = 1 and a rising edge was detected on RCx, or when IOCCNx = 1 and a falling edge was detected on RCx.
0 = No change was detected, or the user cleared the detected change.

26.4 Reload Operation

Four of the PWM module control register pairs and one control bit are double buffered so that all can be updated simultaneously. These include:

- PWMxPHH:PWMxPHL register pair
- PWMxDCH:PWMxDCL register pair
- PWMxPRH:PWMxPRL register pair
- PWMxOFH:PWMxOFL register pair
- ODO control bit

When written to, these registers do not immediately affect the operation of the PWM. By default, writes to these registers will not be loaded into the PWM operating buffer registers until after the arming conditions are met. The arming control has two methods of operation:

- Immediate
- Triggered

The LDT bit of the PWMxLDCON register controls the arming method. Both methods require the LDA bit to be set. All four buffer pairs will load simultaneously at the loading event.

26.4.1 IMMEDIATE RELOAD

When the LDT bit is clear then the Immediate mode is selected and the buffers will be loaded at the first period event after the LDA bit is set. Immediate reloading is used when a PWM module is operating stand-alone or when the PWM module is operating as a master to other slave PWM modules.

26.4.2 TRIGGERED RELOAD

When the LDT bit is set then the Triggered mode is selected and a trigger event is required for the LDA bit to take effect. The trigger source is the buffer load event of one of the other PWM modules in the device. The triggering source is selected by the LDS<1:0> bits of the PWMxLDCON register. The buffers will be loaded at the first period event following the trigger event. Triggered reloading is used when a PWM module is operating as a slave to another PWM and it is necessary to synchronize the buffer reloads in both modules.

Note 1: The buffer load operation clears the LDA bit.

2: If the LDA bit is set at the same time as PWMxTMR = PWMxPR, the LDA bit is ignored until the next period event. Such is the case when triggered reload is selected and the triggering event occurs simultaneously with the target's period event

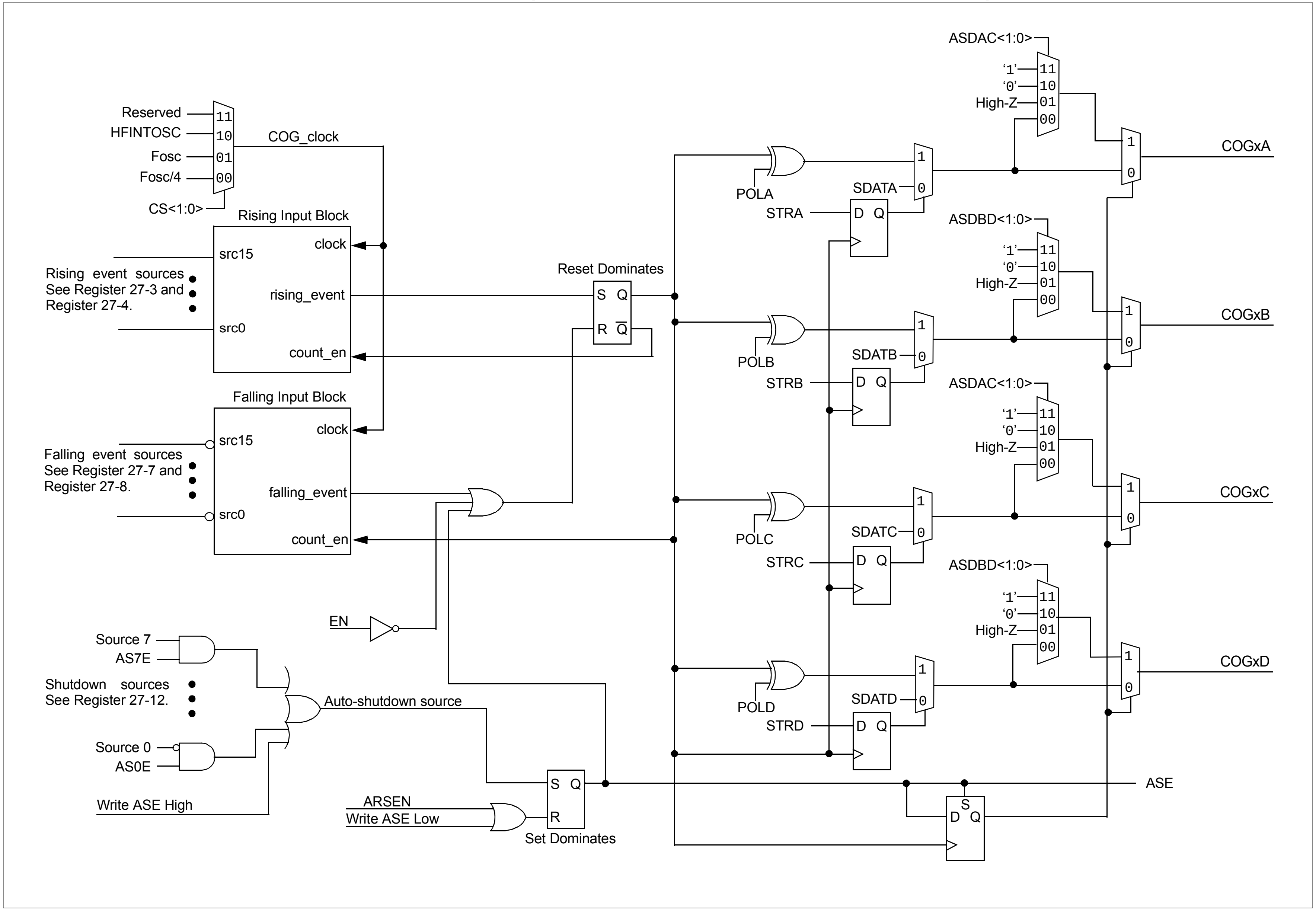
26.5 Operation in Sleep Mode

Each PWM module will continue to operate in Sleep mode when either the HFINTOSC or LFINTOSC is selected as the clock source by PWMxCLKCON<1:0>.

26.6 Interrupts

Each PWM module has four independent interrupts based on the phase, duty cycle, period, and offset match events. The interrupt flag is set on the rising edge of each of these signals. Refer to Figures 26-8 and 26-12 for detailed timing diagrams of the match signals.

FIGURE 27-3: SIMPLIFIED COG BLOCK DIAGRAM (SYNCHRONOUS STEERED PWM MODE, MD = 1)



27.11 Buffer Updates

Changes to the phase, dead-band, and blanking count registers need to occur simultaneously during COG operation to avoid unintended operation that may occur as a result of delays between each register write. This is accomplished with the LD bit of the COGxCON0 register and double buffering of the phase, blanking and dead-band count registers.

Before the COG module is enabled, writing the count registers loads the count buffers without need of the LD bit. However, when the COG is enabled, the count buffer updates are suspended after writing the count registers until after the LD bit is set. When the LD bit is set, the phase, dead-band and blanking register values are transferred to the corresponding buffers synchronous with COG operation. The LD bit is cleared by hardware when the transfer is complete.

27.12 Input and Output Pin Selection

The COG has one selection for an input from a device pin. That one input can be used as rising and falling event source or a fault source. The COGxINPPS register is used to select the pin. Refer to registers xxxPPS (Register 12-1) and RxyPPS (Register 12-2).

The pin PPS control registers are used to enable the COG outputs. Any combination of outputs to pins is possible including multiple pins for the same output. See the RxyPPS control register and **Section 12.2 "PPS Outputs"** for more details.

27.13 Operation During Sleep

The COG continues to operate in Sleep provided that the COG_clock, rising event, and falling event sources remain active.

The HFINTSOC remains active during Sleep when the COG is enabled and the HFINTOSC is selected as the COG_clock source.

27.14 Configuring the COG

The following steps illustrate how to properly configure the COG to ensure a synchronous start with the rising event input:

1. If a pin is to be used for the COG fault or event input, use the COGxINPPS register to configure the desired pin.
2. Clear all ANSEL register bits associated with pins that are used for COG functions.
3. Ensure that the TRIS control bits corresponding to the COG outputs to be used are set so that all are configured as inputs. The COG module will enable the output drivers as needed later.
4. Clear the EN bit, if not already cleared.
5. Set desired dead-band times with the COGxDBR and COGxDBF registers and select the source with the RDBS and FDBS bits of the COGxCON1 register.
6. Set desired blanking times with the COGxBLKR and COGxBLKF registers.
7. Set desired phase delay with the COGxPHR and COGxPHF registers.
8. Select the desired shutdown sources with the COGxASD1 register.
9. Setup the following controls in COGxASD0 auto-shutdown register:
   - Select both output override controls to the desired levels (this is necessary, even if not using auto-shutdown because start-up will be from a shutdown state).
   - Set the ASE bit and clear the ARSEN bit.
10. Select the desired rising and falling event sources with the COGxRIS0, COGxRIS1, COGxFIS0, and COGxFIS1 registers.
11. Select the desired rising and falling event modes with the COGxRSIM0, COGxRSIMI1, COGxFSIM0, and COGxFSIM1 registers.
12. Configure the following controls in the COGxCON1 register:
    - Set the polarity for each output
    - Select the desired dead-band timing sources
13. Configure the following controls in the COGxCON0 register:
    - Set the desired operating mode
    - Select the desired clock source
14. If one of the steering modes is selected then configure the following controls in the COGxSTR register:
    - Set the steering bits of the outputs to be used.
    - Set the desired static levels.
15. Set the EN bit.
16. Set the pin PPS controls to direct the COG outputs to the desired pins.
17. If auto-restart is to be used, set the ARSEN bit and the ASE will be cleared automatically. Otherwise, clear the ASE bit to start the COG.

REGISTER 27-12: COGxASD1: COG AUTO-SHUTDOWN CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
AS7E	AS6E	AS5E	AS4E	AS3E	AS2E	AS1E	AS0E
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-0 **AS<7:0>E:** Auto-shutdown Source <n> Enable bits[1]. See Table 27-6.
1 = COGx is shutdown when source <n> output is low
0 = Source <n> has no effect on shutdown

Note 1: Any combination of <n> bits can be selected.

TABLE 27-6: AUTO-SHUTDOWN SOURCES

Bit <n>	COG1	COG2	COG3[2]	COG3[3]	COG4[2]
7	TMR4_postscaled[1]	TMR4_postscaled[1]	TMR8_postscaled[1]	TMR8_postscaled[1]	TMR8_postscaled[1]
6	TMR2_postscaled[1]	TMR2_postscaled[1]	TMR6_postscaled[1]	TMR6_postscaled[1]	TMR6_postscaled[1]
5	LC2_out	LC2_out	LC4_out	LC4_out	LC4_out
4	sync_CM4_out	sync_CM4_out	sync_CM8_out	sync_CM6_out	sync_CM8_out
3	sync_CM3_out	sync_CM3_out	sync_CM7_out	sync_CM5_out	sync_CM7_out
2	sync_CM2_out	sync_CM2_out	sync_CM6_out	sync_CM2_out	sync_CM6_out
1	sync_CM1_out	sync_CM1_out	sync_CM5_out	sync_CM1_out	sync_CM5_out
0	Pin selected by COG1PPS	Pin selected by COG2PPS	Pin selected by COG3PPS	Pin selected by COG3PPS	Pin selected by COG4PPS

Note 1: Shutdown when source is high.
2: PIC16(L)F1777/9 only.
3: PIC16(L)F1778 only.

30.10 Register Definitions: Slope Compensation Control

Long bit name prefixes for the PRG peripherals are shown in Table 30-2. Refer to **Section 1.1 "Register and Bit naming conventions"** for more information

TABLE 30-2:

Peripheral	Bit Name Prefix
PRG1	RG1
PRG2	RG2
PRG3	RG3
PRG4[1]	RG4

Note 1: PIC16(L)F1777/9 only.

REGISTER 30-1: PRGxCON0: PROGRAMMABLE RAMP GENERATOR CONTROL 0 REGISTER

R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EN	—	FEDG	REDG	MODE<1:0>		OS	GO
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = value depends on configuration bits

bit 7 **EN:** Programmable Ramp Generator Enable bit
1 = PRG module is enabled
0 = PRG module is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **FEDG:** Set_falling Input Mode Select bit
1 = Set_falling timing input is edge sensitive
0 = Set_falling timing input is level sensitive

bit 4 **REDG:** Set_rising Input Mode Select bit
1 = Set_rising timing input is edge sensitive
0 = Set_rising timing input is level sensitive

bit 3-2 **MODE<1:0>:** Programmable Ramp Generator Mode Selection bits
11 = Reserved
10 = Rising Ramp Generator
01 = Alternating Rising/Falling Ramp Generator
00 = Slope Compensation

bit 1 **OS:** One-Shot Enable bit
1 = One-shot is enabled. Minimum capacitor discharge is internally timed by one-shot.
0 = One-shot is disabled. Capacitor is discharged when timing input is true.

bit 0 **GO:** Ramp Generation Control Start bit
if EN = 1:
1 = Slope or Ramp function is operating
0 = Slope or Ramp function is not operating. All current source current source switches are open and capacitor discharge switch is closed.
If EN = 0:
This bit is forced to 0

32.6.13.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

a) SDA or SCL are sampled low at the beginning of the Start condition (Figure 32-33).

b) SCL is sampled low before SDA is asserted low (Figure 32-34).

During a Start condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low, or the SCL pin is already low, then all of the following occur:

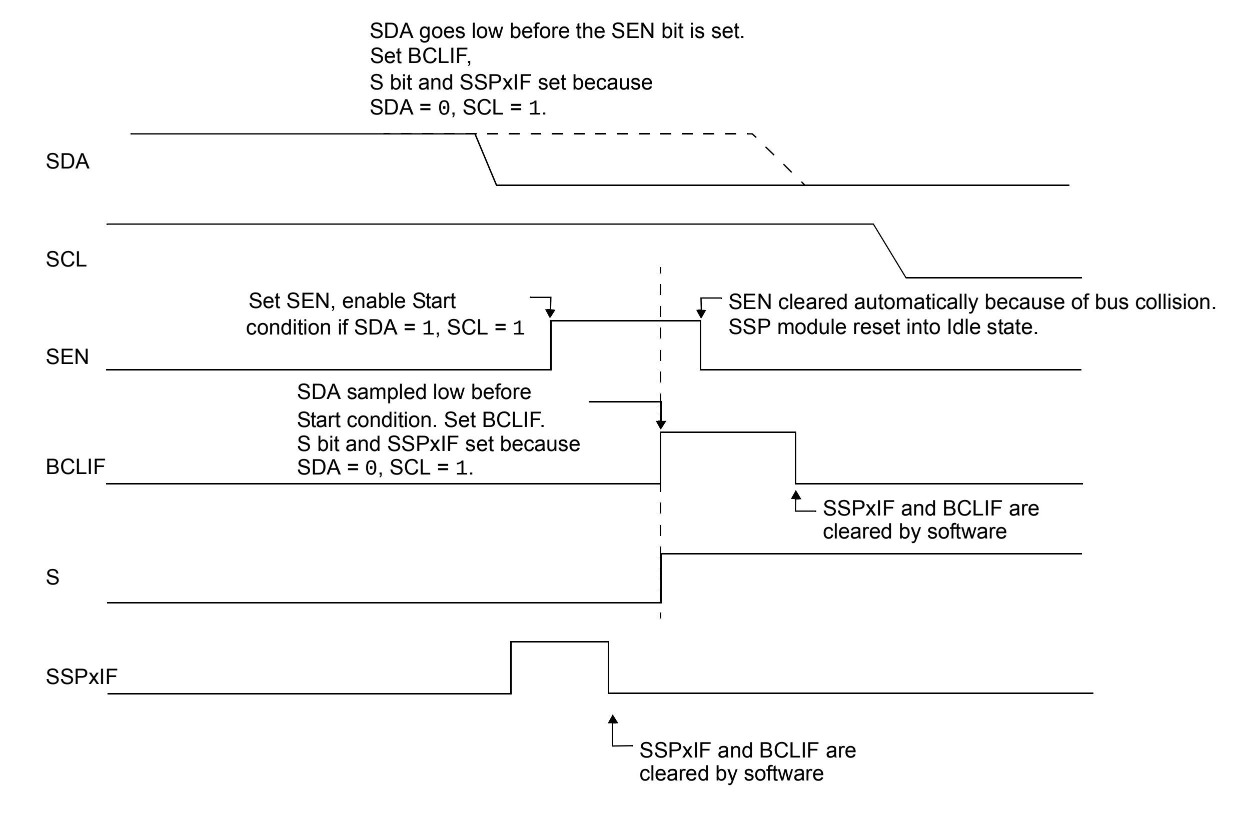
- the Start condition is aborted,
- the BCLIF flag is set and
- the MSSP module is reset to its Idle state (Figure 32-33).

The Start condition begins with the SDA and SCL pins deasserted. When the SDA pin is sampled high, the Baud Rate Generator is loaded and counts down. If the SCL pin is sampled low while SDA is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 32-35). If, however, a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to zero; if the SCL pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

Note: The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.

FIGURE 32-33: BUS COLLISION DURING START CONDITION (SDA ONLY)


SDA goes low before the SEN bit is set.
Set BCLIF,
S bit and SSPxIF set because
SDA = 0, SCL = 1.
SDA
SCL
Set SEN, enable Start
condition if SDA = 1, SCL = 1
SEN cleared automatically because of bus collision.
SSP module reset into Idle state.
SEN
SDA sampled low before
Start condition. Set BCLIF.
S bit and SSPxIF set because
SDA = 0, SCL = 1.
BCLIF
SSPxIF and BCLIF are
cleared by software
S
SSPxIF
SSPxIF and BCLIF are
cleared by software

REGISTER 32-3: SSP1CON2: SSP CONTROL REGISTER 2[1]

R/W-0/0	R-0/0	R/W-0/0	R/S/HS-0/0	R/S/HS-0/0	R/S/HS-0/0	R/S/HS-0/0	R/W/HS-0/0
GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HC = Cleared by hardware S = User set

bit 7 **GCEN:** General Call Enable bit (in I^2C Slave mode only)
1 = Enable interrupt when a general call address (0x00 or 00h) is received in the SSPSR
0 = General call address disabled

bit 6 **ACKSTAT:** Acknowledge Status bit (in I^2C mode only)
1 = Acknowledge was not received
0 = Acknowledge was received

bit 5 **ACKDT:** Acknowledge Data bit (in I^2C mode only)
In Receive mode:
Value transmitted when the user initiates an Acknowledge sequence at the end of a receive
1 = Not Acknowledge
0 = Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit (in I^2C Master mode only)
In Master Receive mode:
1 = Initiate Acknowledge sequence on SDA and SCL pins, and transmit ACKDT data bit. Automatically cleared by hardware.
0 = Acknowledge sequence idle

bit 3 **RCEN:** Receive Enable bit (in I^2C Master mode only)
1 = Enables Receive mode for I^2C
0 = Receive idle

bit 2 **PEN:** Stop Condition Enable bit (in I^2C Master mode only)
SCKMSSP Release Control:
1 = Initiate Stop condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Stop condition Idle

bit 1 **RSEN:** Repeated Start Condition Enable bit (in I^2C Master mode only)
1 = Initiate Repeated Start condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Repeated Start condition Idle

bit 0 **SEN:** Start Condition Enable/Stretch Enable bit
In Master mode:
1 = Initiate Start condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Start condition Idle
In Slave mode:
1 = Clock stretching is enabled for both slave transmit and slave receive (stretch enabled)
0 = Clock stretching is disabled

Note 1: For bits ACKEN, RCEN, PEN, RSEN, SEN: If the I^2C module is not in the Idle mode, this bit may not be set (no spooling) and the SSP1BUF may not be written (or writes to the SSP1BUF are disabled).

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

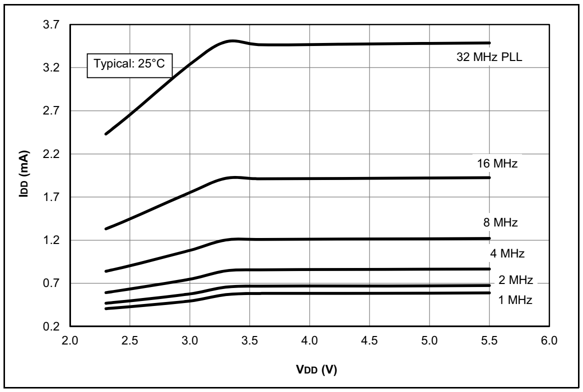


FIGURE 37-25: *I_{DD} Typical, HFINTOSC Mode, PIC16F1777/8/9 Only.*

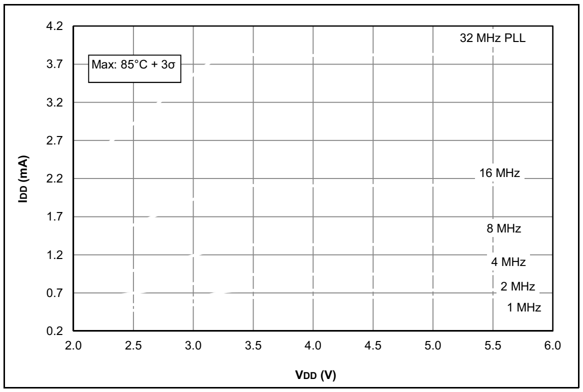


FIGURE 37-26: *I_{DD} Maximum, HFINTOSC Mode, PIC16F1777/8/9 Only.*

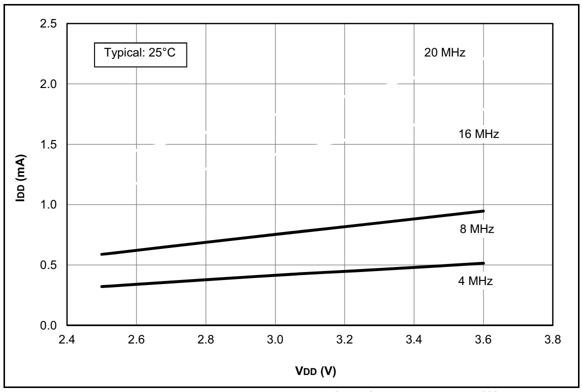


FIGURE 37-27: *I_{DD} Typical, HS Oscillator, 25°C, PIC16LF1777/8/9 Only.*

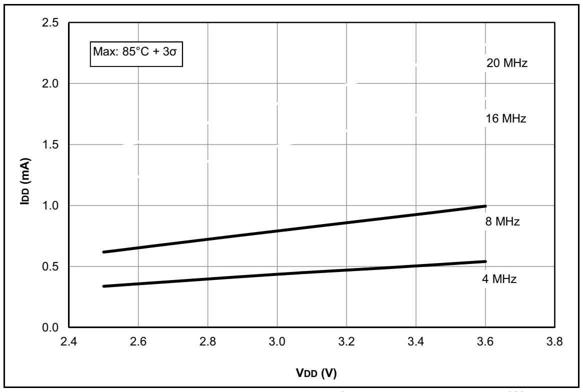


FIGURE 37-28: *I_{DD} Maximum, HS Oscillator, PIC16LF1777/8/9 Only.*

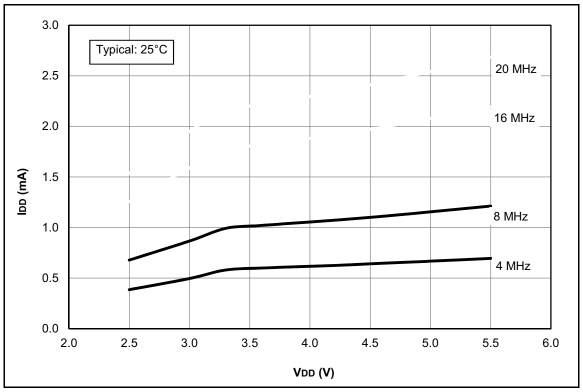


FIGURE 37-29: *I_{DD} Typical, HS Oscillator, 25°C, PIC16F1777/8/9 Only.*

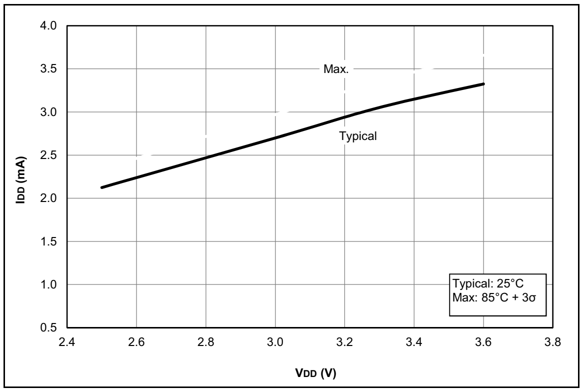


FIGURE 37-30: *I_{DD}, HS Oscillator (8 MHz + 4x PLL), PIC16LF1777/8/9 Only.*

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

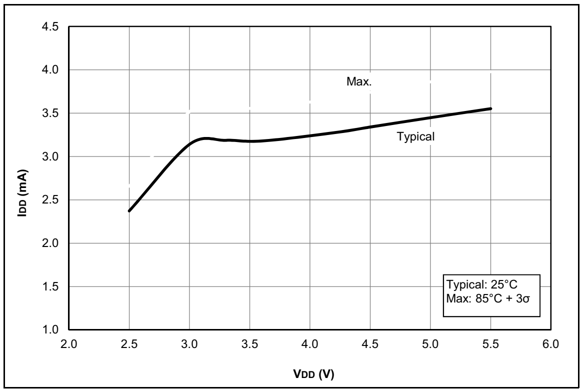


FIGURE 37-31: *IDD, HS Oscillator, 32 MHz (8 MHz + 4x PLL), PIC16F1777/8/9 Only.*

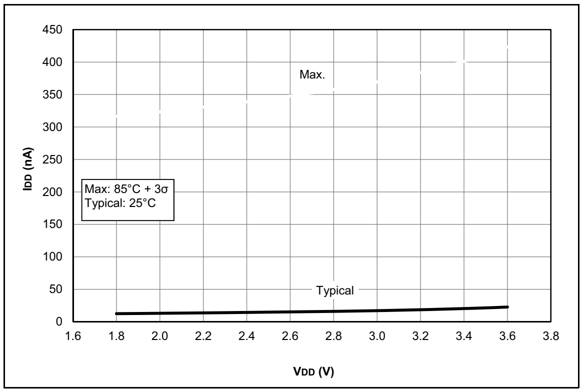


FIGURE 37-32: *IPD Base, LP Sleep Mode, PIC16LF1777/8/9 Only.*

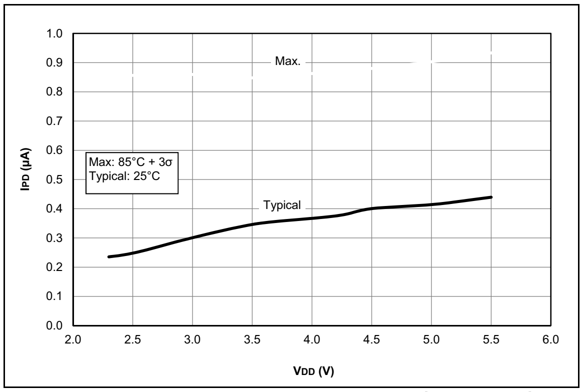


FIGURE 37-33: *IPD Base, LP Sleep Mode (VREGPM = 1), PIC16F1777/8/9 Only.*

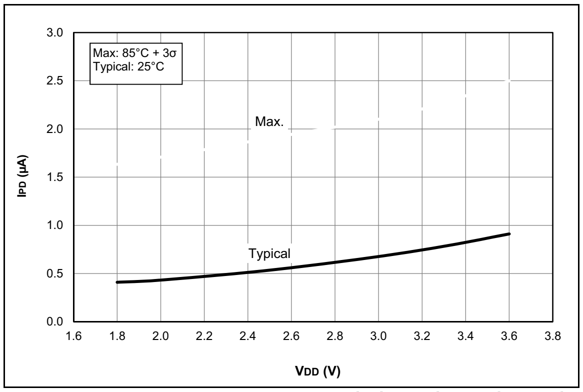


FIGURE 37-34: *IPD, Watchdog Timer (WDT), PIC16LF1777/8/9 Only.*

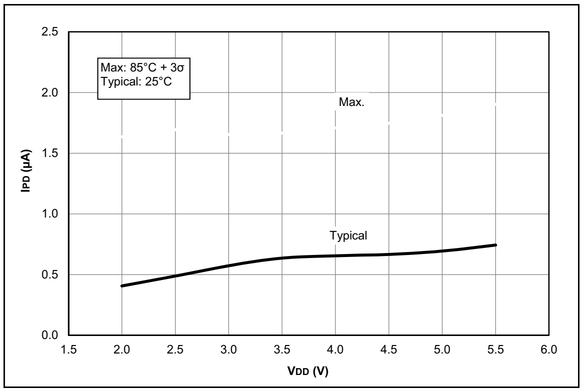


FIGURE 37-35: *IPD, Watchdog Timer (WDT), PIC16F1777/8/9 Only.*

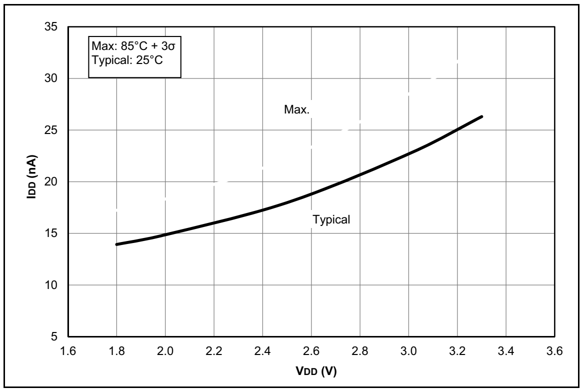


FIGURE 37-36: *IPD, Fixed Voltage Reference (FVR), ADC, PIC16LF1777/8/9 Only.*

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

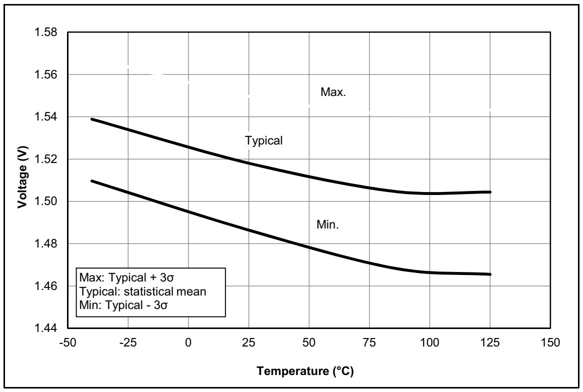


FIGURE 37-73: *POR Rearm Voltage, NP Mode (VREGPM1 = 0), PIC16F1773/6 Only.*

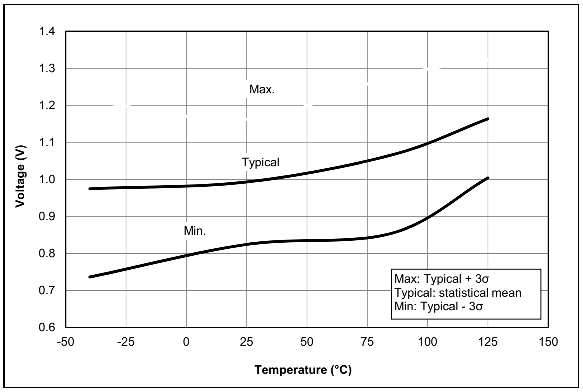


FIGURE 37-74: *POR Rearm Voltage, NP Mode, PIC16LF1777/8/9 Only.*

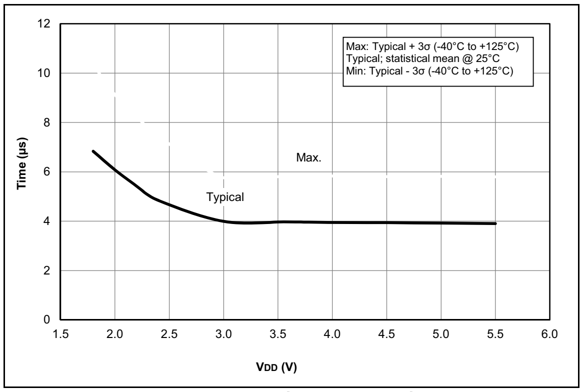


FIGURE 37-75: *Wake From Sleep, VREGPM = 0.*

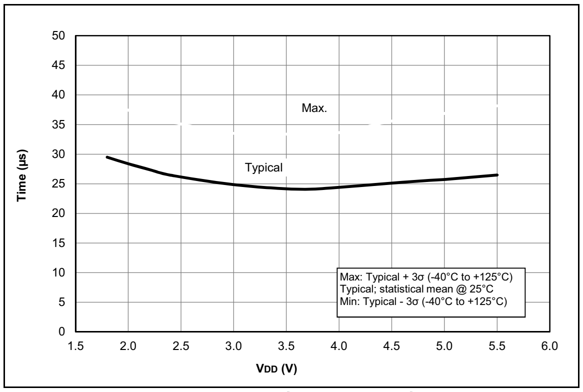


FIGURE 37-76: *Wake From Sleep, VREGPM = 1.*

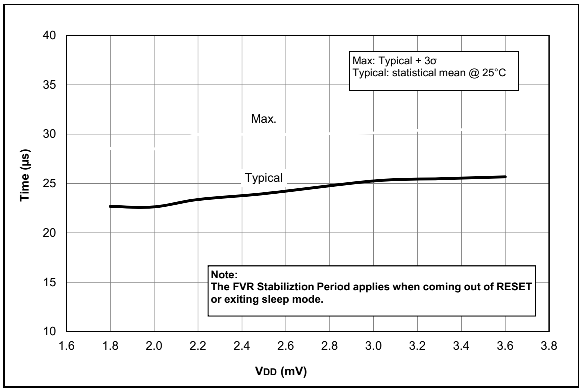


FIGURE 37-77: FVR Stabilization Period, *PIC16LF1777/8/9 Only.*

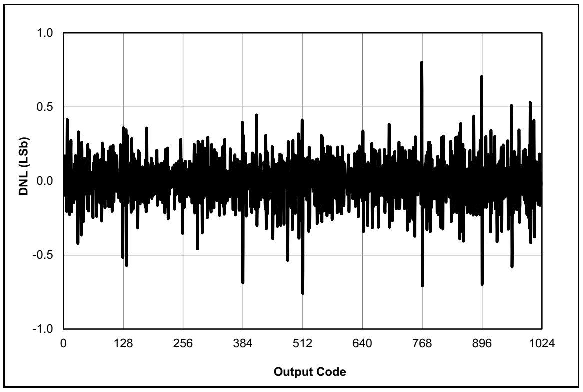


FIGURE 37-78: *ADC 10-bit Mode, Single-Ended DNL, V_{DD} = 3.0V, T_{AD} = 1 µS, 25°C.*

38.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

38.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

38.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

38.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility