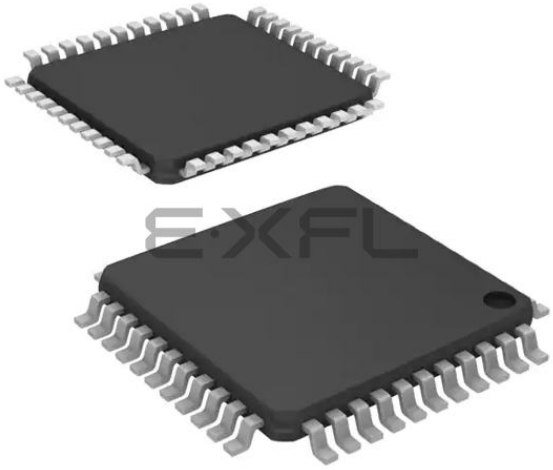

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 28x10b; D/A 4x5b, 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1779-e-pt

TABLE 1-3: PIC16(L)F1777/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA5/AN4/OPA1IN0-/ DAC2OUT1/PRG1F/ MD1MOD/$\overline{SS}$	RA5	TTL/ST	CMOS	General purpose I/O.
	AN4	AN	—	ADC Channel 4 input.
	OPA1IN0-	AN	—	Operational amplifier 1 inverting input.
	DAC2OUT1	—	AN	DAC2 voltage output.
	PRG1F(1)	TTL/ST	—	Ramp generator set_falling input.
	MD1MOD(1)	TTL/ST	—	Data signal modulator modulation input.
	$\overline{SS}$	ST	—	Slave Select input.
RA6/CLKOUT/C6IN1+/OSC2	RA6	TTL/ST	CMOS	General purpose I/O.
	CLKOUT	—	CMOS	FOSC/4 output.
	C6IN1+	AN	—	Comparator 6 positive input.
	OSC2	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
RA7/CLKIN/OSC1	RA7	TTL/ST	CMOS	General purpose I/O.
	CLKIN	TTL/ST	—	CLC input.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
RB0/AN12/ZCD/HIB0/C2IN1+/ CCP8/COG1IN/MD4CL/ INT	RB0	TTL/ST	CMOS	General purpose I/O.
	AN12	AN	—	ADC Channel 12 input.
	ZCD	AN	—	Zero-cross detection input.
	HIB0	HP	HP	High-Power output.
	C2IN1+	AN	—	Comparator 2 positive input.
	CCP8(1)	TTL/ST	—	CCP8 capture input.
	COG1IN(1)	TTL/ST	—	Complementary output generator 1 input.
	MD4CL(1)	TTL/ST	—	Data signal modulator 4 low carrier input.
	INT	TTL/ST	—	External interrupt.
RB1/AN10/PRG1IN1/PRG2IN0/ PRG4R/HIB1/C1IN3-/C2IN3-/ C3IN3-/C4IN3-/OPA2OUT/ OPA1IN1+/OPA1IN1-/COG2IN/ MD4CH	RB1	TTL/ST	CMOS	General purpose I/O.
	AN10	AN	—	ADC Channel 10 input.
	PRG1IN1	AN	—	Ramp generator 1 reference voltage input.
	PRG2IN0	AN	—	Ramp generator 2 reference voltage input.
	PRG4R(1)	TTL/ST	—	Ramp generator set_rising input.
	HIB1	HP	HP	High-Power output.
	C1IN3-	AN	—	Comparator 1 negative input.
	C2IN3-	AN	—	Comparator 2 negative input.
	C3IN3-	AN	—	Comparator 3 negative input.
	C4IN3-	AN	—	Comparator 4 negative input.
	OPA2OUT	—	AN	Operational amplifier 2 output.
	OPA1IN1+	AN	—	Operational amplifier 1 non-inverting input.
	OPA1IN1-	AN	—	Operational amplifier 1 inverting input.
	COG2IN(1)	TTL/ST	—	Complementary output generator 2 input.
	MD4CH(1)	TTL/ST	—	Data signal modulator 4 high carrier input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HP = High Power XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.
2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-3: PIC16(L)F1777/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB7/C5IN1+/DAC1OUT2/ DAC2OUT2/DAC3OUT2/ DAC4OUT2/DAC5OUT2/ DAC6OUT2/DAC7OUT2/ DAC8OUT2/T6IN/CLCIN3/ ICSPDAT	RB7	TTL/ST	CMOS	General purpose I/O.
	C5IN1+	AN	—	Comparator 5 positive input.
	DAC1OUT2	—	AN	DAC1 voltage output.
	DAC2OUT2	—	AN	DAC2 voltage output.
	DAC3OUT2	—	AN	DAC3 voltage output.
	DAC4OUT2	—	AN	DAC4 voltage output.
	DAC5OUT2	—	AN	DAC5 voltage output.
	DAC6OUT2	—	AN	DAC6 voltage output.
	DAC7OUT2	—	AN	DAC7 voltage output.
	DAC8OUT2	—	AN	DAC8 voltage output.
	T6IN(1)	TTL/ST	—	Timer6 gate input.
	CLCIN3(1)	TTL/ST	—	CLC input 3.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RC0/DAC5OUT1/T1CKI/T3CKI/ T3G/SOSCO	RC0	TTL/ST	CMOS	General purpose I/O.
	DAC5OUT1	—	AN	DAC5 voltage output.
	T1CKI(1)	AN	—	Comparator 4 negative input.
	T3CKI(1)	TTL/ST	—	Timer3 clock input.
	T3G(1)	TTL/ST	—	Timer3 gate input.
	SOSCO	—	XTAL	Secondary oscillator output.
RC1/DAC7OUT1/PRG2R/CCP2/ SOSCI	RC1	TTL/ST	CMOS	General purpose I/O.
	DAC7OUT1	—	AN	DAC7 voltage output.
	PRG2R(1)	TTL/ST	—	Ramp generator set_rising input.
	CCP2(1)	TTL/ST	—	CCP2 capture input.
	SOSCI	XTAL	—	Secondary oscillator input.
RC2/AN14/C5IN2-/C6IN2-/ PRG2F/CCP1	RC2	TTL/ST	CMOS	General purpose I/O.
	AN14	AN	—	ADC Channel 14 input.
	C5IN2-	AN	—	Comparator 5 negative input.
	C6IN2-	AN	—	Comparator 6 negative input.
RC3/AN15/C1IN4-/C2IN4-/ C3IN4-/C4IN4-/C5IN4-/C6IN4-/ C7IN4-/C8IN4-/T2IN/MD2CL/ SCL	RC3	TTL/ST	CMOS	General purpose I/O.
	AN15	AN	—	ADC Channel 15 input.
	C1IN4-	AN	—	Comparator 1 negative input.
	C2IN4-	AN	—	Comparator 2 negative input.
	C3IN4-	AN	—	Comparator 3 negative input.
	C4IN4-	AN	—	Comparator 4 negative input.
	C5IN4-	AN	—	Comparator 5 negative input.
	C6IN4-	AN	—	Comparator 6 negative input.
	C7IN4-	AN	—	Comparator 7 negative input.
	C8IN4-	AN	—	Comparator 8 negative input.
	T2IN(1)	TTL/ST	—	Timer2 gate input.
	MD2CL(1)	TTL/ST	—	Data signal modulator 2 low carrier input.
	SCL	I^2C	OD	I^2C clock.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HP = High Power XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 27											
D8Ch	—	Unimplemented								—	—
D8Dh	—	Unimplemented								—	—
D8Eh	PWMEN	—	—	—	—	MPWM12EN(3)	MPWM11EN	MPWM6EN	MPWM5EN	---- 0000	---- 0000
D8Fh	PWMLD	—	—	—	—	MPWM12LD(3)	MPWM11LD	MPWM6LD	MPWM5LD	---- 0000	---- 0000
D90h	PWMOUT	—	—	—	—	MPWM12OUT(3)	MPWM11OUT	MPWM6OUT	MPWM5OUT	---- 0000	---- 0000
D91h	PWM5PHL	PH<7:0>								xxxx xxxx	uuuu uuuu
D92h	PWM5PHH	PH<15:8>								xxxx xxxx	uuuu uuuu
D93h	PWM5DCL	DC<7:0>								xxxx xxxx	uuuu uuuu
D94h	PWM5DCH	DC<15:8>								xxxx xxxx	uuuu uuuu
D95h	PWM5PRL	PR<7:0>								xxxx xxxx	uuuu uuuu
D96h	PWM5PRH	PR<15:8>								xxxx xxxx	uuuu uuuu
D97h	PWM5OFL	OF<7:0>								xxxx xxxx	uuuu uuuu
D98h	PWM5OFH	OF<15:8>								xxxx xxxx	uuuu uuuu
D99h	PWM5TMRL	TMR<7:0>								0000 0000	0000 0000
D9Ah	PWM5TMRH	TMR<15:8>								0000 0000	0000 0000
D9Bh	PWM5CON	EN	—	OUT	POL	MODE<1:0>		—	—	0-00 00--	0-00 00--
D9Ch	PWM5INTE	—	—	—	—	OFIE	PHIE	DCIE	PRIE	---- 0000	---- 0000
D9Dh	PWM5INTF	—	—	—	—	OFIF	PHIF	DCIF	PRIF	---- 0000	---- 0000
D9Eh	PWM5CLKCON	—	PS<2:0>			—	—	CS<1:0>		-000 --00	-000 --00
D9Fh	PWM5LDCON	LDA	LDT	—	—	—	—	LDS<1:0>		00-- --00	00-- --00
DA0h	PWM5OFCON	—	OFM<1:0>		OFO	—	—	OFS<1:0>		-000 --00	-000 --00
DA1h	PWM6PHL	PH<7:0>								xxxx xxxx	uuuu uuuu
DA2h	PWM6PHH	PH<15:8>								xxxx xxxx	uuuu uuuu
DA3h	PWM6DCL	DC<7:0>								xxxx xxxx	uuuu uuuu
DA4h	PWM6DCH	DC<15:8>								xxxx xxxx	uuuu uuuu
DA5h	PWM6PRL	PR<7:0>								xxxx xxxx	uuuu uuuu
DA6h	PWM6PRH	PR<15:8>								xxxx xxxx	uuuu uuuu
DA7h	PWM6OFL	OF<7:0>								xxxx xxxx	uuuu uuuu
DA8h	PWM6OFH	OF<15:8>								xxxx xxxx	uuuu uuuu
DA9h	PWM6TMRL	TMR<7:0>								0000 0000	0000 0000
DAAh	PWM6TMRH	TMR<15:8>								0000 0000	0000 0000

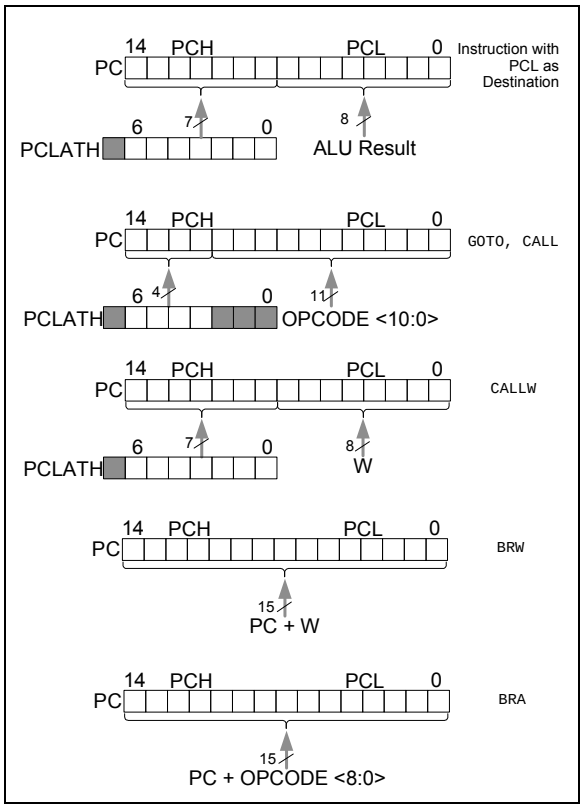
Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

3.5 PCL and PCLATH

The Program Counter (PC) is 15 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<14:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 3-4 shows the five situations for the loading of the PC.

FIGURE 3-4: LOADING OF PC IN DIFFERENT SITUATIONS



3.5.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<14:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper seven bits to the PCLATH register. When the lower eight bits are written to the PCL register, all 15 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

3.5.2 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to Application Note AN556, *"Implementing a Table Read"* (DS00556).

3.5.3 COMPUTED FUNCTION CALLS

A computed function CALL allows programs to maintain tables of functions and provide another way to execute state machines or look-up tables. When performing a table read using a computed function CALL, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block).

If using the CALL instruction, the PCH<2:0> and PCL registers are loaded with the operand of the CALL instruction. PCH<6:3> is loaded with PCLATH<6:3>.

The CALLW instruction enables computed calls by combining PCLATH and W to form the destination address. A computed CALLW is accomplished by loading the W register with the desired address and executing CALLW. The PCL register is loaded with the value of W and PCH is loaded with PCLATH.

3.5.4 BRANCHING

The branching instructions add an offset to the PC. This allows relocatable code and code that crosses page boundaries. There are two forms of branching, BRW and BRA. The PC will have incremented to fetch the next instruction in both cases. When using either branching instruction, a PCL memory boundary may be crossed.

If using BRW, load the W register with the desired unsigned address and execute BRW. The entire PC will be loaded with the address PC + 1 + W.

If using BRA, the entire PC will be loaded with PC + 1 +, the signed value of the operand of the BRA instruction.

TABLE 7-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	132
OPTION_REG	$\overline{\text{WPUEN}}$	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			274
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	133
PIE2	OSFIE	C2IE	C1IE	COG1IE	BCL1IE	C4IE	C3IE	CCP2IE	134
PIE3	—	—	COG2IE	ZCDIE	CLC4IE	CLC3IE	CLC2IE	CLC1IE	135
PIE4	—	TMR8IE	TMR5GIE	TMR5IE	TMR3GIE	TMR3IE	TMR6IE	TRM4IE	136
PIE5	CCP8IE(1)	CCP7IE	COG4IE(1)	COG3IE	C8IE(1)	C7IE(1)	C6IE	C5IE	137
PIE6	—	—	—	—	PWM12IE(1)	PWM11IE	PWM6IE	PWM5IE	138
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	139
PIR2	OSFIF	C2IF	C1IF	COG1IF	BCL1IF	C4IF	C3IF	CCP2IF	140
PIR3	—	—	COG2IF	ZCDIF	CLC4IF	CLC3IF	CLC2IF	CLC1IF	141
PIR4	—	TMR8IF	TMR5GIF	TMR5IF	TMR3GIF	TMR3IF	TMR6IF	TRM4IF	142
PIR5	CCP8IF(1)	CCP7IF	COG4IF(1)	COG3IF	C8IF(1)	C7IF(1)	C6IF	C5IF	143
PIR6	—	—	—	—	PWM12IF(1)	PWM11IF	PWM6IF	PWM5IF	144

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by interrupts.

Note 1: PIC16(L)F1777/9 only.

TABLE 9-2: WDT CLEARING CONDITIONS

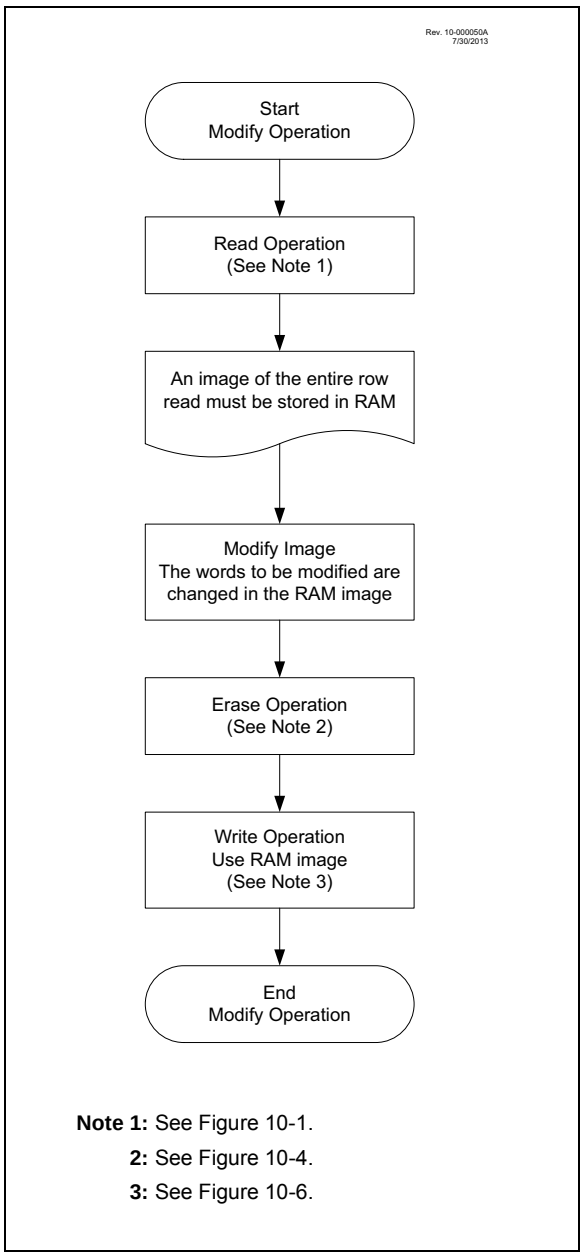
Conditions	WDT
WDTE<1:0> = 00	Cleared
WDTE<1:0> = 01 and SWDTEN = 0	
WDTE<1:0> = 10 and enter Sleep	
CLRWDT Command	
Oscillator Fail Detected	
Exit Sleep + System Clock = T1OSC, EXTRC, INTOSC, EXTCLK	
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST
Change INTOSC divider (IRCF bits)	Unaffected

10.3 Modifying Flash Program Memory

When modifying existing data in a program memory row, and data within that row must be preserved, it must first be read and saved in a RAM image. Program memory is modified using the following steps:

1. Load the starting address of the row to be modified.
2. Read the existing data from the row into a RAM image.
3. Modify the RAM image to contain the new data to be written into program memory.
4. Load the starting address of the row to be rewritten.
5. Erase the program memory row.
6. Load the write latches with data from the RAM image.
7. Initiate a programming operation.

FIGURE 10-7: FLASH PROGRAM MEMORY MODIFY FLOWCHART



Note 1: See Figure 10-1.
2: See Figure 10-4.
3: See Figure 10-6.

11.7 PORTD Registers (PIC16(L)F1777/9 only)

11.7.1 DATA REGISTER

PORTD is an 8-bit wide bidirectional port in the PIC16(L)F1777/8/9 devices. The corresponding data direction register is TRISD (Register 11-27). Setting a TRISD bit (= 1) will make the corresponding PORTD pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISD bit (= 0) will make the corresponding PORTD pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 11-1 shows how to initialize an I/O port.

Reading the PORTD register (Register 11-26) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATD).

11.7.2 DIRECTION CONTROL

The TRISD register (Register 11-27) controls the PORTD pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISD register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

11.7.3 INPUT THRESHOLD CONTROL

The INLVLD register (Register 11-33) controls the input voltage threshold for each of the available PORTD input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTD register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Table 36-4: I/O Ports for more information on threshold levels.

Note:	Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

11.7.4 OPEN-DRAIN CONTROL

The ODCOND register (Register 11-31) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCOND bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCOND bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

11.7.5 SLEW RATE CONTROL

The SLRCOND register (Register 11-32) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCOND bit is set, the corresponding port pin drive is slew rate limited. When an SLRCOND bit is cleared, The corresponding port pin drive slews at the maximum rate possible.

11.7.6 ANALOG CONTROL

The ANSELD register (Register 11-29) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELD bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELD bits has no effect on digital output functions. A pin with TRIS clear and ANSELD set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELD bits default to the Analog mode after reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

11.7.7 PORTD FUNCTIONS AND OUTPUT PRIORITIES

Each pin defaults to the PORT latch data after reset. Other functions are selected with the peripheral pin select logic. See **Section 12.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELD register. Digital output functions may continue to control the pin when it is in Analog mode.

REGISTER 11-30: WPUD: WEAK PULL-UP PORTD REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
WPUD7	WPUD6	WPUD5	WPUD4	WPUD3	WPUD2	WPUD1	WPUD0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **WPUD<7:0>**: Weak Pull-up Register bits(1, 2)
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: Global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is configured as an output.

REGISTER 11-31: ODCOND: PORTD OPEN-DRAIN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ODD7	ODD6	ODD5	ODD4	ODD3	ODD2	ODD1	ODD0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ODD<7:0>:** PORTD Open-Drain Enable bits
For RD<7:0> pins
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

12.8 Register Definitions: PPS Input Selection

REGISTER 12-1: xxxPPS: PERIPHERAL xxx INPUT SELECTION

U-0	U-0	R/W-q/u	R/W-q/u	R/W-q/u	R/W-q/u	R/W-q/u	R/W-q/u
—	—	xxxPPS<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = value depends on peripheral

bit 7-6 **Unimplemented:** Read as '0'

bit 5-3 **xxxPPS<5:3>:** Peripheral xxx Input PORT Selection bits
100 = Peripheral input is PORTE
011 = Peripheral input is PORTD(1)
010 = Peripheral input is PORTC
001 = Peripheral input is PORTB
000 = Peripheral input is PORTA

bit 2-0 **xxxPPS<2:0>:** Peripheral xxx Input Bit Selection bits(1)
111 = Peripheral input is from PORTx Bit 7 (Rx7)
110 = Peripheral input is from PORTx Bit 6 (Rx6)
101 = Peripheral input is from PORTx Bit 5 (Rx5)
100 = Peripheral input is from PORTx Bit 4 (Rx4)
011 = Peripheral input is from PORTx Bit 3 (Rx3)
010 = Peripheral input is from PORTx Bit 2 (Rx2)
001 = Peripheral input is from PORTx Bit 1 (Rx1)
000 = Peripheral input is from PORTx Bit 0 (Rx0)

Note 1: See Table 12-1 for xxxPPS register list and Reset values.
2: PIC16(L)F1777/9 only.

REGISTER 12-2: RxyPPS: PIN Rxy OUTPUT SOURCE SELECTION REGISTER

U-0	U-0	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u
—	—	RxyPPS<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RxyPPS<5:0>:** Pin Rxy Output Source Selection bits
Selection code determines the output signal on the port pin.
See Table 12-2 for the selection codes

EQUATION 20-2: R-C CALCULATIONS

V_{peak} = external voltage source peak voltage
f = external voltage source frequency
C = series capacitor
R = series resistor
V_C = Peak capacitor voltage
ϕ = Capacitor induced zero crossing phase advance in radians
T_ϕ = Time ZC event occurs before actual zero crossing

$$Z = \frac{V_{PEAK}}{3x10^{-4}}$$

$$X_C = \frac{1}{(2\pi fC)}$$

$$R = \sqrt{Z^2 - X_C}$$

$$V_C = X_C(3x10^{-4})$$

$$\phi = Tan^{-1}\left(\frac{X_C}{R}\right)$$

$$T_\phi = \frac{\phi}{(2\pi f)}$$

V_{rms} = 120

EQUATION 20-3: R-C CALCULATIONS EXAMPLE

$$V_{peak} = V_{rms} \cdot \sqrt{2} = 169.7$$

f = 60 Hz
C = 0.1 μf

$$Z = \frac{V_{peak}}{3 \times 10^{-4}} = \frac{169.7}{3 \times 10^{-4}} = 565.7\ kOhms$$

$$X_C = \frac{1}{(2\pi fC)} = \frac{1}{(2\pi \cdot 60 \cdot 1 \cdot 10^{-7})} = 26.53\ \text{kOhms}$$

R = 560 kOhms

$$Z_R = \sqrt{(R^2 + X_C^2)} = 560.6\ kOhm\ \text{(using actual resistor)}$$

$$I_{peak} = \frac{V_{peak}}{Z_R} = 302.7 \cdot 10^{-6}$$

$$V_C = X_C \cdot I_{peak} = 8.0\ \text{V}$$

$$\phi = Tan^{-1}\left(\frac{X_C}{R}\right) = 0.047\ radians$$

$$T_\phi = \frac{\phi}{(2\pi f)} = 125.6\ \mu s$$

22.0 TIMER1/3/5 MODULE WITH GATE CONTROL

The Timer1 module is a 16-bit timer/counter with the following features:

- 16-bit timer/counter register pair (TMR1H:TMR1L)
- Programmable internal or external clock source
- 2-bit prescaler
- Dedicated 32 kHz oscillator circuit
- Optionally synchronized comparator out
- Multiple Timer1 gate (count enable) sources
- Interrupt-on-overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- Time base for the Capture/Compare function
- Auto-conversion Trigger (with CCP)
- Selectable Gate Source Polarity
- Gate Toggle mode
- Gate Single-pulse mode
- Gate Value Status
- Gate Event Interrupt

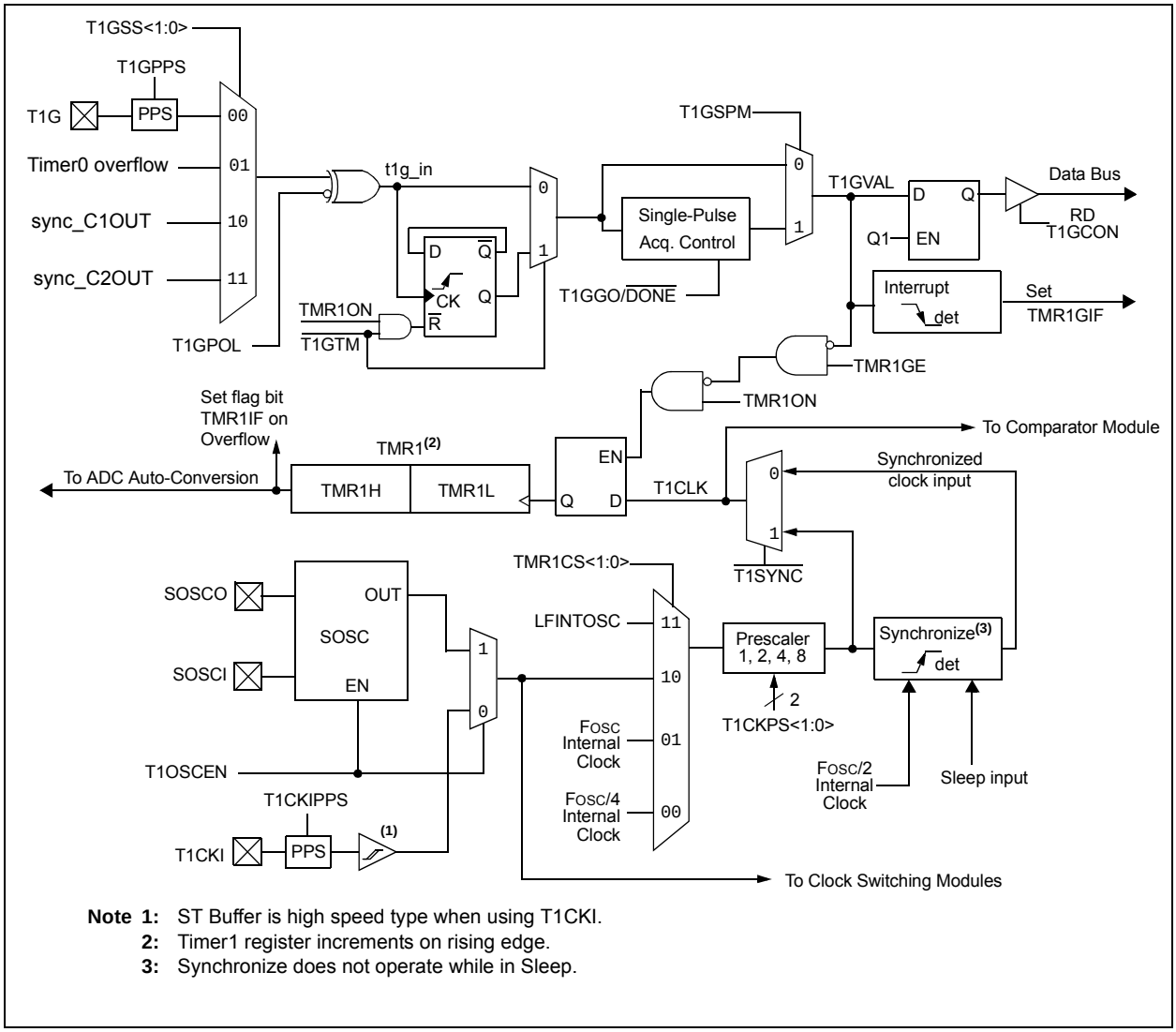
Figure 22-1 is a block diagram of the Timer1 module.

This device has three instances of Timer1 type modules. They include:

- Timer1
- Timer3
- Timer5

Note:	All references to Timer1 and Timer1 Gate apply to Timer3 and Timer5.

FIGURE 22-1: TIMER1 BLOCK DIAGRAM



Note 1: ST Buffer is high speed type when using T1CKI.
2: Timer1 register increments on rising edge.
3: Synchronize does not operate while in Sleep.

25.0 10-BIT PULSE-WIDTH MODULATION (PWM) MODULE

The 10-bit PWM module generates a Pulse-Width Modulated signal determined by the duty cycle, period, and resolution that are configured by the following registers:

- T2PR
- T2CON
- PWMxDCH
- PWMxDCL
- PWMxCON

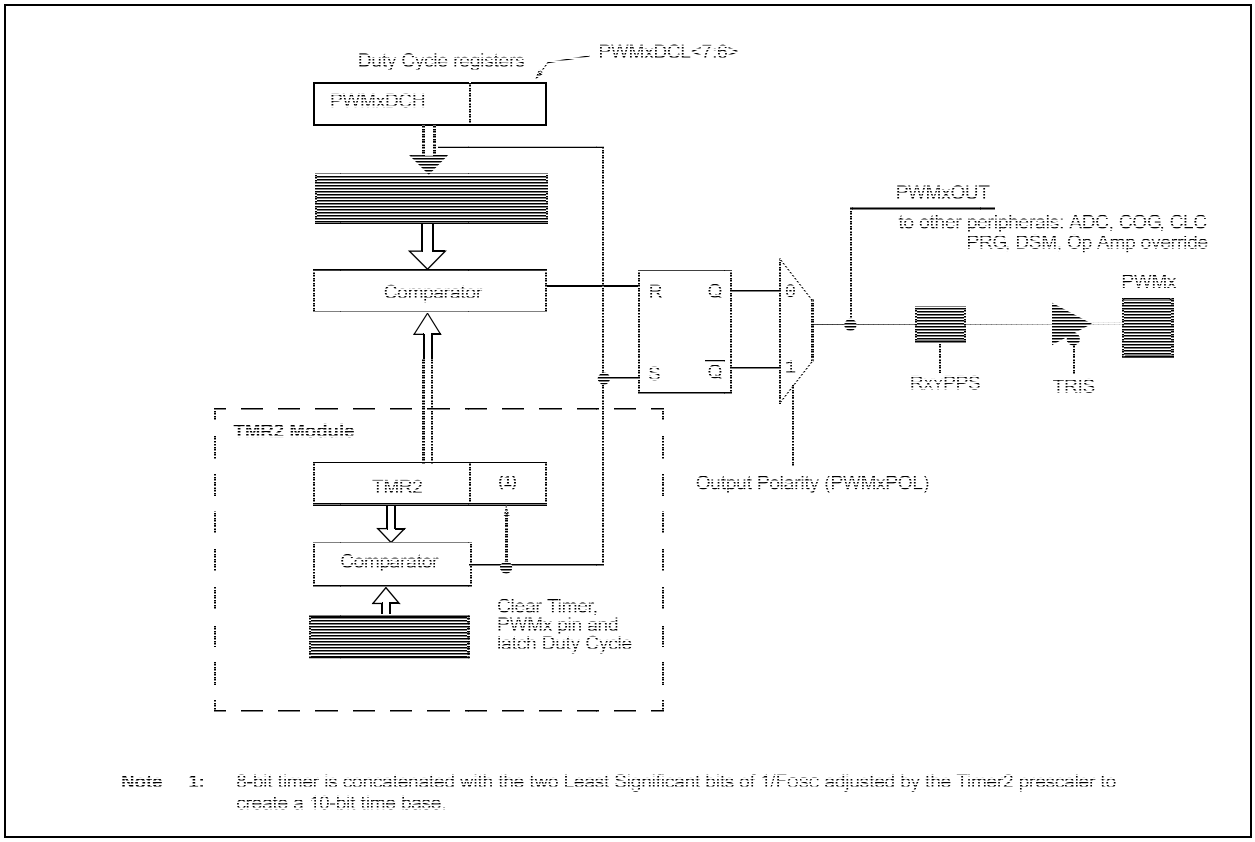
Figure 25-1 shows a simplified block diagram of PWM operation.

Figure 25-2 shows a typical waveform of the PWM signal.

TABLE 25-1: AVAILABLE 10-BIT PWM MODULES

Device	PWM3	PWM4	PWM9	PWM10
PIC16(L)F1778	•	•	•	
PIC16(L)F1777/9	•	•	•	•

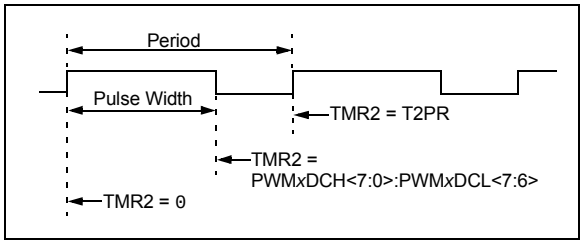
FIGURE 25-1: SIMPLIFIED PWM BLOCK DIAGRAM



Note 1: 8-bit timer is concatenated with the two Least Significant bits of 1/Fosc adjusted by the Timer2 prescaler to create a 10-bit time base.

For a step-by-step procedure on how to set up this module for PWM operation, refer to **Section 25.1.9 "Setup for PWM Operation using PWMx Output Pins"**.

FIGURE 25-2: PWM OUTPUT



27.5.2 RISING EVENT

The rising event starts the PWM output active duty cycle period. The rising event is the low-to-high transition of the rising_event output. When the rising event phase delay and dead-band time values are zero, the primary output starts immediately. Otherwise, the primary output is delayed. The rising event source causes all the following actions:

- Start rising event phase delay counter (if enabled).
- Clear complementary output after phase delay.
- Start falling event input blanking (if enabled).
- Start dead-band delay (if enabled).
- Set primary output after dead-band delay expires.

27.5.3 FALLING EVENT

The falling event terminates the PWM output active duty cycle period. The falling event is the high-to-low transition of the falling_event output. When the falling event phase delay and dead-band time values are zero, the complementary output starts immediately. Otherwise, the complementary output is delayed. The falling event source causes all the following actions:

- Start falling event phase delay counter (if enabled).
- Clear primary output.
- Start rising event input blanking (if enabled).
- Start falling event dead-band delay (if enabled).
- Set complementary output after dead-band delay expires.

27.6 Output Control

Upon disabling, or immediately after enabling the COG module, the primary COG outputs are inactive and complementary COG outputs are active.

27.6.1 OUTPUT ENABLES

There are no output enable controls in the COG module. Instead, each device pin has an individual output selection control called the PPS register. All four COG outputs are available for selection in the PPS register of every pin.

When a COG output is enabled by PPS selection, the output on the pin has several possibilities which depend on the mode, steering control, EN bit, and shutdown state as shown in Table 27-2 and Table 27-3.

.

TABLE 27-2: PIN OUTPUT STATES MD<2:0> = 00x

EN	STR bit	Shutdown	Output
x	0	Inactive	Static steering data
x	1	Active	Shutdown override
0	1	Inactive	Inactive state
1	1	Inactive	Active PWM signal

TABLE 27-3: PIN OUTPUT STATES MD<2:0> > 001

EN	STR bit	Shutdown	Output
x	x	Inactive	Inactive state
x	x	Active	Shutdown override
1	x	Inactive	Active PWM signal

27.6.2 POLARITY CONTROL

The polarity of each COG output can be selected independently. When the output polarity bit is set, the corresponding output is active-low. Clearing the output polarity bit configures the corresponding output as active-high. However, polarity affects the outputs in only one of the four shutdown override modes. See **Section 27.10 "Auto-Shutdown Control"** for more details.

Output polarity is selected with the POLA through POLD bits of the COGxCON1 register (Register 27-2).

27.7 Dead-Band Control

The dead-band control provides for non-overlapping PWM output signals to prevent shoot-through current in the external power switches. Dead-band time affects the output only in the Half-Bridge mode and when changing direction in the Full-Bridge mode.

The COG contains two dead-band timers. One dead-band timer is used for rising event dead-band control. The other is used for falling event dead-band control. Timer modes are selectable as either:

- Asynchronous delay chain
- Synchronous counter

The Dead-Band Timer mode is selected for the rising event and falling event dead-band times with the respective RDBS and FDBS bits of the COGxCON1 register (Register 27-2).

In Half-Bridge mode, the rising event dead-band time delays all selected primary outputs from going active for the selected dead-band time after the rising event. COGxA and COGxC are the primary outputs in Half-Bridge mode.

In Half-Bridge mode, the falling event dead-band time delays all selected complementary outputs from going active for the selected dead-band time after the falling event. COGxB and COGxD are the complementary outputs in Half-Bridge mode.

In Full-Bridge mode, the dead-band delay occurs only during direction changes. The modulated output is delayed for the falling event dead-band time after a direction change from forward to reverse. The modulated output is delayed for the rising event dead-band time after a direction change from reverse to forward.

27.10.3 AUTO-SHUTDOWN RESTART

After an auto-shutdown event has occurred, there are two ways to resume operation:

- Software controlled
- Auto-restart

The restart method is selected with the ARSEN bit of the COGxASD0 register. Waveforms of a software controlled automatic restart are shown in Figure 27-15.

27.10.3.1 Software Controlled Restart

When the ARSEN bit of the COGxASD0 register is cleared, software must clear the ASE bit to restart COG operation after an auto-shutdown event.

The COG will resume operation on the first rising event after the ASE bit is cleared. Clearing the shutdown state requires all selected shutdown inputs to be false, otherwise, the ASE bit will remain set.

27.10.3.2 Auto-Restart

When the ARSEN bit of the COGxASD0 register is set, the COG will restart from the auto-shutdown state automatically.

The ASE bit will clear automatically and the COG will resume operation on the first rising event after all selected shutdown inputs go false.

32.2.6 SPI OPERATION IN SLEEP MODE

In SPI Master mode, module clocks may be operating at a different speed than when in Full-Power mode; in the case of the Sleep mode, all clocks are halted.

Special care must be taken by the user when the MSSP clock is much faster than the system clock.

In Slave mode, when MSSP interrupts are enabled, after the master completes sending data, an MSSP interrupt will wake the controller from Sleep.

If an exit from Sleep mode is not desired, MSSP interrupts should be disabled.

In SPI Master mode, when the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the device wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all eight bits have been received, the MSSP interrupt flag bit will be set and if enabled, will wake the device.

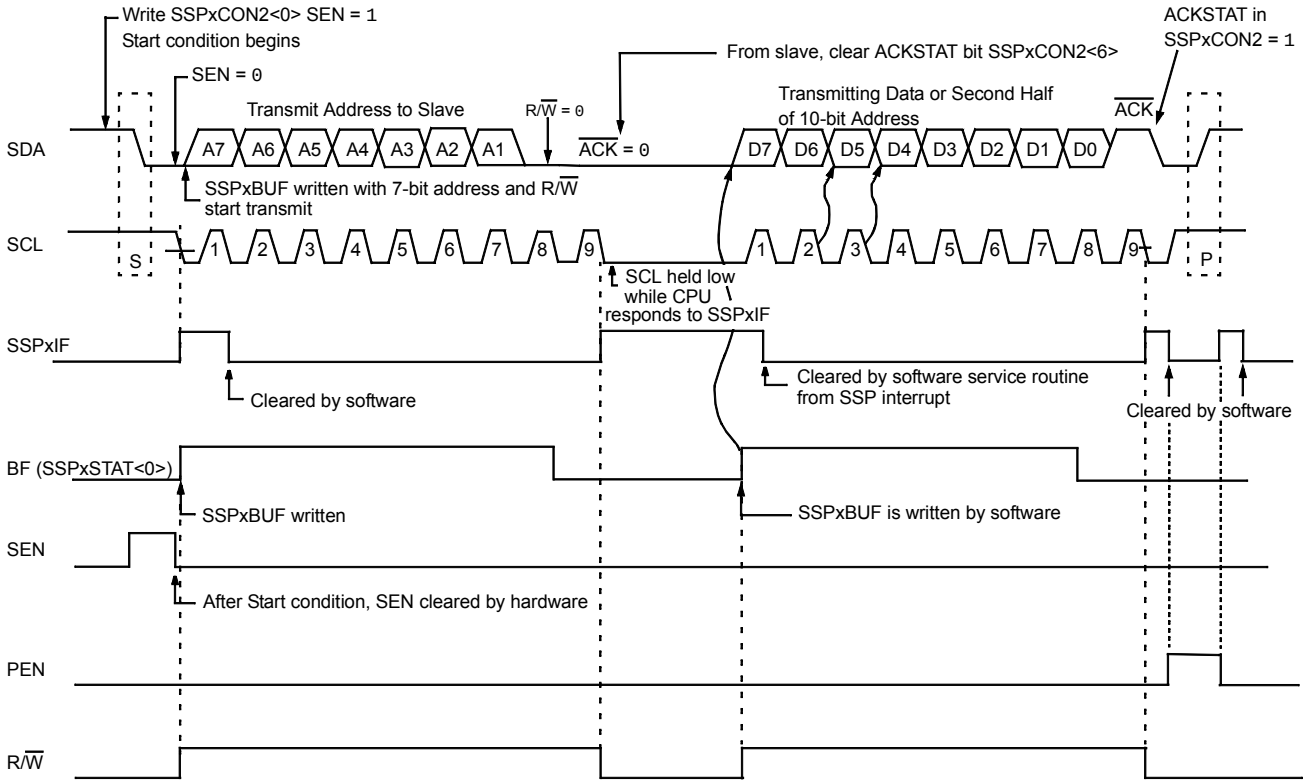
TABLE 32-1: SUMMARY OF REGISTERS ASSOCIATED WITH SPI OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	177
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—	187
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	132
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	133
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	139
RxyPPS	—	—	RxyPPS<5:0>						205
SSPCLKPPS	—	—	SSPCLKPPS<5:0>						205, 207
SSPDATPPS	—	—	SSPDATPPS<5:0>						205, 207
SSPSSPPS	—	—	SSPSSPPS<5:0>						205, 207
SSP1BUF	Synchronous Serial Port Receive Buffer/Transmit Register								444*
SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				489
SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	488
SSP1STAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	488
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	176
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	181
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	186

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the MSSP in SPI mode.

* Page provides register information.

FIGURE 32-28: I^2C MASTER MODE WAVEFORM (TRANSMISSION, 7 OR 10-BIT ADDRESS)



REGISTER 32-4: SSP1CON3: SSP CONTROL REGISTER 3

R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ACKTIM(3)	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **ACKTIM:** Acknowledge Time Status bit (I^2C mode only)(3)
1 = Indicates the I^2C bus is in an Acknowledge sequence, set on eighth falling edge of SCL clock
0 = Not an Acknowledge sequence, cleared on ninth rising edge of SCL clock

bit 6 **PCIE**: Stop Condition Interrupt Enable bit (I^2C slave mode only)
1 = Enable interrupt on detection of Stop condition
0 = Stop detection interrupts are disabled(2)

bit 5 **SCIE**: Start Condition Interrupt Enable bit (I^2C slave mode only)
1 = Enable interrupt on detection of Start or Restart conditions
0 = Start detection interrupts are disabled(2)

bit 4 **BOEN:** Buffer Overwrite Enable bit
In SPI Slave mode:(1)
1 = SSP1BUF updates every time that a new data byte is shifted in ignoring the BF bit
0 = If new byte is received with BF bit of the SSP1STAT register already set, SSPOV bit of the SSP1CON1 register is set, and the buffer is not updated
In I^2C Master mode and SPI Master mode:
This bit is ignored.
In I^2C Slave mode:
1 = SSP1BUF is updated and $\overline{ACK}$ is generated for a received address/data byte, ignoring the state of the SSPOV bit only if the BF bit = 0.
0 = SSP1BUF is only updated when SSPOV is clear

bit 3 **SDAHT:** SDA Hold Time Selection bit (I^2C mode only)
1 = Minimum of 300 ns hold time on SDA after the falling edge of SCL
0 = Minimum of 100 ns hold time on SDA after the falling edge of SCL

bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I^2C Slave mode only)
If, on the rising edge of SCL, SDA is sampled low when the module is outputting a high state, the BCL1IF bit of the PIR2 register is set, and bus goes idle
1 = Enable slave bus collision interrupts
0 = Slave bus collision interrupts are disabled

bit 1 **AHEN:** Address Hold Enable bit (I^2C Slave mode only)
1 = Following the eighth falling edge of SCL for a matching received address byte; CKP bit of the SSP1CON1 register will be cleared and the SCL will be held low.
0 = Address holding is disabled

bit 0 **DHEN:** Data Hold Enable bit (I^2C Slave mode only)
1 = Following the eighth falling edge of SCL for a received data byte; slave hardware clears the CKP bit of the SSP1CON1 register and SCL is held low.
0 = Data holding is disabled

Note 1: For daisy-chained SPI operation; allows the user to ignore all but the last received byte. SSPOV is still set when a new byte is received and BF = 1, but hardware continues to write the most recent byte to SSP1BUF.
2: This bit has no effect in Slave modes that Start and Stop condition detection is explicitly listed as enabled.
3: The ACKTIM Status bit is only active when the AHEN bit or DHEN bit is set.

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

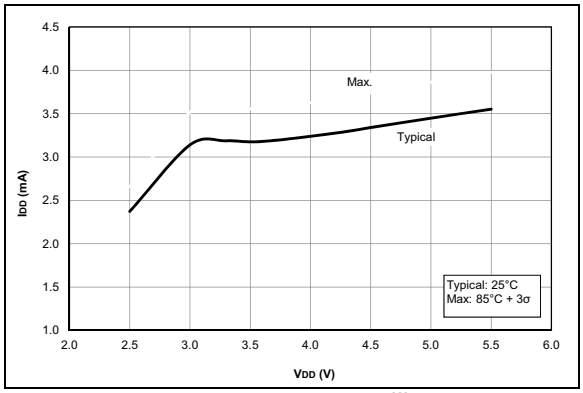


FIGURE 37-31: *IDD, HS Oscillator, 32 MHz (8 MHz + 4x PLL), PIC16F1777/8/9 Only.*

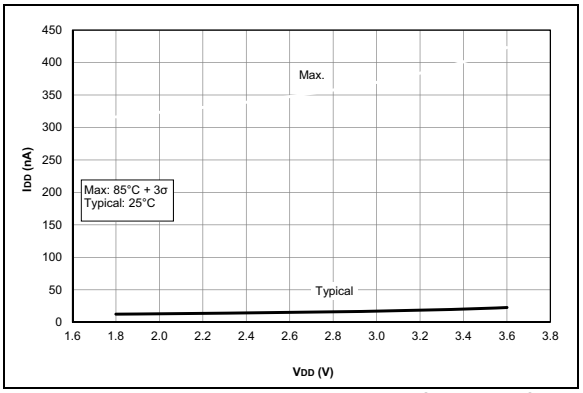


FIGURE 37-32: *IPD Base, LP Sleep Mode, PIC16LF1777/8/9 Only.*

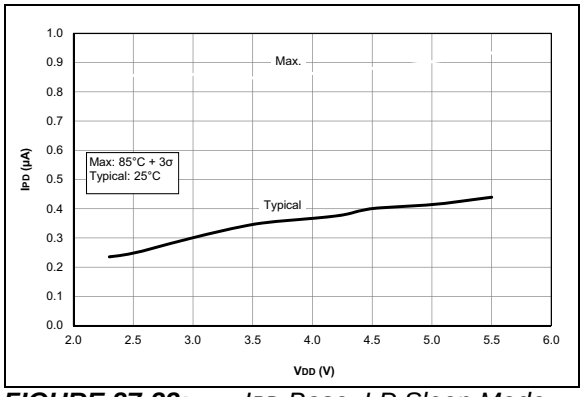


FIGURE 37-33: *IPD Base, LP Sleep Mode (VREGPM = 1), PIC16F1777/8/9 Only.*

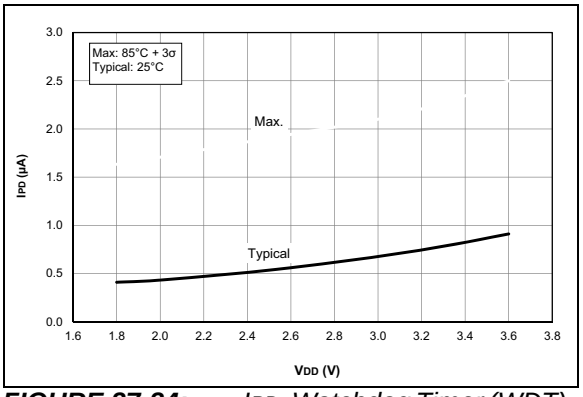


FIGURE 37-34: *IPD, Watchdog Timer (WDT), PIC16LF1777/8/9 Only.*

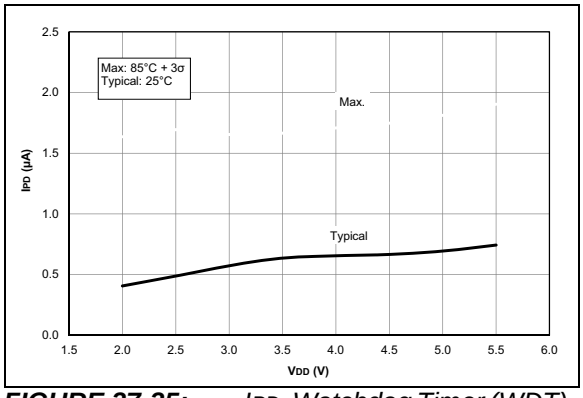


FIGURE 37-35: *IPD, Watchdog Timer (WDT), PIC16F1777/8/9 Only.*

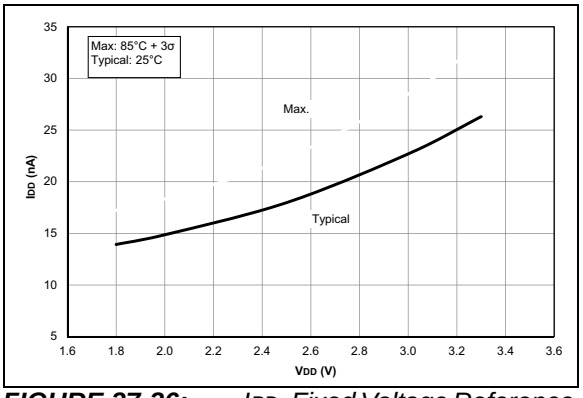
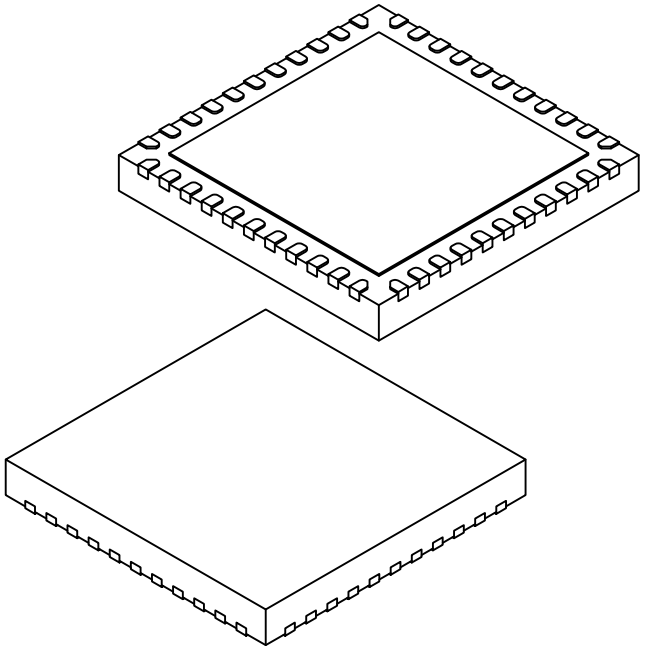


FIGURE 37-36: *IPD, Fixed Voltage Reference (FVR), ADC, PIC16LF1777/8/9 Only.*

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.25	6.45	6.60
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.25	6.45	6.60
Terminal Width	b	0.20	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103D Sheet 2 of 2