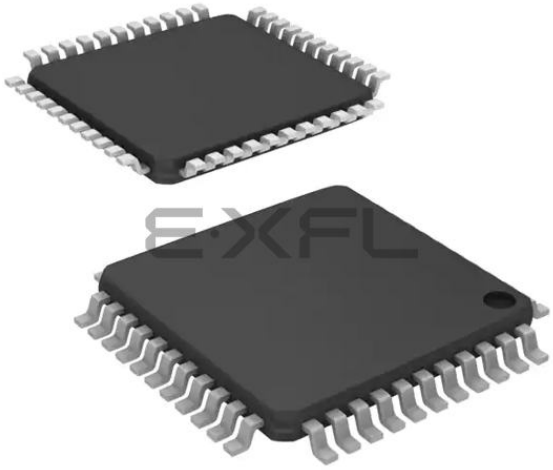

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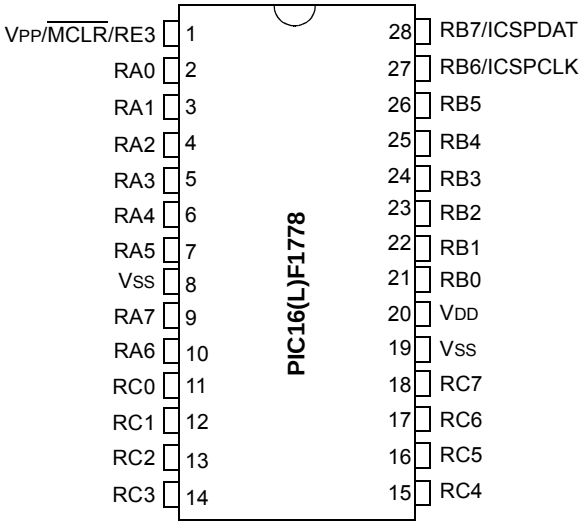
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 28x10b; D/A 4x5b, 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1779-i-pt

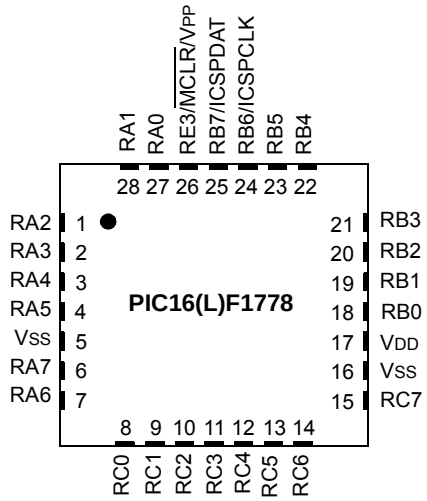
PIN DIAGRAMS

FIGURE 1: 28-PIN SPDIP, SOIC, SSOP



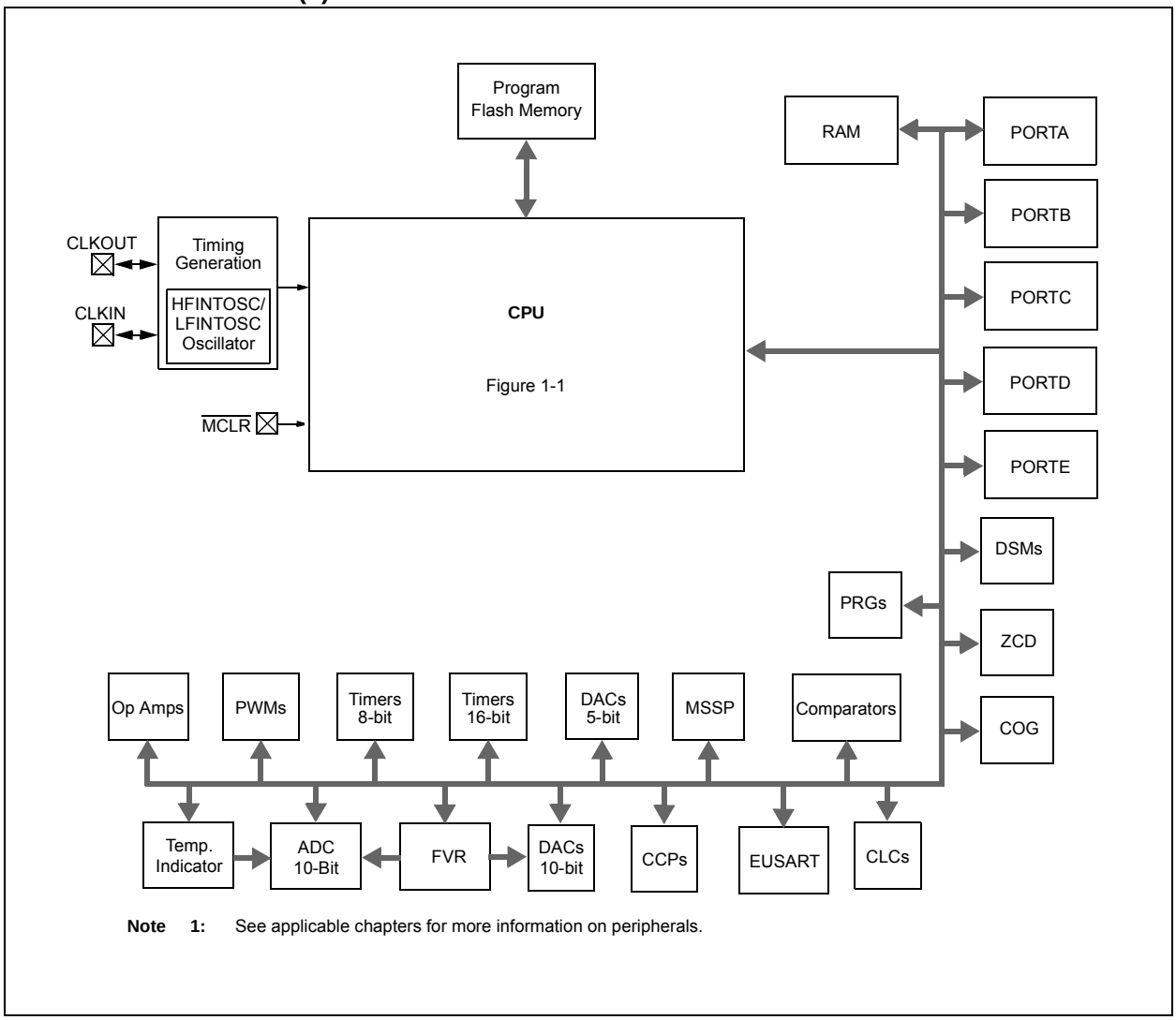
Note: See Table 3 for location of all peripheral functions.

FIGURE 2: 28-PIN UQFN (6x6x0.5 mm)



Note: See Table 3 for location of all peripheral functions.

FIGURE 1-1: PIC16(L)F1777/8/9 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.

3.2.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set an FSR to point to the program memory.

3.2.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

EXAMPLE 3-1: RETLW INSTRUCTION

```
constants
    BRW                 ;Add Index in W to
                        ;program counter to
                        ;select data
    RETLW DATA0         ;Index0 data
    RETLW DATA1         ;Index1 data
    RETLW DATA2
    RETLW DATA3


my_function
    ;… LOTS OF CODE…
    MOVLW       DATA_INDEX
    call constants
    ;… THE CONSTANT IS IN W
```

The BRW instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the BRW instruction is not available so the older table read method must be used.

3.2.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower eight bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The high directive will set bit<7> if a label points to a location in program memory.

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
  DW DATA0              ;First constant
  DW DATA1              ;Second constant
  DW DATA2
  DW DATA3
my_function
  ;… LOTS OF CODE…
  MOVLW  DATA_INDEX
  ADDLW  LOW constants
  MOVWF  FSR1L
  MOVLW  HIGH constants;MSb sets
                        automatically
  MOVWF  FSR1H
  BTFSC  STATUS, C      ;carry from ADDLW?
  INCF   FSR1H, f       ;yes
  MOVIW  0[FSR1]
;THE PROGRAM MEMORY IS IN W
```

TABLE 3-14: PIC16(L)F1778 MEMORY MAP, BANK 27-30

	Bank 27		Bank 28		Bank 29		Bank 30
D8Ch	—	E0Ch	PPSLOCK	E8Ch	—	F0Ch	—
D8Dh	—	E0Dh	INTPPS	E8Dh	—	F0Dh	—
D8Eh	PWMEN	E0Eh	T0CKIPPS	E8Eh	—	F0Eh	—
D8Fh	PWMLD	E0Fh	T1CKIPPS	E8Fh	—	F0Fh	CLCDATA
D90h	PWMOUT	E10h	T1GPPS	E90h	RA0PPS	F10h	CLC1CON
D91h	PWM5PHL	E11h	T3CKIPPS	E91h	RA1PPS	F11h	CLC1POL
D92h	PWM5PHH	E12h	T3GPPS	E92h	RA2PPS	F12h	CLC1SEL0
D93h	PWM5DCL	E13h	T5CKIPPS	E93h	RA3PPS	F13h	CLC1SEL1
D94h	PWM5DCH	E14h	T5GPPS	E94h	RA4PPS	F14h	CLC1SEL2
D95h	PWM5PRL	E15h	T2INPPS	E95h	RA5PPS	F15h	CLC1SEL3
D96h	PWM5PRH	E16h	T4INPPS	E96h	RA6PPS	F16h	CLC1GLS0
D97h	PWM5OFL	E17h	T6INPPS	E97h	RA7PPS	F17h	CLC1GLS1
D98h	PWM5OFH	E18h	T8INPPS	E98h	RB0PPS	F18h	CLC1GLS2
D99h	PWM5TMRL	E19h	CCP1PPS	E99h	RB1PPS	F19h	CLC1GLS3
D9Ah	PWM5TMRH	E1Ah	CCP2PPS	E9Ah	RB2PPS	F1Ah	CLC2CON
D9Bh	PWM5CON	E1Bh	CCP7PPS	E9Bh	RB3PPS	F1Bh	CLC2POL
D9Ch	PWM5INTE	E1Ch	—	E9Ch	RB4PPS	F1Ch	CLC2SEL0
D9Dh	PWM5INTF	E1Dh	COG1INPPS	E9Dh	RB5PPS	F1Dh	CLC2SEL1
D9Eh	PWM5CLKCON	E1Eh	COG2INPPS	E9Eh	RB6PPS	F1Eh	CLC2SEL2
D9Fh	PWM5LDCON	E1Fh	COG3INPPS	E9Fh	RB7PPS	F1Fh	CLC2SEL3
DA0h	PWM5OFCON	E20h	—	EA0h	RC0PPS	F20h	CLC2GLS0
DA1h	PWM6PHL	E21h	MD1CLPPS	EA1h	RC1PPS	F21h	CLC2GLS1
DA2h	PWM6PHH	E22h	MD1CHPPS	EA2h	RC2PPS	F22h	CLC2GLS2
DA3h	PWM6DCL	E23h	MD1MODPPS	EA3h	RC3PPS	F23h	CLC2GLS3
DA4h	PWM6DCH	E24h	MD2CLPPS	EA4h	RC4PPS	F24h	CLC3CON
DA5h	PWM6PRL	E25h	MD2CHPPS	EA5h	RC5PPS	F25h	CLC3POL
DA6h	PWM6PRH	E26h	MD2MODPPS	EA6h	RC6PPS	F26h	CLC3SEL0
DA7h	PWM6OFL	E27h	MD3CLPPS	EA7h	RC7PPS	F27h	CLC3SEL1
DA8h	PWM6OFH	E28h	MD3CHPPS	EA8h	—	F28h	CLC3SEL2
DA9h	PWM6TMRL	E29h	MD3MODPPS	EA9h	—	F29h	CLC3SEL3
DAAh	PWM6TMRH	E2Ah	—	EAAh	—	F2Ah	CLC3GLS0
DABh	PWM6CON	E2Bh	—	EABh	—	F2Bh	CLC3GLS1
DACh	PWM6INTE	E2Ch	—	EACh	—	F2Ch	CLC3GLS2
DADh	PWM6INTF	E2Dh	PRG1RPPS	EADh	—	F2Dh	CLC3GLS3
DAEh	PWM6CLKCON	E2Eh	PRG1FPPS	EAEh	—	F2Eh	CLC4CON
DAFh	PWM6LDCON	E2Fh	PRG2RPPS	EAFh	—	F2Fh	CLC4POL
DB0h	PWM6OFCON	E30h	PRG2FPPS	EB0h	—	F30h	CLC4SEL0
DB1h	PWM11PHL	E31h	PRG3FPPS	EB1h	—	F31h	CLC4SEL1
DB2h	PWM11PHH	E32h	PRG3RPPS	EB2h	—	F32h	CLC4SEL2
DB3h	PWM11DCL	E33h		EB3h	—	F33h	CLC4SEL3
DB4h	PWM11DCH	E34h		EB4h	—	F34h	CLC4GLS0
DB5h	PWM11PRL	E35h	CLCIN0PPS	EB5h	—	F35h	CLC4GLS1
DB6h	PWM11PRH	E36h	CLCIN1PPS	EB6h	—	F36h	CLC4GLS2
DB7h	PWM11OFL	E37h	CLCIN2PPS	EB7h	—	F37h	CLC4GLS3
DB8h	PWM11OFH	E38h	CLCIN3PPS	EB8h	—	F38h	—
DB9h	PWM11TMRL	E39h	ADCACTPPS	EB9h	—	F39h	—
DBAh	PWM11TMRH	E3Ah	SSPCLKPPS	EBAh	—	F3Ah	—
DBBh	PWM11CON	E3Bh	SSPDATPPS	EBBh	—	F3Bh	—
DBCh	PWM11INTE	E3Ch	SSPSSPPS	EBCh	—	F3Ch	—
DBDh	PWM11INTF	E3Dh	RXPPS	EBDh	—	F3Dh	—
DBEh	PWM11CLKCON	E3Eh	CKPPS	EBEh	—	F3Eh	—
DBFh	PWM11LDCON	E3Fh	—	EBFh	—	F3Fh	—
DC0h	PWM11OFCON	E40h		EC0h		F40h	
DC1h	—		—		—		—
DEFh		E6Fh		EEFh		F6Fh	

Legend: = Unimplemented data memory locations, read as '0',

TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 30											
F0Ch — F0Eh	—	Unimplemented								—	—
F0Fh	CLCDATA	—	—	—	—	MLC4OUT	MLC3OUT	MLC2OUT	MLC1OUT	---- x000	---- u000
F10h	CLC1CON	EN	—	OUT	INTP	INTN	MODE<2:0>			0-00 0000	0-00 0000
F11h	CLC1POL	POL	—	—	—	G4POL	G3POL	G2POL	G1POL	0--- xxxx	0--- uuuu
F12h	CLC1SEL0	—	—	D1S<5:0>						--xx xxxx	--uu uuuu
F13h	CLC1SEL1	—	—	D2S<5:0>						--xx xxxx	--uu uuuu
F14h	CLC1SEL2	—	—	D3S<5:0>						--xx xxxx	--uu uuuu
F15h	CLC1SEL3	—	—	D4S<5:0>						--xx xxxx	--uu uuuu
F16h	CLC1GLS0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	xxxx xxxx	uuuu uuuu
F17h	CLC1GLS1	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	xxxx xxxx	uuuu uuuu
F18h	CLC1GLS2	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	xxxx xxxx	uuuu uuuu
F19h	CLC1GLS3	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	xxxx xxxx	uuuu uuuu
F1Ah	CLC2CON	EN	—	OUT	INTP	INTN	MODE<2:0>			0-00 0000	0-00 0000
F1Bh	CLC2POL	POL	—	—	—	G4POL	G3POL	G2POL	G1POL	0--- xxxx	0--- uuuu
F1Ch	CLC2SEL0	—	—	D1S<5:0>						--xx xxxx	--uu uuuu
F1Dh	CLC2SEL1	—	—	D2S<5:0>						--xx xxxx	--uu uuuu
F1Eh	CLC2SEL2	—	—	D3S<5:0>						--xx xxxx	--uu uuuu
F1Fh	CLC2SEL3	—	—	D4S<5:0>						--xx xxxx	--uu uuuu
F20h	CLC2GLS0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	xxxx xxxx	uuuu uuuu
F21h	CLC2GLS1	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	xxxx xxxx	uuuu uuuu
F22h	CLC2GLS2	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	xxxx xxxx	uuuu uuuu
F23h	CLC2GLS3	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	xxxx xxxx	uuuu uuuu
F24h	CLC3CON	EN	—	OUT	INTP	INTN	MODE<2:0>			0-00 0000	0-00 0000
F25h	CLC3POL	POL	—	—	—	G4POL	G3POL	G2POL	G1POL	0--- xxxx	0--- uuuu
F26h	CLC3SEL0	—	—	D1S<5:0>						--xx xxxx	--uu uuuu
F27h	CLC3SEL1	—	—	D2S<5:0>						--xx xxxx	--uu uuuu
F28h	CLC3SEL2	—	—	D3S<5:0>						--xx xxxx	--uu uuuu
F29h	CLC3SEL3	—	—	D4S<5:0>						--xx xxxx	--uu uuuu
F2Ah	CLC3GLS0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

7.0 INTERRUPTS

The interrupt feature allows certain events to preempt normal program flow. Firmware is used to determine the source of the interrupt and act accordingly. Some interrupts can be configured to wake the MCU from Sleep mode.

This chapter contains the following information for Interrupts:

- Operation
- Interrupt Latency
- Interrupts During Sleep
- INT Pin
- Automatic Context Saving

Many peripherals produce interrupts. Refer to the corresponding chapters for details.

A block diagram of the interrupt logic is shown in Figure 7-1.

FIGURE 7-1: INTERRUPT LOGIC

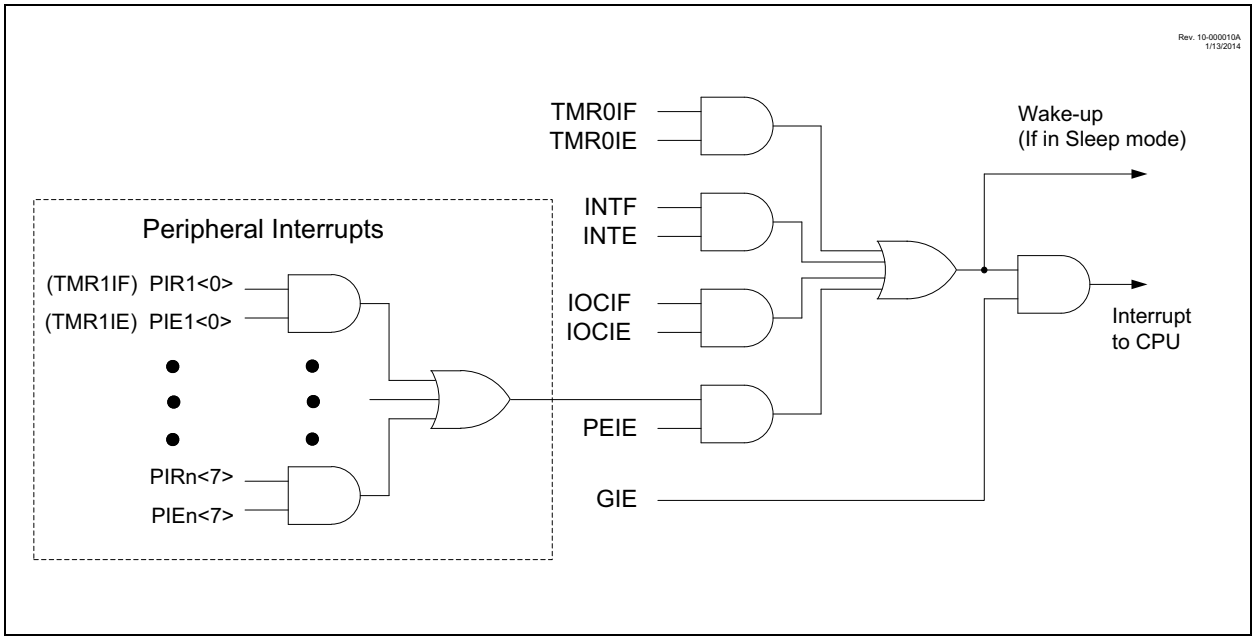
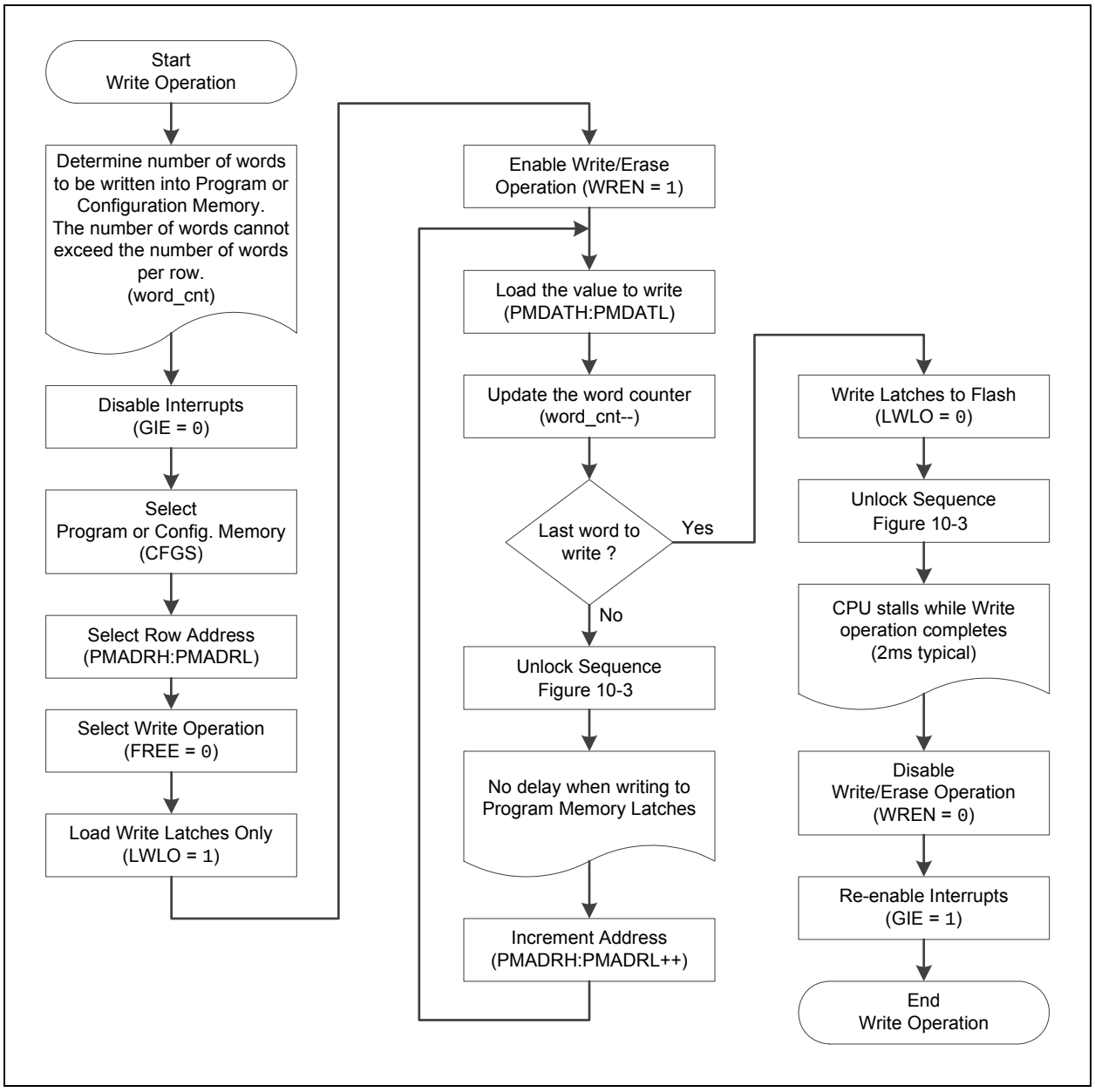


FIGURE 10-6: FLASH PROGRAM MEMORY WRITE FLOWCHART

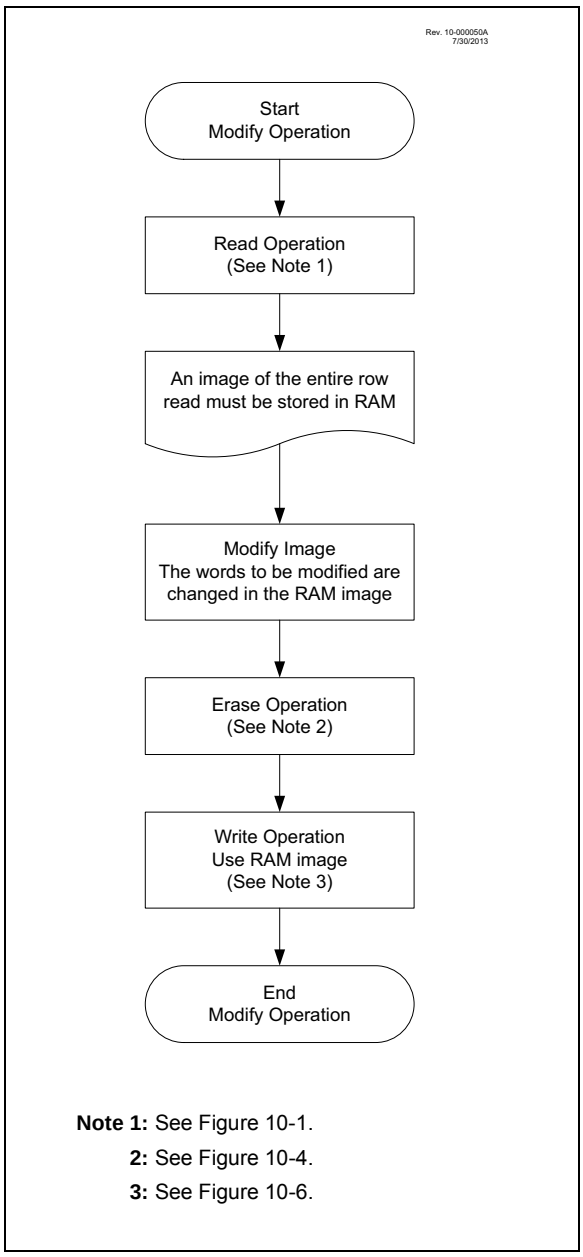


10.3 Modifying Flash Program Memory

When modifying existing data in a program memory row, and data within that row must be preserved, it must first be read and saved in a RAM image. Program memory is modified using the following steps:

1. Load the starting address of the row to be modified.
2. Read the existing data from the row into a RAM image.
3. Modify the RAM image to contain the new data to be written into program memory.
4. Load the starting address of the row to be rewritten.
5. Erase the program memory row.
6. Load the write latches with data from the RAM image.
7. Initiate a programming operation.

FIGURE 10-7: FLASH PROGRAM MEMORY MODIFY FLOWCHART



Note 1: See Figure 10-1.
2: See Figure 10-4.
3: See Figure 10-6.

REGISTER 10-5: PMCON1: PROGRAM MEMORY CONTROL 1 REGISTER

U-1	R/W-0/0	R/W-0/0	R/W/HC-0/0	R/W/HC-x/q[2]	R/W-0/0	R/S/HC-0/0	R/S/HC-0/0
—[1]	CFGS	LWLO[3]	FREE	WRERR	WREN	WR	RD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
S = Bit can only be set	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Bit is cleared by hardware

bit 7 **Unimplemented:** Read as '1'

bit 6 **CFGS:** Configuration Select bit
1 = Access Configuration, User ID and Device ID Registers
0 = Access Flash program memory

bit 5 **LWLO:** Load Write Latches Only bit[3]
1 = Only the addressed program memory write latch is loaded/updated on the next WR command
0 = The addressed program memory write latch is loaded/updated and a write of all program memory write latches will be initiated on the next WR command

bit 4 **FREE:** Program Flash Erase Enable bit
1 = Performs an erase operation on the next WR command (hardware cleared upon completion)
0 = Performs a write operation on the next WR command

bit 3 **WRERR:** Program/Erase Error Flag bit
1 = Condition indicates an improper program or erase sequence attempt or termination (bit is set automatically on any set attempt (write '1') of the WR bit).
0 = The program or erase operation completed normally

bit 2 **WREN:** Program/Erase Enable bit
1 = Allows program/erase cycles
0 = Inhibits programming/erasing of program Flash

bit 1 **WR:** Write Control bit
1 = Initiates a program Flash program/erase operation.
The operation is self-timed and the bit is cleared by hardware once operation is complete.
The WR bit can only be set (not cleared) in software.
0 = Program/erase operation to the Flash is complete and inactive

bit 0 **RD:** Read Control bit
1 = Initiates a program Flash read. Read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software.
0 = Does not initiate a program Flash read

Note 1: Unimplemented bit, read as '1'.
2: The WRERR bit is automatically set by hardware when a program memory write or erase operation is started (WR = 1).
3: The LWLO bit is ignored during a program memory erase operation (FREE = 1).

REGISTER 16-2: ADCON1: ADC CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **ADFM:** ADC Result Format Select bit
- 1 = Right justified. Six Most Significant bits of ADRESH are set to '0' when the conversion result is loaded.
- 0 = Left justified. Six Least Significant bits of ADRESL are set to '0' when the conversion result is loaded.

bit 6-4 **ADCS<2:0>:** ADC Conversion Clock Select bits
- 111 = FRC (clock supplied from an internal RC oscillator)
- 110 = FOSC/64
- 101 = FOSC/16
- 100 = FOSC/4
- 011 = FRC (clock supplied from an internal RC oscillator)
- 010 = FOSC/32
- 001 = FOSC/8
- 000 = FOSC/2

bit 3 **Unimplemented:** Read as '0'

bit 2 **ADNREF:** ADC Negative Voltage Reference Configuration bit
- 1 = VREF- is connected to external VREF- pin
- 0 = VREF- is connected to VSS

bit 1-0 **ADPREF<1:0>:** ADC Positive Voltage Reference Configuration bits
- 11 = VREF+ is connected to internal Fixed Voltage Reference (FVR) module(1)
- 10 = VREF+ is connected to external VREF+ pin(1)
- 01 = Reserved
- 00 = VREF+ is connected to VDD

Note 1: When selecting the VREF+ pin as the source of the positive reference, be aware that a minimum voltage specification exists. See Table 36-16: ADC Conversion Requirements for details.

REGISTER 24-4: CCPxCAP: CCPx CAPTURE INPUT SELECTION REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	CTS<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Reset
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **CTS<3:0>:** Capture Trigger Input Selection bits

1101 = IOC_event
1100 = LC4_output
1011 = LC3_output
1010 = LC2_output
1001 = LC1_output
1000 = C8_sync_out(1)
0111 = C7_sync_out(1)
0110 = C6_sync_out
0101 = C5_sync_out
0100 = C4_sync_out
0011 = C3_sync_out
0010 = C2_sync_out
0001 = C1_sync_out
0000 = Pin selected with the CCPxPPS register

Note 1: PIC16LF1777/9 only.

REGISTER 25-2: PWMxDCH: PWM DUTY CYCLE HIGH BITS

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
DC<9:2>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **DC<9:2>:** PWM Duty Cycle Most Significant bits
These bits are the MSbs of the PWM duty cycle. The two LSbs are found in the PWMxDCL Register.

REGISTER 25-3: PWMxDCL: PWM DUTY CYCLE LOW BITS

R/W-x/u	R/W-x/u	U-0	U-0	U-0	U-0	U-0	U-0
DC<1:0>		—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **DC<1:0>:** PWM Duty Cycle Least Significant bits
These bits are the LSbs of the PWM duty cycle. The MSbs are found in the PWMxDCH Register.

bit 5-0 **Unimplemented:** Read as ‘0’

TABLE 27-7: SUMMARY OF REGISTERS ASSOCIATED WITH COGx(1)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	177
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	182
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—	187
COGxASD0	ASE	ARSEN	ASDBD<1:0>		ASDAC<1:0>		—	—	384
COGxASD1	AS7E	AS6E	AS5E	AS4E	AS3E	AS2E	AS1E	AS0E	385
COGxBLKR	—	—	BLKR<5:0>						388
COGxBLKF	—	—	BLKF<5:0>						388
COGxCON0	EN	LD	—	CS<1:0>		MD<2:0>			378
COGxCON1	RDBS	FDBS	—	—	POLD	POLC	POLB	POLA	379
COGxDBR	—	—	DBR<5:0>						387
COGxDBF	—	—	DBF<5:0>						387
COGxFIS0	FIS7	FIS6	FIS5	FIS4	FIS3	FIS2	FIS1	FIS0	382
COGxFIS1	FIS15	FIS14	FIS13	FIS12	FIS11	FIS10	FIS9	FIS8	382
COGxFSIM0	FSIM7	FSIM6	FSIM5	FSIM4	FSIM3	FSIM2	FSIM1	FSIM0	383
COGxFSIM1	FSIM15	FSIM14	FSIM13	FSIM12	FSIM11	FSIM10	FSIM9	FSIM8	383
COGxPHR	—	—	PHR<5:0>						389
COGxPHF	—	—	PHF<5:0>						389
COGxPPS	—	—	COG1PPS<5:0>						205, 207
COGxRIS0	RIS7	RIS6	RIS5	RIS4	RIS3	RIS2	RIS1	RIS0	380
COGxRIS1	RIS15	RIS14	RIS13	RIS12	RIS11	RIS10	RIS9	RIS8	380
COGxRSIM0	RSIM7	RSIM6	RSIM5	RSIM4	RSIM3	RSIM2	RSIM1	RSIM0	381
COGxRSIM1	RSIM15	RSIM14	RSIM13	RSIM12	RSIM11	RSIM10	RSIM9	RSIM8	381
COGxSTR	SDATD	SDATC	SDATB	SDATA	STRD	STRC	STRB	STRA	386
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	132
RxyPPS	—	—	RxyPPS<5:0>						205

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by COG.

Note 1: COG4 is available on PIC16(L)F1777/9 only.

28.6 Register Definitions: CLC Control

Long bit name prefixes for the CLC peripherals are shown in Table 28-3. Refer to **Section 1.1 "Register and Bit naming conventions"** for more information

TABLE 28-3:

Peripheral	Bit Name Prefix
CLC1	LC1
CLC2	LC2
CLC3	LC3
CLC4	LC4

REGISTER 28-1: CLCxCON: CONFIGURABLE LOGIC CELL CONTROL REGISTER

R/W-0/0	U-0	R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EN	—	OUT	INTP	INTN	MODE<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **EN:** Configurable Logic Cell Enable bit
- 1 = Configurable logic cell is enabled and mixing input signals
- 0 = Configurable logic cell is disabled and has logic zero output

bit 6 **Unimplemented:** Read as '0'

bit 5 **OUT:** Configurable Logic Cell Data Output bit
Read-only: logic cell output data, after POL; sampled from lcx_out wire.

bit 4 **INTP:** Configurable Logic Cell Positive Edge Going Interrupt Enable bit
- 1 = CLCxIF will be set when a rising edge occurs on lcx_out
- 0 = CLCxIF will not be set

bit 3 **INTN:** Configurable Logic Cell Negative Edge Going Interrupt Enable bit
- 1 = CLCxIF will be set when a falling edge occurs on lcx_out
- 0 = CLCxIF will not be set

bit 2-0 **MODE<2:0>:** Configurable Logic Cell Functional Mode bits
- 111 = Cell is 1-input transparent latch with S and R
- 110 = Cell is J-K flip-flop with R
- 101 = Cell is 2-input D flip-flop with R
- 100 = Cell is 1-input D flip-flop with S and R
- 011 = Cell is S-R latch
- 010 = Cell is 4-input AND
- 001 = Cell is OR-XOR
- 000 = Cell is AND-OR

The MSSP consists of a transmit/receive shift register (SSPSR) and a buffer register (SSPxBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPxBUF holds the data that was written to the SSPSR until the received data is ready. Once the eight bits of data have been received, that byte is moved to the SSPxBUF register. Then, the Buffer Full Detect bit, BF of the SSPxSTAT register, and the interrupt flag bit, SSPxIF, are set. This double-buffering of the received data (SSPxBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPxBUF register during transmission/reception of data will be ignored and the Write Collision Detect bit WCOL of the SSPxCON1 register, will be set. User software must clear the WCOL bit to allow the following write(s) to the SSPxBUF register to complete successfully.

When the application software is expecting to receive valid data, the SSPxBUF should be read before the next byte of data to transfer is written to the SSPxBUF. The Buffer Full bit, BF of the SSPxSTAT register, indicates when SSPxBUF has been loaded with the received data (transmission is complete). When the SSPxBUF is read, the BF bit is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally, the MSSP interrupt is used to determine when the transmission/reception has completed. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur.

The SSPSR is not directly readable or writable and can only be accessed by addressing the SSPxBUF register. Additionally, the SSPxSTAT register indicates the various Status conditions.

FIGURE 32-5: SPI MASTER/SLAVE CONNECTION

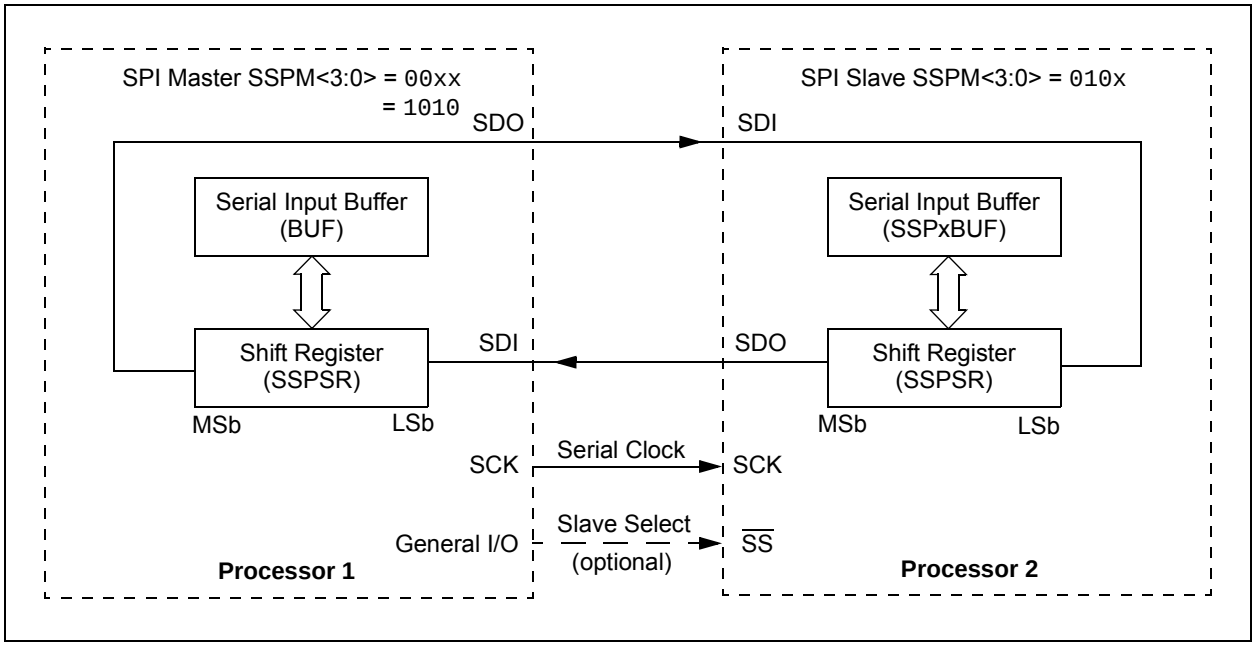


TABLE 33-5: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
	FOSC = 32.000 MHz			FOSC = 20.000 MHz			FOSC = 18.432 MHz			FOSC = 11.0592 MHz		
	Actual Rate	% Error	SPxBRG value (decimal)	Actual Rate	% Error	SPxBRG value (decimal)	Actual Rate	% Error	SPxBRG value (decimal)	Actual Rate	% Error	SPxBRG value (decimal)
300	300.0	0.00	26666	300.0	0.00	16665	300.0	0.00	15359	300.0	0.00	9215
1200	1200	0.00	6666	1200	-0.01	4166	1200	0.00	3839	1200	0.00	2303
2400	2400	0.01	3332	2400	0.02	2082	2400	0.00	1919	2400	0.00	1151
9600	9604	0.04	832	9597	-0.03	520	9600	0.00	479	9600	0.00	287
10417	10417	0.00	767	10417	0.00	479	10425	0.08	441	10433	0.16	264
19.2k	19.18k	-0.08	416	19.23k	0.16	259	19.20k	0.00	239	19.20k	0.00	143
57.6k	57.55k	-0.08	138	57.47k	-0.22	86	57.60k	0.00	79	57.60k	0.00	47
115.2k	115.9k	0.64	68	116.3k	0.94	42	115.2k	0.00	39	115.2k	0.00	23

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
	FOSC = 8.000 MHz			FOSC = 4.000 MHz			FOSC = 3.6864 MHz			FOSC = 1.000 MHz		
	Actual Rate	% Error	SPxBRG value (decimal)	Actual Rate	% Error	SPxBRG value (decimal)	Actual Rate	% Error	SPxBRG value (decimal)	Actual Rate	% Error	SPxBRG value (decimal)
300	300.0	0.00	6666	300.0	0.01	3332	300.0	0.00	3071	300.1	0.04	832
1200	1200	-0.02	1666	1200	0.04	832	1200	0.00	767	1202	0.16	207
2400	2401	0.04	832	2398	0.08	416	2400	0.00	383	2404	0.16	103
9600	9615	0.16	207	9615	0.16	103	9600	0.00	95	9615	0.16	25
10417	10417	0	191	10417	0.00	95	10473	0.53	87	10417	0.00	23
19.2k	19.23k	0.16	103	19.23k	0.16	51	19.20k	0.00	47	19.23k	0.16	12
57.6k	57.14k	-0.79	34	58.82k	2.12	16	57.60k	0.00	15	—	—	—
115.2k	117.6k	2.12	16	111.1k	-3.55	8	115.2k	0.00	7	—	—	—

TABLE 36-3: POWER-DOWN CURRENTS (I_{PD})(1,2)

PIC16LF1777/8/9		Operating Conditions: (unless otherwise stated) Low-Power Sleep Mode						
PIC16F1777/8/9		Low-Power Sleep Mode, VREGPM = 1						
Param No.	Device Characteristics	Min.	Typ†	Max. +85°C	Max. +125°C	Units	Conditions	
							V_{DD}	Note
D023	Base I_{PD}	—	0.05	1.0	8.0	µA	1.8	WDT, BOR, FVR, and SOSC disabled, all Peripherals Inactive
		—	0.08	2.0	9.0	µA	3.0	
D023	Base I_{PD}	—	0.3	2.4	10	µA	2.3	WDT, BOR, FVR, and SOSC disabled, all Peripherals Inactive, Low-Power Sleep mode
		—	0.4	4	12	µA	3.0	
		—	0.5	6	15	µA	5.0	
D023A	Base I_{PD}	—	9.8	17	28	µA	2.3	WDT, BOR, FVR and SOSC disabled, all Peripherals inactive, Normal Power Sleep mode VREGPM = 0
		—	10.3	20	40	µA	3.0	
		—	11.5	22	44	µA	5.0	
D024		—	0.5	6	14	µA	1.8	WDT Current
		—	0.8	7	17	µA	3.0	
D024		—	0.8	6	15	µA	2.3	WDT Current
		—	0.9	7	20	µA	3.0	
		—	1.0	8	22	µA	5.0	
D025		—	15	28	30	µA	1.8	FVR Current (ADC)
		—	24	35	38	µA	3.0	
D025		—	18	33	35	µA	2.3	FVR Current (ADC)
		—	24	35	40	µA	3.0	
		—	26	37	44	µA	5.0	
D025A		—	25	50	55	µA	1.8	FVR Current (DAC)
		—	30	65	70	µA	3.0	
D025A		—	30	55	66	µA	2.3	FVR Current (DAC)
		—	32	68	82	µA	3.0	
		—	35	77	90	µA	5.0	
D026		—	7.5	25	28	µA	3.0	BOR Current
D026		—	10	25	28	µA	3.0	BOR Current
		—	12	28	31	µA	5.0	
D027		—	0.5	4	10	µA	3.0	LPBOR Current
D027		—	0.8	6	15	µA	3.0	LPBOR Current
		—	1	8	17	µA	5.0	
D028		—	0.5	5	9	µA	1.8	SOSC Current
		—	0.8	8.5	12	µA	3.0	
D028		—	1.1	6	10	µA	2.3	SOSC Current
		—	1.3	8.5	20	µA	3.0	
		—	1.4	10	25	µA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base I_{PD} and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base I_{DD} or I_{PD} current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{SS}.

3: ADC clock source is FRC.

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

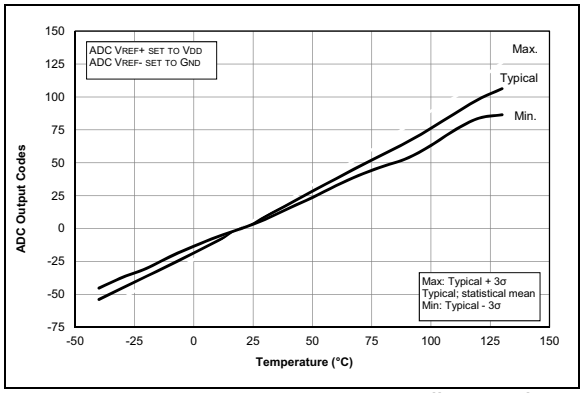


FIGURE 37-91: *Temperature Indicator Slope Normalized to 20°C, Low Range, V_{DD} = 3.0V, PIC16F1777/8/9 only.*

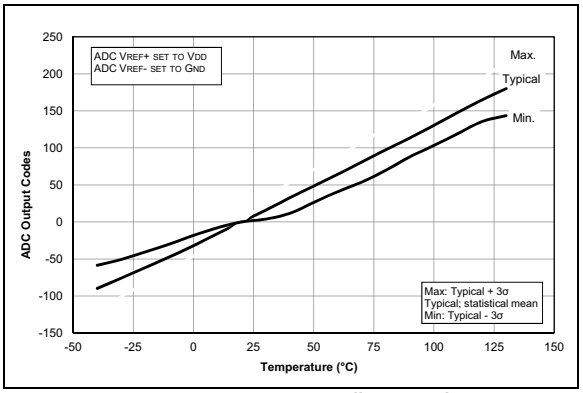


FIGURE 37-92: *Temp. Indicator Slope Normalized to 20°C, Low Range, V_{DD} = 1.8V, PIC16LF1773/6 Only.*

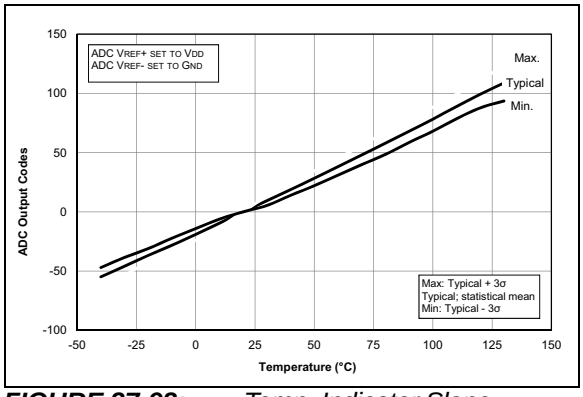


FIGURE 37-93: *Temp. Indicator Slope Normalized to 20°C, Low Range, V_{DD} = 3.0V, PIC16LF1773/6 Only.*

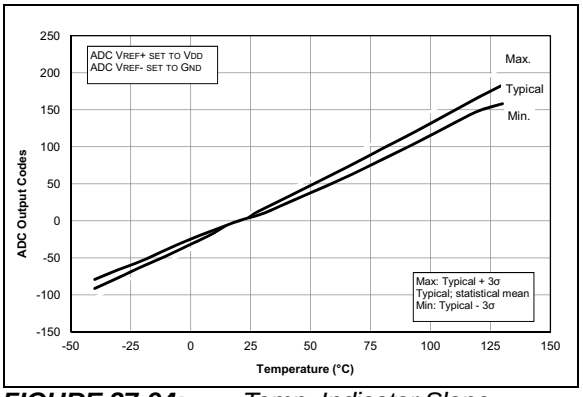


FIGURE 37-94: *Temp. Indicator Slope Normalized to 20°C, High Range, V_{DD} = 3.6V, PIC16LF1773/6 Only.*

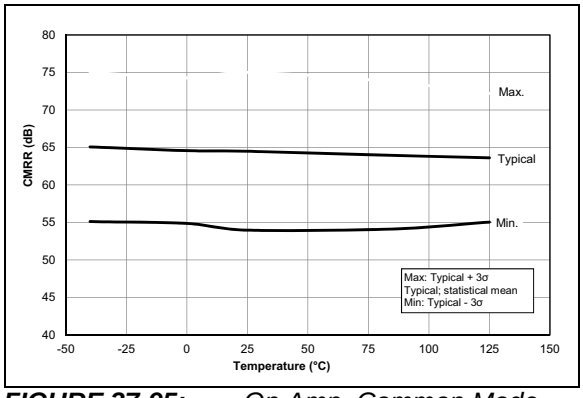


FIGURE 37-95: *Op Amp, Common Mode Rejection Ratio (CMRR), V_{DD} = 3.0V.*

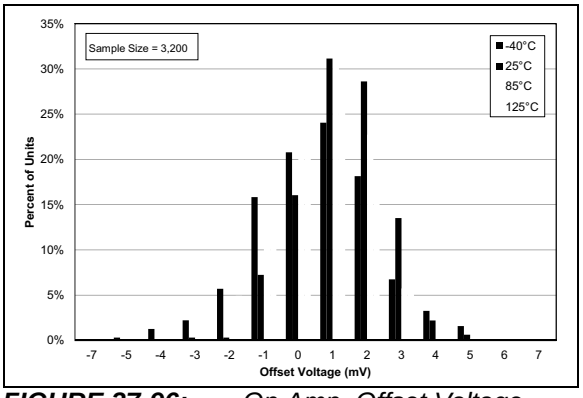
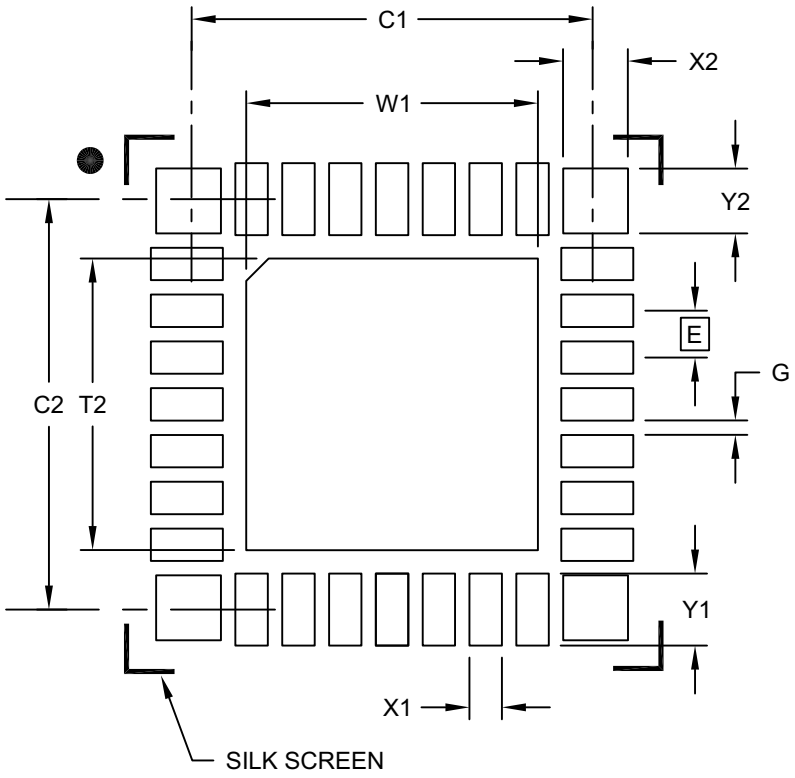


FIGURE 37-96: *Op Amp, Offset Voltage Histogram, V_{DD} = 3.0V, V_{CM} = V_{DD}/2.*

28-Lead Plastic Quad Flat, No Lead Package (MX) - 6x6 mm Body [UQFN] With 0.60mm Contact Length And Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W1			4.05
Optional Center Pad Length	T2			4.05
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.00
Corner Pad Width (X4)	X2			0.90
Corner Pad Length (X4)	Y2			0.90
Distance Between Pads	G	0.20		

Notes:

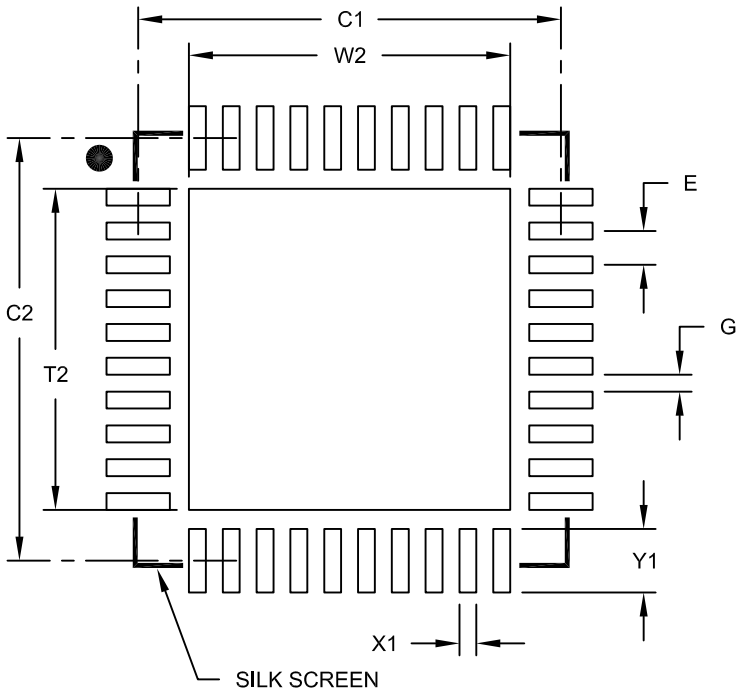
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2209B

40-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) - 5x5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	W2			3.80
Optional Center Pad Length	T2			3.80
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X40)	X1			0.20
Contact Pad Length (X40)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2156B