

Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 28x10b; D/A 4x5b, 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1779t-i-ml

TABLE 1-2: PIC16(L)F1778 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA3/AN3/VREF+/DAC1REF0+/ DAC2REF0+/DAC3REF0+/ DAC4REF0+/DAC5REF0+/ DAC7REF0+/C1IN1+/MD1CL	RA3	TTL/ST	CMOS	General purpose I/O.
	AN3	AN	—	ADC Channel 3 input.
	VREF+	AN	—	ADC positive reference.
	DAC1REF0+	AN	—	DAC1 positive reference.
	DAC2REF0+	AN	—	DAC2 positive reference.
	DAC3REF0+	AN	—	DAC3 positive reference.
	DAC4REF0+	AN	—	DAC4 positive reference.
	DAC5REF0+	AN	—	DAC5 positive reference.
	DAC7REF0+	AN	—	DAC7 positive reference.
	C1IN1+	AN	—	Comparator 1 positive input.
	MD1CL ⁽¹⁾	TTL/ST	—	Data signal modulator 1 low carrier input.
RA4/OPA1IN0+/PRG1R/ MD1CH/DAC4OUT1/T0CKI	RA4	TTL/ST	CMOS	General purpose I/O.
	OPA1IN0+	AN	—	Operational Amplifier 1 non-inverting input.
	PRG1R ⁽¹⁾	TTL/ST	—	Ramp generator set_rising input.
	MD1CH ⁽¹⁾	TTL/ST	—	Data signal modulator 1 high carrier input.
	DAC4OUT1	—	AN	DAC4 voltage output.
	T0CKI ⁽¹⁾	TTL/ST	—	Timer0 clock input.
RA5/AN4/OPA1IN0-/ DAC2OUT1/PRG1F/ MD1MOD/SS	RA5	TTL/ST	CMOS	General purpose I/O.
	AN4	AN	—	ADC Channel 4 input.
	OPA1IN0-	AN	—	Operational amplifier 1 inverting input.
	DAC2OUT1	—	AN	DAC2 voltage output.
	PRG1F ⁽¹⁾	TTL/ST	—	Ramp generator set_falling input.
	MD1MOD ⁽¹⁾	TTL/ST	—	Data signal modulator modulation input.
RA6/CLKOUT/C6IN1+/OSC2	SS	ST	—	Slave Select input.
	RA6	TTL/ST	CMOS	General purpose I/O.
	CLKOUT	—	CMOS	Fosc/4 output.
	C6IN1+	AN	—	Comparator 6 positive input.
RA7/CLKIN/OSC1	OSC2	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	RA7	TTL/ST	CMOS	General purpose I/O.
	CLKIN	TTL/ST	—	CLC input.
RB0/AN12/ZCD/HIB0/C2IN1+/ COG1IN	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	RB0	TTL/ST	CMOS	General purpose I/O.
	AN12	AN	—	ADC Channel 12 input.
	ZCD	AN	—	Zero-cross detection input.
	HIB0	HP	HP	High-Power output.
	C2IN1+	AN	—	Comparator 2 positive input.
	COG1IN ⁽¹⁾	TTL/ST	—	Complementary output generator 1 input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C = Schmitt Trigger input with I²C
HP = High Power XTAL = Crystal levels

- Note** 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.
2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 3-3: PIC16(L)F1778 MEMORY MAP (BANKS 0-7)

BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7	
000h	Core Registers (Table 3-2)	080h	Core Registers (Table 3-2)	100h	Core Registers (Table 3-2)	180h	Core Registers (Table 3-2)	200h	Core Registers (Table 3-2)	280h	Core Registers (Table 3-2)	300h	Core Registers (Table 3-2)	380h	Core Registers (Table 3-2)
00Bh		08Bh		10Bh		18Bh		20Bh		28Bh		30Bh		38Bh	
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	WPUA	28Ch	ODCONA	30Ch	SLRCONA	38Ch	INLVLA
00Dh	PORTB	08Dh	TRISB	10Dh	LATB	18Dh	ANSELB	20Dh	WPUB	28Dh	ODCONB	30Dh	SLRCONB	38Dh	INLVLB
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	ANSELC	20Eh	WPUC	28Eh	ODCONC	30Eh	SLRCONC	38Eh	INLVLC
00Fh	—	08Fh	—	10Fh	—	18Fh	—	20Fh	—	28Fh	—	30Fh	—	38Fh	—
010h	PORTE	090h	TRISE	110h	—	190h	—	210h	WPUE	290h	—	310h	—	390h	INLVLE
011h	PIR1	091h	PIE1	111h	CMOUT	191h	PMADRL	211h	SSP1BUF	291h	CCPR1L	311h	—	391h	IOCAP
012h	PIR2	092h	PIE2	112h	CM1CON0	192h	PMADRH	212h	SSP1ADD	292h	CCPR1H	312h	—	392h	IOCAN
013h	PIR3	093h	PIE3	113h	CM1CON1	193h	PMDATL	213h	SSP1MSK	293h	CCP1CON	313h	—	393h	IOCAF
014h	PIR4	094h	PIE4	114h	CM1NSEL	194h	PMDATH	214h	SSP1STAT	294h	CCP1CAP	314h	—	394h	IOCBP
015h	PIR5	095h	PIE5	115h	CM1PSEL	195h	PMCON1	215h	SSP1CON1	295h	CCPR2L	315h	MD1CON0	395h	IOCBN
016h	PIR6	096h	PIE6	116h	CM2CON0	196h	PMCON2	216h	SSP1CON2	296h	CCPR2H	316h	MD1CON1	396h	IOCBF
017h	TMR0	097h	OPTION_REG	117h	CM2CON1	197h	VREGCON ⁽¹⁾	217h	SSP1CON3	297h	CCP2CON	317h	MD1SRC	397h	IOCCP
018h	TMR1L	098h	PCON	118h	CM2NSEL	198h	—	218h	—	298h	CCP2CAP	318h	MD1CARL	398h	IOCCN
019h	TMR1H	099h	WDTCON	119h	CM2PSEL	199h	RC1REG	219h	—	299h	CCPR7L	319h	MD1CARH	399h	IOCCF
01Ah	T1CON	09Ah	OSCTUNE	11Ah	CM3CON0	19Ah	TX1REG	21Ah	—	29Ah	CCPR7H	31Ah	—	39Ah	—
01Bh	T1GCON	09Bh	OSCCON	11Bh	CM3CON1	19Bh	SP1BRGL	21Bh	MD3CON0	29Bh	CCP7CON	31Bh	MD2CON0	39Bh	—
01Ch	TMR3L	09Ch	OSCSTAT	11Ch	CM3NSEL	19Ch	SP1BRGH	21Ch	MD3CON1	29Ch	CCP7CAP	31Ch	MD2CON1	39Ch	—
01Dh	TMR3H	09Dh	BORCON	11Dh	CM3PSEL	19Dh	RC1STA	21Dh	MD3SRC	29Dh	—	31Dh	MD2SRC	39Dh	IOCEP
01Eh	T3CON	09Eh	FVRCON	11Eh	—	19Eh	TX1STA	21Eh	MD3CARL	29Eh	CCPTMRS1	31Eh	MD2CARL	39Eh	IOCEN
01Fh	T3GCON	09Fh	ZCD1CON	11Fh	—	19Fh	BAUD1CON	21Fh	MD3CARH	29Fh	CCPTMRS2	31Fh	MD2CARH	39Fh	IOCEF
020h	General Purpose Register 80 Bytes	0A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h	General Purpose Register 80 Bytes	220h	General Purpose Register 80 Bytes	2A0h	General Purpose Register 80 Bytes	320h	General Purpose Register 80 Bytes	3A0h	General Purpose Register 80 Bytes
06Fh		0EFh		16Fh		1EFh		26Fh		2EFh		36Fh		3EFh	
070h	Common RAM 70h – 7Fh	0F0h	Accesses 70h – 7Fh	170h	Accesses 70h – 7Fh	1F0h	Accesses 70h – 7Fh	270h	Accesses 70h – 7Fh	2F0h	Accesses 70h – 7Fh	370h	Accesses 70h – 7Fh	3F0h	Accesses 70h – 7Fh
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		37Fh		3FFh	

Legend: ■ = Unimplemented data memory locations, read as '0'.

Note 1: Unimplemented on PIC16LF1778.

TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 27											
D8Ch	—	Unimplemented								—	—
D8Dh	—	Unimplemented								—	—
D8Eh	PWMEN	—	—	—	—	MPWM12EN ⁽³⁾	MPWM11EN	MPWM6EN	MPWM5EN	---- 0000	---- 0000
D8Fh	PWMLD	—	—	—	—	MPWM12LD ⁽³⁾	MPWM11LD	MPWM6LD	MPWM5LD	---- 0000	---- 0000
D90h	PWMOUT	—	—	—	—	MPWM12OUT ⁽³⁾	MPWM11OUT	MPWM6OUT	MPWM5OUT	---- 0000	---- 0000
D91h	PWM5PHL	PH<7:0>								xxxx xxxx	uuuu uuuu
D92h	PWM5PHH	PH<15:8>								xxxx xxxx	uuuu uuuu
D93h	PWM5DCL	DC<7:0>								xxxx xxxx	uuuu uuuu
D94h	PWM5DCH	DC<15:8>								xxxx xxxx	uuuu uuuu
D95h	PWM5PRL	PR<7:0>								xxxx xxxx	uuuu uuuu
D96h	PWM5PRH	PR<15:8>								xxxx xxxx	uuuu uuuu
D97h	PWM5OFL	OF<7:0>								xxxx xxxx	uuuu uuuu
D98h	PWM5OFH	OF<15:8>								xxxx xxxx	uuuu uuuu
D99h	PWM5TMRL	TMR<7:0>								0000 0000	0000 0000
D9Ah	PWM5TMRH	TMR<15:8>								0000 0000	0000 0000
D9Bh	PWM5CON	EN	—	OUT	POL	MODE<1:0>		—	—	0-00 00--	0-00 00--
D9Ch	PWM5INTE	—	—	—	—	OFIE	PHIE	DCIE	PRIE	---- 0000	---- 0000
D9Dh	PWM5INTF	—	—	—	—	OFIF	PHIF	DCIF	PRIF	---- 0000	---- 0000
D9Eh	PWM5CLKCON	—	PS<2:0>			—	—	CS<1:0>		-000 --00	-000 --00
D9Fh	PWM5LDCON	LDA	LDT	—	—	—	—	LDS<1:0>		00-- --00	00-- --00
DA0h	PWM5OFCON	—	OFM<1:0>		OFO	—	—	OFS<1:0>		-000 --00	-000 --00
DA1h	PWM6PHL	PH<7:0>								xxxx xxxx	uuuu uuuu
DA2h	PWM6PHH	PH<15:8>								xxxx xxxx	uuuu uuuu
DA3h	PWM6DCL	DC<7:0>								xxxx xxxx	uuuu uuuu
DA4h	PWM6DCH	DC<15:8>								xxxx xxxx	uuuu uuuu
DA5h	PWM6PRL	PR<7:0>								xxxx xxxx	uuuu uuuu
DA6h	PWM6PRH	PR<15:8>								xxxx xxxx	uuuu uuuu
DA7h	PWM6OFL	OF<7:0>								xxxx xxxx	uuuu uuuu
DA8h	PWM6OFH	OF<15:8>								xxxx xxxx	uuuu uuuu
DA9h	PWM6TMRL	TMR<7:0>								0000 0000	0000 0000
DAAh	PWM6TMRH	TMR<15:8>								0000 0000	0000 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

- Note** 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 30 (Continued)											
F2Bh	CLC3GLS1	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	xxxx xxxx	uuuu uuuu
F2Ch	CLC3GLS2	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	xxxx xxxx	uuuu uuuu
F2Dh	CLC3GLS3	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	xxxx xxxx	uuuu uuuu
F2Eh	CLC4CON	EN	OE	OUT	INTP	INTN	MODE<2:0>			0000 0000	0000 0000
F2Fh	CLC4POL	POL	—	—	—	G4POL	G3POL	G2POL	G1POL	0--- xxxx	0--- uuuu
F30h	CLC4SEL0	D1S<7:0>								xxxx xxxx	uuuu uuuu
F31h	CLC4SEL1	D2S<7:0>								xxxx xxxx	uuuu uuuu
F32h	CLC4SEL2	D3S<7:0>								xxxx xxxx	uuuu uuuu
F33h	CLC4SEL3	D4S<7:0>								xxxx xxxx	uuuu uuuu
F34h	CLC4GLS0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	xxxx xxxx	uuuu uuuu
F35h	CLC4GLS1	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	xxxx xxxx	uuuu uuuu
F36h	CLC4GLS2	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	xxxx xxxx	uuuu uuuu
F37h	CLC4GLS3	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	xxxx xxxx	uuuu uuuu
F2Eh — F6Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, c = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

6.13 Power Control (PCON) Register

The PCON register bits are shown in Register 6-2.

The Power Control (PCON) register contains flag bits to differentiate between a:

- Power-on Reset ($\overline{\text{POR}}$)
- Brown-out Reset ($\overline{\text{BOR}}$)
- Reset Instruction Reset ($\overline{\text{RI}}$)
- MCLR Reset ($\overline{\text{RMCLR}}$)
- Watchdog Timer Reset ($\overline{\text{RWDT}}$)
- Stack Underflow Reset (STKUNF)
- Stack Overflow Reset (STKOVF)

6.14 Register Definitions: Power Control

REGISTER 6-2: PCON: POWER CONTROL REGISTER

R/W/HS-0/q	R/W/HS-0/q	U-0	R/W/HC-1/q	R/W/HC-1/q	R/W/HC-1/q	R/W/HC-q/u	R/W/HC-q/u
STKOVF	STKUNF	—	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
bit 7							bit 0

Legend:

HC = Bit is cleared by hardware

HS = Bit is set by hardware

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-m/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

q = Value depends on condition

bit 7 **STKOVF:** Stack Overflow Flag bit

1 = A Stack Overflow occurred

0 = A Stack Overflow has not occurred or cleared by firmware

bit 6 **STKUNF:** Stack Underflow Flag bit

1 = A Stack Underflow occurred

0 = A Stack Underflow has not occurred or cleared by firmware

bit 5 **Unimplemented:** Read as '0'

bit 4 **$\overline{\text{RWDT}}$:** Watchdog Timer Reset Flag bit

1 = A Watchdog Timer Reset has not occurred or set to '1' by firmware

0 = A Watchdog Timer Reset has occurred (cleared by hardware)

bit 3 **$\overline{\text{RMCLR}}$:** MCLR Reset Flag bit

1 = A $\overline{\text{MCLR}}$ Reset has not occurred or set to '1' by firmware

0 = A MCLR Reset has occurred (cleared by hardware)

bit 2 **$\overline{\text{RI}}$:** RESET Instruction Flag bit

1 = A RESET instruction has not been executed or set to '1' by firmware

0 = A RESET instruction has been executed (cleared by hardware)

bit 1 **$\overline{\text{POR}}$:** Power-on Reset Status bit

1 = No Power-on Reset occurred

0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{\text{BOR}}$:** Brown-out Reset Status bit

1 = No Brown-out Reset occurred

0 = A Brown-out Reset occurred (must be set in software after a Power-on Reset or Brown-out Reset occurs)

REGISTER 11-14: ODCONB: PORTB OPEN-DRAIN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ODB7	ODB6	ODB5	ODB4	ODB3	ODB2	ODB1	ODB0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ODB<7:0>:** PORTB Open-Drain Enable bits
 For RB<7:0> pins
 1 = Port pin operates as open-drain drive (sink current only)
 0 = Port pin operates as standard push-pull drive (source and sink current)

REGISTER 11-15: SLRCONB: PORTB SLEW RATE CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
SLRB7	SLRB6	SLRB5	SLRB4	SLRB3	SLRB2	SLRB1	SLRB0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **SLRB<7:0>:** PORTB Slew Rate Enable bits
 For RB<7:0> pins
 1 = Port pin slew rate is limited
 0 = Port pin slews at maximum rate

REGISTER 11-16: INLVLB: PORTB INPUT LEVEL CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
INLVLB7	INLVLB6	INLVLB5	INLVLB4	INLVLB3	INLVLB2	INLVLB1	INLVLB0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **INLVLB<7:0>:** PORTB Input Level Select bits
 For RB<7:0> pins
 1 = Port pin digital input operates with ST thresholds
 0 = Port pin digital input operates with TTL thresholds

PIC16(L)F1777/8/9

TABLE 11-5: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSEL	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—	187
INLVLC	INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	189
LATC	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	187
ODCONC	ODC7	ODC6	ODC5	ODC4	ODC3	ODC2	ODC1	ODC0	188
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	186
SLRCONC	SLRC7	SLRC6	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0	189
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	186
WPUC	WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	188

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTC.

11.7 PORTD Registers (PIC16(L)F1777/9 only)

11.7.1 DATA REGISTER

PORTD is an 8-bit wide bidirectional port in the PIC16(L)F1777/8/9 devices. The corresponding data direction register is TRISD (Register 11-27). Setting a TRISD bit (= 1) will make the corresponding PORTD pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISD bit (= 0) will make the corresponding PORTD pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 11-1 shows how to initialize an I/O port.

Reading the PORTD register (Register 11-26) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATD).

11.7.2 DIRECTION CONTROL

The TRISD register (Register 11-27) controls the PORTD pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISD register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

11.7.3 INPUT THRESHOLD CONTROL

The INLVLD register (Register 11-33) controls the input voltage threshold for each of the available PORTD input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTD register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Table 36-4: I/O Ports for more information on threshold levels.

Note: Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

11.7.4 OPEN-DRAIN CONTROL

The ODCOND register (Register 11-31) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCOND bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCOND bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

11.7.5 SLEW RATE CONTROL

The SLRCOND register (Register 11-32) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCOND bit is set, the corresponding port pin drive is slew rate limited. When an SLRCOND bit is cleared, The corresponding port pin drive slews at the maximum rate possible.

11.7.6 ANALOG CONTROL

The ANSELD register (Register 11-29) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELD bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELD bits has no effect on digital output functions. A pin with TRIS clear and ANSELD set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note: The ANSELD bits default to the Analog mode after reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

11.7.7 PORTD FUNCTIONS AND OUTPUT PRIORITIES

Each pin defaults to the PORT latch data after reset. Other functions are selected with the peripheral pin select logic. See **Section 12.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELD register. Digital output functions may continue to control the pin when it is in Analog mode.

13.0 INTERRUPT-ON-CHANGE

All pins on all ports can be configured to operate as Interrupt-on-Change (IOC) pins. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual pin, or combination of pins, can be configured to generate an interrupt. The interrupt-on-change module has the following features:

- Interrupt-on-Change enable (Master Switch)
- Individual pin configuration
- Rising and falling edge detection
- Individual pin interrupt flags

Figure 13-1 is a block diagram of the IOC module.

13.1 Enabling the Module

To allow individual pins to generate an interrupt, the IOCIE bit of the INTCON register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

13.2 Individual Pin Configuration

For each pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated bit of the IOCxP register is set. To enable a pin to detect a falling edge, the associated bit of the IOCxN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting the associated bits in both of the IOCxP and IOCxN registers.

13.3 Interrupt Flags

The bits located in the IOCxF registers are status flags that correspond to the Interrupt-on-Change pins of each port. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the INTCON register reflects the status of all IOCxF bits.

13.4 Clearing Interrupt Flags

The individual status flags, (IOCxF register bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

EXAMPLE 13-1: CLEARING INTERRUPT FLAGS (PORTA EXAMPLE)

```
MOVLW    0xff
XORWF    IOCAF, W
ANDWF    IOCAF, F
```

13.5 Operation in Sleep

The Interrupt-on-Change interrupt sequence will wake the device from Sleep mode, if the IOCIE bit is set.

If an edge is detected while in Sleep mode, the affected IOCxF register will be updated prior to the first instruction executed out of Sleep.

REGISTER 13-10: IOCEP: INTERRUPT-ON-CHANGE PORTE POSITIVE EDGE REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	U-0	U-0	U-0
—	—	—	—	IOCEP3	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **IOCEP3:** Interrupt-on-Change PORTE Positive Edge Enable bits

1 = Interrupt-on-Change enabled on the pin for a positive going edge. IOCEPx bit and IOCIF flag will be set upon detecting an edge.

0 = Interrupt-on-Change disabled for the associated pin.

bit 2-0 **Unimplemented:** Read as '0'

REGISTER 13-11: IOCEN: INTERRUPT-ON-CHANGE PORTE NEGATIVE EDGE REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	U-0	U-0	U-0
—	—	—	—	IOCEN3	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-4 **Unimplemented:** Read as '0'

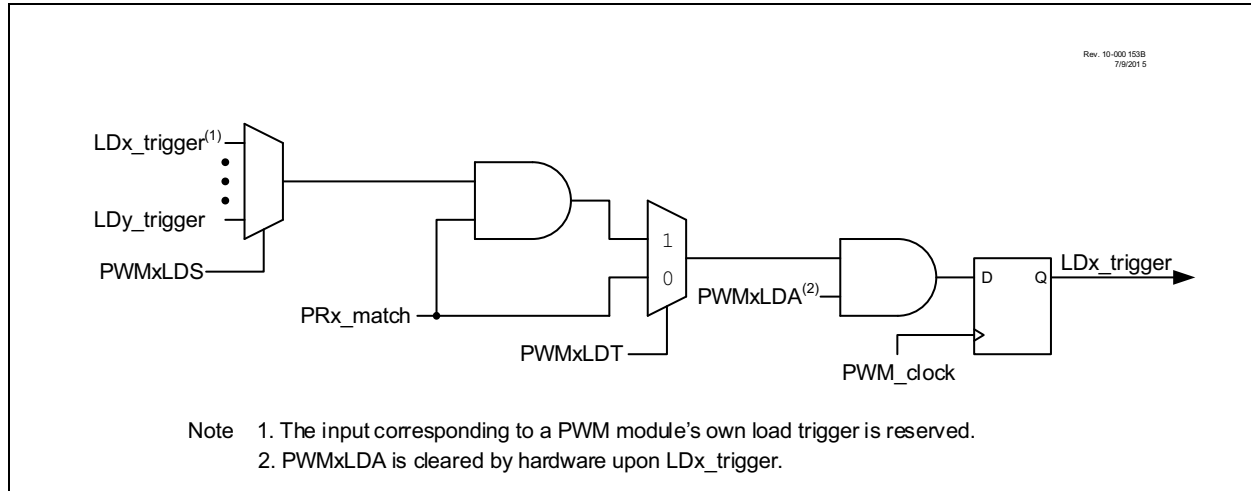
bit 3 **IOCEN3:** Interrupt-on-Change PORTE Negative Edge Enable bits

1 = Interrupt-on-Change enabled on the pin for a negative going edge. IOCEPx bit and IOCIF flag will be set upon detecting an edge.

0 = Interrupt-on-Change disabled for the associated pin.

bit 2-0 **Unimplemented:** Read as '0'

FIGURE 26-2: LOAD TRIGGER BLOCK DIAGRAM



26.1 Fundamental Operation

The PWM module produces a 16-bit resolution pulse-width modulated output.

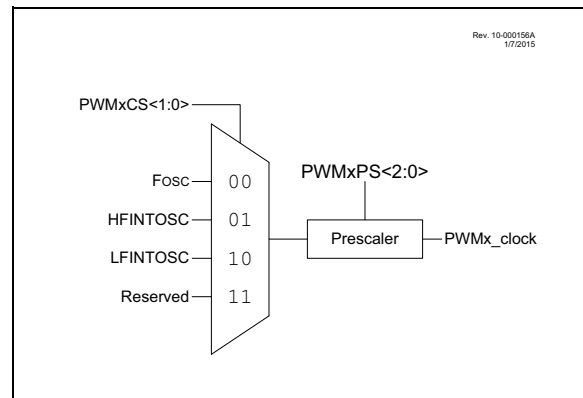
Each PWM module has an independent timer driven by a selection of clock sources determined by the PWMxCLKCON register (Register 26-4). The timer value is compared to event count registers to generate the various events of a the PWM waveform, such as the period and duty cycle. For a block diagram describing the clock sources refer to Figure 26-3.

Each PWM module can be enabled individually using the EN bit of the PWMxCON register, or several PWM modules can be enabled simultaneously using the MPWMxEN bits of the PWMEN register.

The current state of the PWM output can be read using the OUT bit of the PWMxCON register. In some modes this bit can be set and cleared by software giving additional software control over the PWM waveform. This bit is synchronized to Fosc/4 and therefore does not change in real time with respect to the PWM_clock.

Note: If PWM_clock > Fosc/4, the OUT bit may not accurately represent the output state of the PWM.

FIGURE 26-3: PWM CLOCK SOURCE BLOCK DIAGRAM



26.1.1 PWMx PIN CONFIGURATION

This device uses the PPS control circuitry to route peripherals to any device I/O pin. Select the desired pin, or pins, for PWM output with the device pin RxyPPS control registers (Register 12-2).

All PWM outputs are multiplexed with the PORT data latch, so the pins must also be configured as outputs by clearing the associated PORT TRIS bits.

The slew rate feature may be configured to optimize the rate to be used in conjunction with the PWM outputs. High-speed output switching is attained by clearing the associated PORT SLRCON bits.

The PWM outputs can be configured to be open-drain outputs by setting the associated PORT ODCON bits.

26.1.2 PWMx Output Polarity

The output polarity is inverted by setting the POL bit of the PWMxCON register. The polarity control affects the PWM output even when the module is not enabled.

27.3.3 HALF-BRIDGE MODE

In Half-Bridge mode, the COG generates a two output complementary PWM waveform from rising and falling event sources. In the simplest configuration, the rising and falling event sources are the same signal, which is a PWM signal with the desired period and duty cycle. The COG converts this single PWM input into a dual complementary PWM output. The frequency and duty cycle of the dual PWM output match those of the single input PWM signal. The off-to-on transition of each output can be delayed from the on-to-off transition of the other output, thereby, creating a time immediately after the PWM transition where neither output is driven. This is referred to as dead-band time and is covered in **Section 27.7 “Dead-Band Control”**.

The half-bridge configuration is shown in Figure 27-5. A typical operating waveform, with dead band, generated from a single CCP1 input is shown in Figure 27-9.

The primary output is available on either, or both, COGxA and COGxC. The complementary output is available on either, or both, COGxB and COGxD.

Half-Bridge mode is selected by setting the MD<2:0> bits of the COGxCON0 register to '100'.

27.3.4 PUSH-PULL MODE

In Push-Pull mode, the COG generates a single PWM output that alternates between the two pairs of the COG outputs at every PWM period. COGxA has the same signal as COGxC. COGxB has the same signal as COGxD. The output drive activates with the rising input event and terminates with the falling event input. Each rising event starts a new period and causes the output to switch to the COG pair not used in the previous period.

The Push-Pull configuration is shown in Figure 27-6. A typical Push-Pull waveform generated from a single CCP1 input is shown in Figure 27-11.

Push-Pull mode is selected by setting the MD<2:0> bits of the COGxCON0 register to '101'.

PIC16(L)F1777/8/9

REGISTER 27-16: COGxBLKR: COG RISING EVENT BLANKING COUNT REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
		BLKR<5:0>					
bit 7							
							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **BLKR<5:0>:** Rising Event Blanking Count Value bits
= Number of COGx clock periods to inhibit falling event inputs

REGISTER 27-17: COGxBLKF: COG FALLING EVENT BLANKING COUNT REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
		BLKF<5:0>					
bit 7							
							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

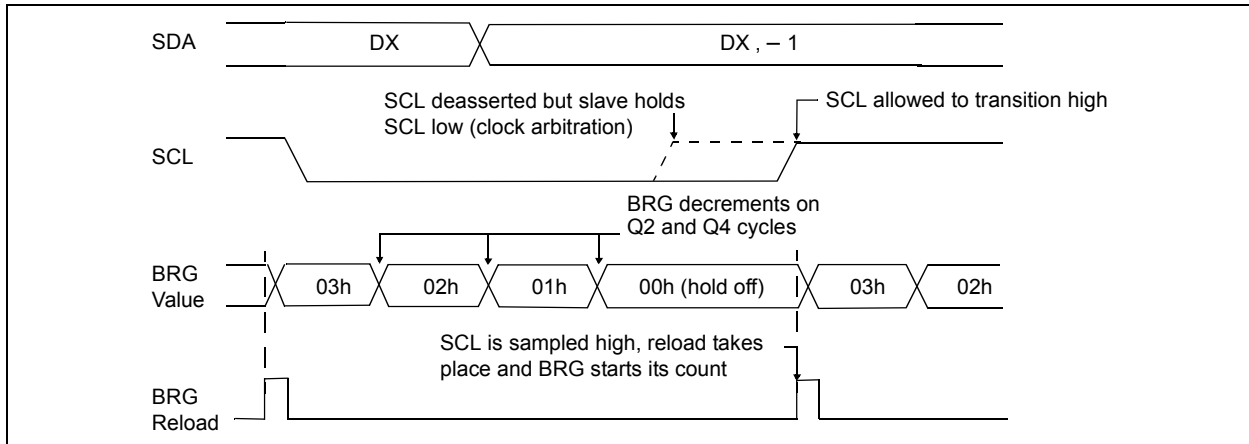
bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **BLKF<5:0>:** Falling Event Blanking Count Value bits
= Number of COGx clock periods to inhibit rising event inputs

32.6.2 CLOCK ARBITRATION

Clock arbitration occurs when the master, during any receive, transmit or Repeated Start/Stop condition, releases the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the Baud Rate Generator (BRG) is suspended from counting until the SCL pin is actually sampled high. When the SCL pin is sampled high, the Baud Rate Generator is reloaded with the contents of SSPxADD<7:0> and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count in the event that the clock is held low by an external device (Figure 32-25).

FIGURE 32-25: BAUD RATE GENERATOR TIMING WITH CLOCK ARBITRATION



32.6.3 WCOL STATUS FLAG

If the user writes the SSPxBUF when a Start, Restart, Stop, Receive or Transmit sequence is in progress, the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur). Any time the WCOL bit is set it indicates that an action on SSPxBUF was attempted while the module was not idle.

Note: Because queuing of events is not allowed, writing to the lower five bits of SSPxCON2 is disabled until the Start condition is complete.

DECFSZ Decrement f, Skip if 0

Syntax: `[label] DECFSZ f,d`

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) - 1 \rightarrow (\text{destination})$;
skip if result = 0

Status Affected: None

Description: The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a 2-cycle instruction.

INCFSZ Increment f, Skip if 0

Syntax: `[label] INCFSZ f,d`

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) + 1 \rightarrow (\text{destination})$,
skip if result = 0

Status Affected: None

Description: The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2-cycle instruction.

GOTO Unconditional Branch

Syntax: `[label] GOTO k`

Operands: $0 \leq k \leq 2047$

Operation: $k \rightarrow PC<10:0>$
 $PCLATH<6:3> \rightarrow PC<14:11>$

Status Affected: None

Description: GOTO is an unconditional branch. The 11-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a 2-cycle instruction.

IORLW Inclusive OR literal with W

Syntax: `[label] IORLW k`

Operands: $0 \leq k \leq 255$

Operation: $(W) .OR. k \rightarrow (W)$

Status Affected: Z

Description: The contents of the W register are OR'ed with the 8-bit literal 'k'. The result is placed in the W register.

INCF Increment f

Syntax: `[label] INCF f,d`

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) + 1 \rightarrow (\text{destination})$

Status Affected: Z

Description: The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

IORWF Inclusive OR W with f

Syntax: `[label] IORWF f,d`

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(W) .OR. (f) \rightarrow (\text{destination})$

Status Affected: Z

Description: Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

Note: Unless otherwise noted, $V_{IN} = 5V$, $F_{OSC} = 300\text{ kHz}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$.

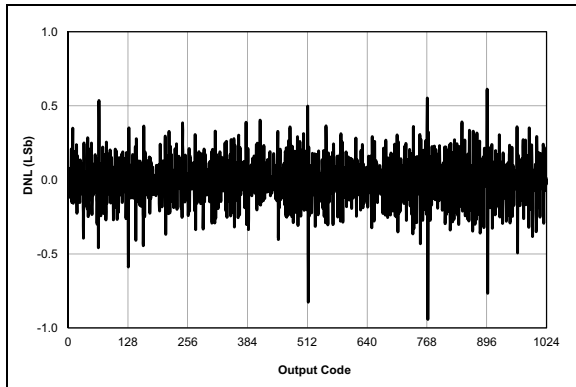


FIGURE 37-79: ADC 10-bit Mode, Single-Ended DNL, $V_{DD} = 3.0V$, $T_{AD} = 4\text{ }\mu\text{S}$, 25°C .

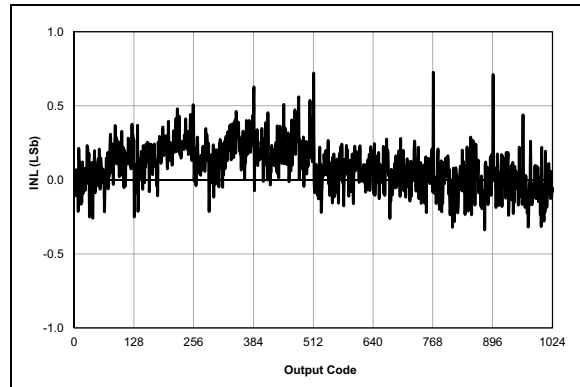


FIGURE 37-80: ADC 10-bit Mode, Single-Ended INL, $V_{DD} = 3.0V$, $T_{AD} = 1\text{ }\mu\text{S}$, 25°C .

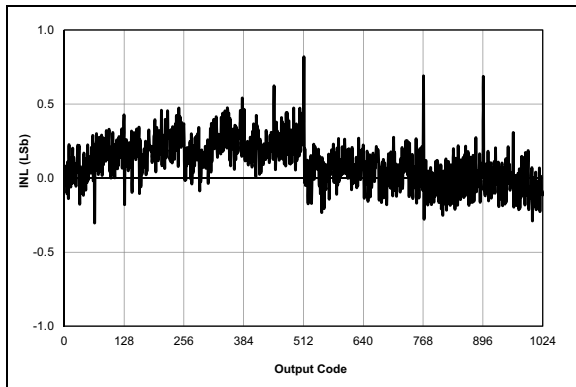


FIGURE 37-81: ADC 10-bit Mode, Single-Ended INL, $V_{DD} = 3.0V$, $T_{AD} = 4\text{ }\mu\text{S}$, 25°C .

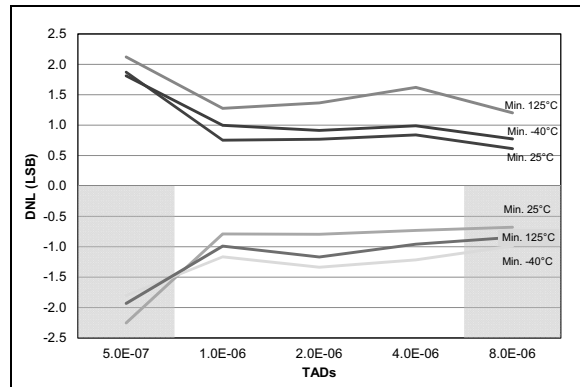


FIGURE 37-82: ADC 10-bit Mode, Single-Ended DNL, $V_{DD} = 3.0V$, $V_{REF} = 3.0V$.

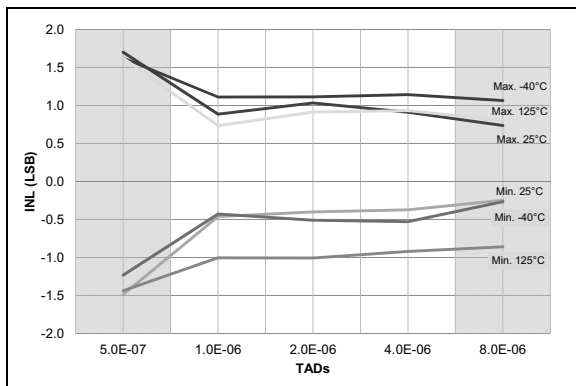


FIGURE 37-83: ADC 10-bit Mode, Single-Ended INL, $V_{DD} = 3.0V$, $V_{REF} = 3.0V$.

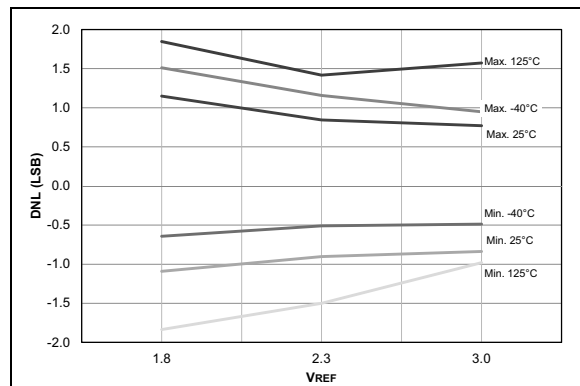
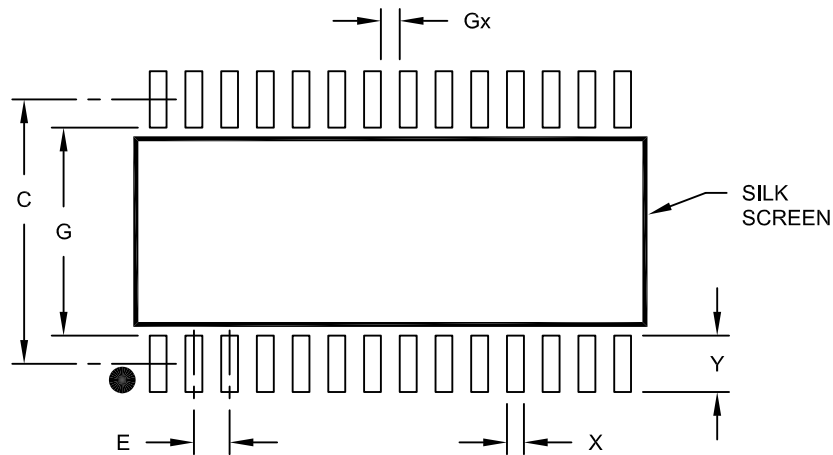


FIGURE 37-84: ADC 10-bit Mode, Single-Ended DNL, $V_{DD} = 3.0V$, $T_{AD} = 1\text{ }\mu\text{S}$.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

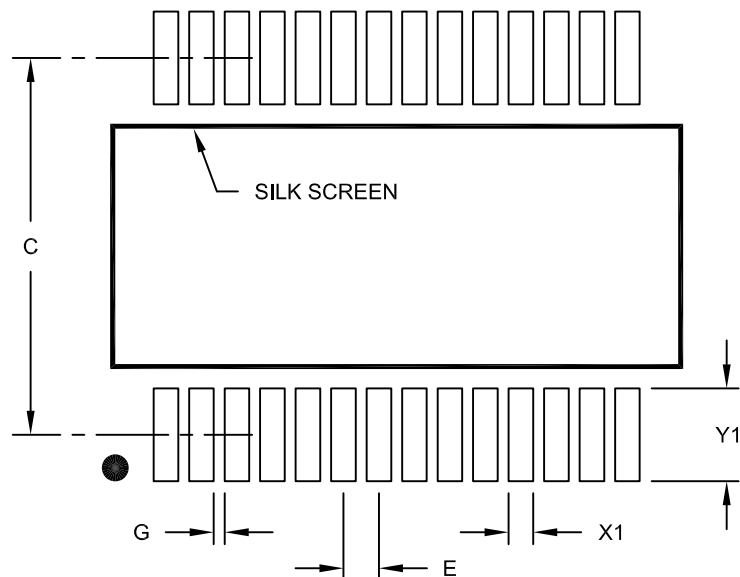
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

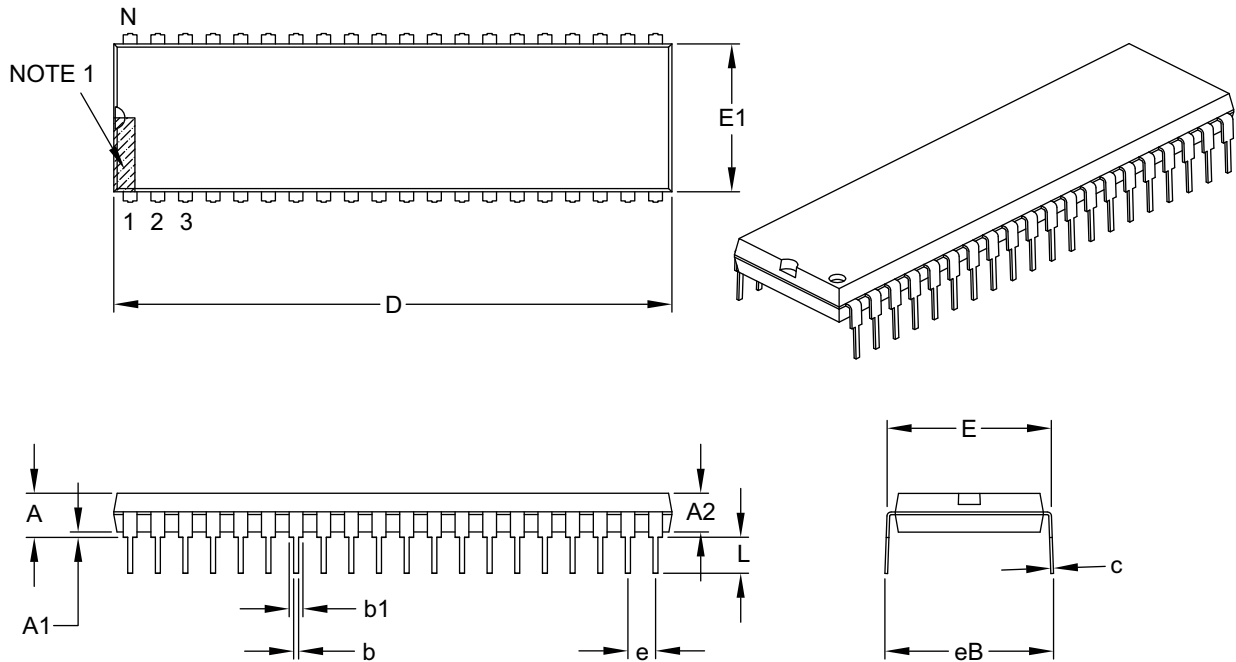
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

40-Lead Plastic Dual In-Line (P) – 600 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	40		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.250
Molded Package Thickness	A2	.125	–	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.590	–	.625
Molded Package Width	E1	.485	–	.580
Overall Length	D	1.980	–	2.095
Tip to Seating Plane	L	.115	–	.200
Lead Thickness	c	.008	–	.015
Upper Lead Width	b1	.030	–	.070
Lower Lead Width	b	.014	–	.023
Overall Row Spacing §	eB	–	–	.700

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-016B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>[X]⁽¹⁾</u>	<u>-</u>	<u>X</u>	<u>/XX</u>	<u>XXX</u>
Device	Tape and Reel Option		Temperature Range	Package	Pattern
<div> <div> Device: PIC16F1777, PIC16LF1777, PIC16F1778, PIC16LF1778, PIC16F1779, PIC16F1779 </div> <div> Tape and Reel Option: Blank = Standard packaging (tube or tray) T = Tape and Reel⁽¹⁾ </div> <div> Temperature Range: I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended) </div> <div> Package:⁽²⁾ MV = UQFN, 40-pin 5x5x0.5 mm MX = UQFN, 28-pin 6x6x0.5 mm P = PDIP, 40-pin PT = TQFN, 44-pin 10x10 mm ML = QFN, 44-pin 8x8 mm SO = SOIC, 28-pin SP = SPDIP, 28-pin SS = SSOP, 28-pin </div> <div> Pattern: QTP, SQTP, Code or Special Requirements (blank otherwise) </div> </div>					
Examples: a) PIC16LF1777-I/P Industrial temperature PDIP package b) PIC16F1779-E/SS Extended temperature SSOP package					
Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option. 2: Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.					