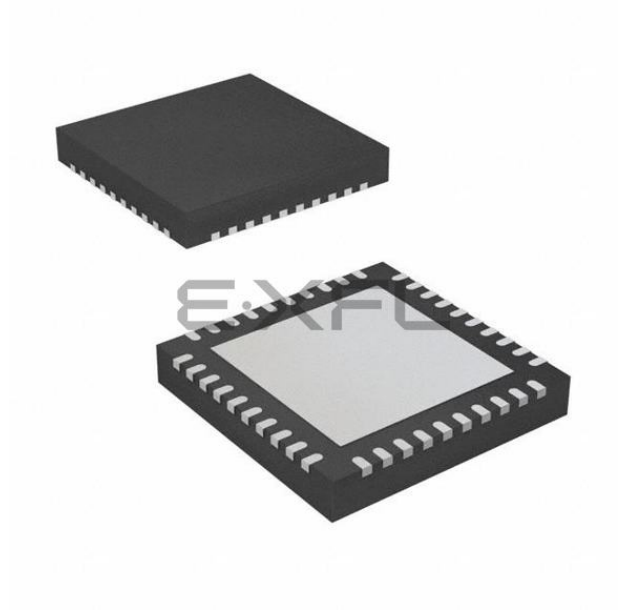

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x10b; D/A 4x5b, 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1777-i-mv

TABLE 1-4: PERIPHERAL CONNECTION MATRIX

	Peripheral Input																							
Peripheral Output	**ADC Trigger**	**COG Clock**	**COG Rising/Falling**	**COG Shutdown**	**10-bit DAC**	**5-bit DAC**	**PRG Analog Input**	**PRG Rising/Falling**	**Comparator +**	**Comparator -**	**CLC**	**DSM CH**	**DSM CL**	**DSM Mod**	**Op Amp +**	**Op Amp -**	**Op Amp Override**	**10-bit PWM**	**16-bit PWM**	**CCP Capture**	**CCP Clock**	**Timer2/4/6/8 Clock**	**Timer2/4/6/8 Reset**	**Timer1/3/5 Gate**	**Timer0 Clock**
FVR					●	●	●		●	●					●	●									
ZCD											●						●					●			
PRG									●						●	●									
10-bit DAC							●		●						●	●									
5-bit DAC							●		●						●	●									
CCP	●		●					●			●	●	●	●			●						●		
Comparator (sync)	●							●			●						●			●			●	●	
Comparator (async)			●	●										●											
CLC	●		●	●							●	●	●	●			●			●		●	●		
DSM																									
COG																	●								
EUSART TX/CK											●			●											
EUSART DT											●			●											
MSSP SCK/SCL											●			●											
MSSP SDO/SDA											●			●											
Op Amp							●																		
10-bit PWM	●		●					●			●	●	●	●			●						●		
16-bit PWM	●		●					●			●	●	●	●			●						●		
Timer0 overflow	●										●													●	
Timer2 = T2PR				●							●							●			●		●		
Timer4 = T4PR				●							●							●			●		●		
Timer6 = T6PR				●							●							●			●		●		
Timer8 = T8PR				●							●							●			●		●		
Timer2 Postscale	●			●							●							●			●		●		
Timer4 Postscale	●			●							●							●			●		●		
Timer6 Postscale	●			●							●							●			●		●		
Timer8 Postscale	●			●							●							●			●		●		
Timer1 overflow	●										●							●			●				
Timer3 overflow	●										●							●			●				
Timer5 overflow	●										●							●			●				
SOSC																			●			●			
FOSC/4		●																				●			
FOSC		●									●	●	●						●			●			
HFINTOSC		●									●	●	●						●			●			
LFINTOSC											●								●			●			
MFINTOSC																						●			
IOCIF											●									●	●				
PPS Input pin			●	●				●				●	●	●						●	●	●	●	●	●

3.4.5 CORE FUNCTION REGISTERS SUMMARY

The Core Function registers listed in Table 3-17 can be addressed from any Bank.

TABLE 3-17: CORE FUNCTION REGISTERS SUMMARY(1)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 0-31											
x00h or x80h	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
x01h or x81h	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
x02h or x82h	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
x03h or x83h	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
x04h or x84h	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
x05h or x85h	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
x06h or x86h	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
x07h or x87h	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
x08h or x88h	BSR	—	—	—	BSR4	BSR3	BSR2	BSR1	BSR0	---0 0000	---0 0000
x09h or x89h	WREG	Working Register								0000 0000	uuuu uuuu
x0Ah or x8Ah	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
x0Bh or x8Bh	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 27 (Continued)											
DC1h	PWM12PHL(3)	PH<7:0>								xxxx xxxx	uuuu uuuu
DC2h	PWM12PHH(3)	PH<15:8>								xxxx xxxx	uuuu uuuu
DC3h	PWM12DCL(3)	DC<7:0>								xxxx xxxx	uuuu uuuu
DC4h	PWM12DCH(3)	DC<15:8>								xxxx xxxx	uuuu uuuu
DC5h	PWM12PRL(3)	PR<7:0>								xxxx xxxx	uuuu uuuu
DC6h	PWM12PRH(3)	PR<15:8>								xxxx xxxx	uuuu uuuu
DC7h	PWM12OFL(3)	OF<7:0>								xxxx xxxx	uuuu uuuu
DC8h	PWM12OFH(3)	OF<15:8>								xxxx xxxx	uuuu uuuu
DC9h	PWM12TMRL(3)	TMR<7:0>								0000 0000	0000 0000
DCAh	PWM12TMRH(3)	TMR<15:8>								0000 0000	0000 0000
DCBh	PWM12CON(3)	EN	—	OUT	POL	MODE<1:0>		—	—	0-00 00--	0-00 00--
DCCh	PWM12INTE(3)	—	—	—	—	OFIE	PHIE	DCIE	PRIE	---- 0000	---- 0000
DCDh	PWM12INTF(3)	—	—	—	—	OFIF	PHIF	DCIF	PRIF	---- 0000	---- 0000
DCEh	PWM12CLKCON(3)	—	PS<2:0>			—	—	CS<1:0>		-000 --00	-000 --00
DCFh	PWM12LDCON(3)	LDA	LDT	—	—	—	—	LDS<1:0>		00-- --00	00-- --00
DD0h	PWM12OFCON(3)	—	OFM<1:0>		OFO	—	—	OFS<1:0>		-000 --00	-000 --00
DD1h to DEFh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

REGISTER 4-1: CONFIG1: CONFIGURATION WORD 1 (CONTINUED)

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits

111 =	ECH	External Clock, High-Power mode: CLKIN supplied to OSC1/CLKIN pin
110 =	ECM	External Clock, Medium Power mode: CLKIN supplied to OSC1/CLKIN pin
101 =	ECL	External Clock, Low-Power mode: CLKIN supplied to OSC1/CLKIN pin
100 =	INTOSC	Internal HFINTOSC. I/O function on CLKIN pin
011 =	EXTRC	External RC circuit connected to CLKIN pin
010 =	HS	High-speed crystal/resonator connected between OSC1 and OSC2 pins
001 =	XT	Crystal/resonator connected between OSC1 and OSC2 pins
000 =	LP	Low-power crystal connected between OSC1 and OSC2 pins

Note 1: The entire Flash program memory will be erased when the code protection is turned off during an erase. When a Bulk Erase Program Memory command is executed, the entire program Flash memory and configuration memory will be erased.

5.2.2.5 Internal Oscillator Frequency Selection

The system clock speed can be selected via software using the Internal Oscillator Frequency Select bits IRCF<3:0> of the OSCCON register.

The postscaled output of the 16 MHz HFINTOSC, 500 kHz MFINTOSC, and 31 kHz LFINTOSC connect to a multiplexer (see Figure 5-1). The Internal Oscillator Frequency Select bits IRCF<3:0> of the OSCCON register select the frequency output of the internal oscillators. One of the following frequencies can be selected via software:

- 32 MHz (requires 4x PLL)
- 16 MHz
- 8 MHz
- 4 MHz
- 2 MHz
- 1 MHz
- 500 kHz (default after Reset)
- 250 kHz
- 125 kHz
- 62.5 kHz
- 31.25 kHz
- 31 kHz (LFINTOSC)

Note:	Following any Reset, the IRCF<3:0> bits of the OSCCON register are set to '0111' and the frequency selection is set to 500 kHz. The user can modify the IRCF bits to select a different frequency.

The IRCF<3:0> bits of the OSCCON register allow duplicate selections for some frequencies. These duplicate choices can offer system design trade-offs. Lower power consumption can be obtained when changing oscillator sources for a given frequency. Faster transition times can be obtained between frequency changes that use the same oscillator source.

5.2.2.6 32 MHz Internal Oscillator Frequency Selection

The Internal Oscillator Block can be used with the 4x PLL associated with the External Oscillator Block to produce a 32 MHz internal system clock source. The following settings are required to use the 32 MHz internal clock source:

- The FOSC bits in Configuration Words must be set to use the INTOSC source as the device system clock (FOSC<2:0> = 100).
- The SCS bits in the OSCCON register must be cleared to use the clock determined by FOSC<2:0> in Configuration Words (SCS<1:0> = 00).
- The IRCF bits in the OSCCON register must be set to the 8 MHz HFINTOSC set to use (IRCF<3:0> = 1110).
- The SPLLEN bit in the OSCCON register must be set to enable the 4x PLL, or the PLLEN bit of the Configuration Words must be programmed to a '1'.

Note:	When using the PLLEN bit of the Configuration Words, the 4x PLL cannot be disabled by software and the SPLLEN option will not be available.

The 4x PLL is not available for use with the internal oscillator when the SCS bits of the OSCCON register are set to '1x'. The SCS bits must be set to '00' to use the 4x PLL with the internal oscillator.

REGISTER 5-2: OSCSTAT: OSCILLATOR STATUS REGISTER

R-1/q	R-0/q	R-q/q	R-0/q	R-0/q	R-q/q	R-0/0	R-0/q
SOSCR	PLLR	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Conditional

bit 7 **SOSCR:** Secondary Oscillator Ready bit
If T1OSCEN = 1:
1 = Secondary oscillator is ready
0 = Secondary oscillator is not ready
If T1OSCEN = 0:
1 = Secondary clock source is always ready

bit 6 **PLLR** 4x PLL Ready bit
1 = 4x PLL is ready
0 = 4x PLL is not ready

bit 5 **OSTS:** Oscillator Start-up Timer Status bit
1 = Running from the clock defined by the FOSC<2:0> bits of the Configuration Words
0 = Running from an internal oscillator (FOSC<2:0> = 100)

bit 4 **HFIOFR:** High-Frequency Internal Oscillator Ready bit
1 = HFINTOSC is ready
0 = HFINTOSC is not ready

bit 3 **HFIOFL:** High-Frequency Internal Oscillator Locked bit
1 = HFINTOSC is at least 2% accurate
0 = HFINTOSC is not 2% accurate

bit 2 **MFIOFR:** Medium-Frequency Internal Oscillator Ready bit
1 = MFINTOSC is ready
0 = MFINTOSC is not ready

bit 1 **LFIOFR:** Low-Frequency Internal Oscillator Ready bit
1 = LFINTOSC is ready
0 = LFINTOSC is not ready

bit 0 **HFIOFS:** High-Frequency Internal Oscillator Stable bit
1 = HFINTOSC is at least 0.5% accurate
0 = HFINTOSC is not 0.5% accurate

16.3 Register Definitions: ADC Control

REGISTER 16-1: ADCON0: ADC CONTROL REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
CHS<5:0>						GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-2 **CHS<5:0>:** Analog Channel Select bits

111111 = FVR (Fixed Voltage Reference) Buffer 1 Output(2)
111110 = DAC1_output(1)
111101 = Temperature Indicator(3)
111100 = DAC2_output(1)
111011 = DAC3_output(4)
111010 = DAC4_output(4)
111001 = DAC5_output(4)
111000 = DAC6_output(4,6)
110111 = DAC7_output(4)
110110 = DAC8_output(1,6)
110101 = Reserved. No channel connected.
110010 = Switched AN18(5)
110001 = Reserved. No channel connected.
•
•
•
101011 = Reserved. No channel connected.
101010 = Switched AN10(5)
101001 = Reserved. No channel connected.
•
•
•
100010 = Reserved. No channel connected.
100001 = Switched AN1(5)
011100 = Reserved. No channel connected.
011011 = AN27(6)
011010 = AN26(6)
011001 = AN25(6)
011000 = AN24(6)
010111 = AN23(6)
010110 = AN22(6)
010101 = AN21(6)
010100 = AN20(6)
010011 = AN19
010010 = AN18
010001 = AN17
010000 = AN16
001111 = AN15
001110 = AN14
001101 = AN13
001100 = AN12
001011 = AN11
001010 = AN10
001001 = AN9
001000 = AN8
000111 = AN7(6)
000110 = AN6(6)
000101 = AN5(6)
000100 = AN4
000011 = AN3
000010 = AN2
000001 = AN1
000000 = AN0

REGISTER 16-1: ADCON0: ADC CONTROL REGISTER 0 (CONTINUED)

bit 1 **GO/$\overline{\text{DONE}}$:** ADC Conversion Status bit
1 = ADC conversion cycle in progress. Setting this bit starts an ADC conversion cycle.
This bit is automatically cleared by hardware when the ADC conversion has completed.
0 = ADC conversion completed/not in progress

bit 0 **ADON:** ADC Enable bit
1 = ADC is enabled
0 = ADC is disabled and consumes no operating current

Note 1: See **Section 17.0 "5-Bit Digital-to-Analog Converter (DAC) Module"** for more information.
2: See **Section 14.0 "Fixed Voltage Reference (FVR)"** for more information.
3: See **Section 15.0 "Temperature Indicator Module"** for more information.
4: See **Section 18.0 "10-bit Digital-to-Analog Converter (DAC) Module"** for more information.
5: Input source is switched off when op amp override is forcing tri-state. See **Section 29.3 "Override Control"**
6: PIC16(L)F1777/9 only.

TABLE 22-6: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	177
CCPxCON	EN	—	OUT	FMT	MODE<3:0>				319
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	132
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	133
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	139
TMRxH	Holding Register for the Most Significant Byte of the 16-bit TMR1/3/5 Register								275*
TMRxL	Holding Register for the Least Significant Byte of the 16-bit TMR1/3/5 Register								275*
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	176
TxCON	CS<1:0>		CKPS<1:0>		OSCEN	$\overline{\text{SYNC}}$	—	ON	283
TxGCON	GE	GPOL	GTM	GSPM	$\overline{\text{GGO}}$/DONE	GVAL	GSS<1:0>		284

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by the Timer1 module.

* Page provides register information.

23.6.9 EDGE-TRIGGERED MONOSTABLE MODES

The Edge-Triggered Monostable modes start the timer on an edge from the external Reset signal input, after the ON bit is set, and stop incrementing the timer when the timer matches the PRx period value. The following edges will start the timer:

- Rising edge (MODE<4:0> = 10001)
- Falling edge (MODE<4:0> = 10010)
- Rising or Falling edge (MODE<4:0> = 10011)

When an Edge-Triggered Monostable mode is used in conjunction with the CCP PWM operation the PWM drive goes active with the external Reset signal edge that starts the timer, but will not go active when the timer matches the PRx value. While the timer is incrementing, additional edges on the external Reset signal will not affect the CCP PWM.

TABLE 24-4: SUMMARY OF REGISTERS ASSOCIATED WITH STANDARD PWM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CCPxCAP	—	—	—	—	CTS<3:0>				321
CCPxCON	EN	—	OUT	FMT	MODE<3:0>				319
CCPRxL	Capture/Compare/PWM Register x (LSB)								320
CCPRxH	Capture/Compare/PWM Register x (MSB)								320
CCPTMRS1	C8TSEL<1:0>(1)		C7TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>		323
CCPTMRS2	P10TSEL<1:0>(1)		P9TSEL<1:0>		P4TSEL<1:0>		P3TSEL<1:0>		323
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	132
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	133
PIE2	OSFIE	C2IE	C1IE	COG1IE	BCL1IE	C4IE	C3IE	CCP2IE	134
PIE5	CCP8IE(1)	CCP7IE	COG4IE(1)	COG3IE	C8IE(1)	C7IE(1)	C6IE	C5IE	137
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	139
PIR2	OSFIF	C2IF	C1IF	COG1IF	BCL1IF	C4IF	C3IF	CCP2IF	140
PIR5	CCP8IF(1)	CCP7IF	COG4IF(1)	COG3IF	C8IF(1)	C7IF(1)	C6IF	C5IF	143
T2PR	Timer2 Period Register								287*
T2CON	ON	CKPS<2:0>			OUTPS<3:0>				307
TMR2	Timer2 Module Register								287
T4PR	Timer4 Period Register								287*
T4CON	ON	CKPS<2:0>			OUTPS<3:0>				307
TMR4	Timer4 Module Register								287
T6PR	Timer6 Period Register								287*
T6CON	ON	CKPS<2:0>			OUTPS<3:0>				307
TMR6	Timer6 Module Register								287
T8PR	Timer8 Period Register								287*
T8CON	ON	CKPS<2:0>			OUTPS<3:0>				307
TMR8	Timer8 Module Register								287

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the PWM.
* Page provides register information.
Note 1: PIC16(L)F1777/9 only.

25.2 Register Definitions: 10-Bit PWM Control

Long bit name prefixes for the DSM peripherals are shown in Table 25-4. Refer to **Section 1.1.2.2 "Long Bit Names"** for more information

TABLE 25-4:

Peripheral	Bit Name Prefix
PWM3	PWM3
PWM4	PWM4
PWM9	PWM9
PWM10(1)	PWM10

Note 1: PIC16(L)F1777/9 only.

REGISTER 25-1: PWMxCON: PWM CONTROL REGISTER

R/W-0/0	U-0	R-0/0	R/W-0/0	U-0	U-0	U-0	U-0
EN	—	OUT	POL	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **EN:** PWM Module Enable bit
1 = PWM module is enabled
0 = PWM module is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **OUT:** PWM module output level when bit is read.

bit 4 **POL:** PWMx Output Polarity Select bit
1 = PWM output is active-low
0 = PWM output is active-high

bit 3-0 **Unimplemented:** Read as '0'

REGISTER 26-5: PWMxLDCON: PWM RELOAD TRIGGER SOURCE SELECT REGISTER

R/W/HC-0/0	R/W-0/0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
LDA(1)	LDT	—	—	—	—	LDS<1:0>(2)	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Cleared by hardware

bit 7 **LDA:** Load Buffer Armed bit(1)
If LDT = 1:
1 = Load the ODO bit and OFx, PHx, DCx and PRx buffers at the end of the period in which the selected trigger occurs
0 = Do not load buffers, load has completed
If LDT = 0:
1 = Load the ODO bit and OFx, PHx, DCx and PRx buffers at the end of the current period
0 = Do not load buffers, load has completed

bit 6 **LDT:** Load Buffer on Trigger bit
1 = Wait for trigger selected by the LDS<1:0> bits to occur before enabling the LDA bit
0 = Load triggering is disabled. Buffer loads are controlled by the LDA bit alone.

bit 5-2 **Unimplemented:** Read as '0'

bit 1-0 **LDS<1:0>:** Load Trigger Source Select bits(2)
10 = LD11_trigger
01 = LD6_trigger
00 = LD5_trigger

Note 1: This bit is cleared by the module after a reload operation. It can be cleared in software to clear an existing arming event.
2: The source corresponding to a PWM module's own LDx_trigger is reserved.

REGISTER 26-15: PWMxTMRH: PWMx TIMER HIGH REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
TMR<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **TMR<15:8>**: PWM Timer High bits
Upper eight bits of PWM timer counter

REGISTER 26-16: PWMxTMRL: PWMx TIMER LOW REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
TMR<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **TMR<7:0>**: PWM Timer Low bits
Lower eight bits of PWM timer counter

FIGURE 27-9: TYPICAL HALF-BRIDGE MODE COG OPERATION WITH CCP1

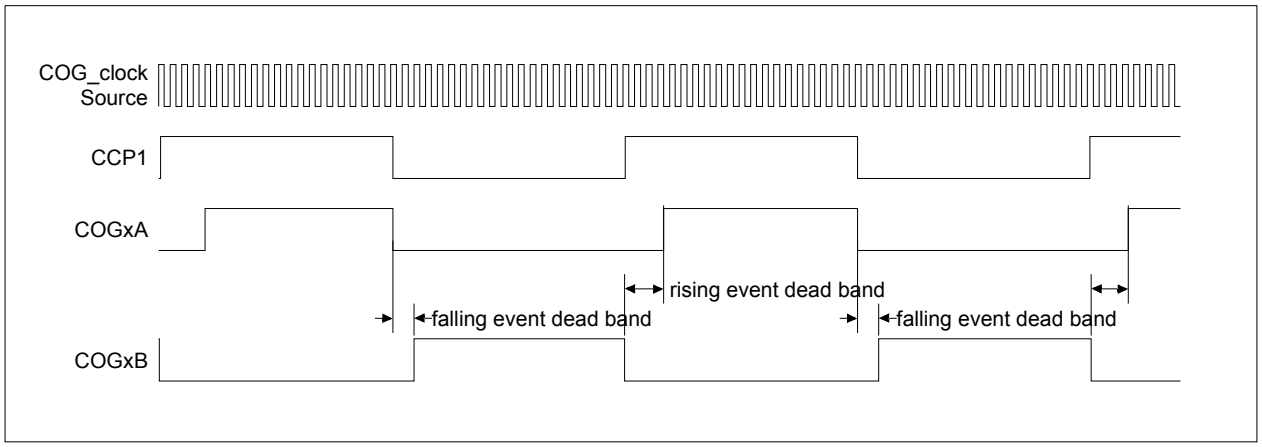

FIGURE 27-10: HALF-BRIDGE MODE COG OPERATION WITH CCP1 AND PHASE DELAY

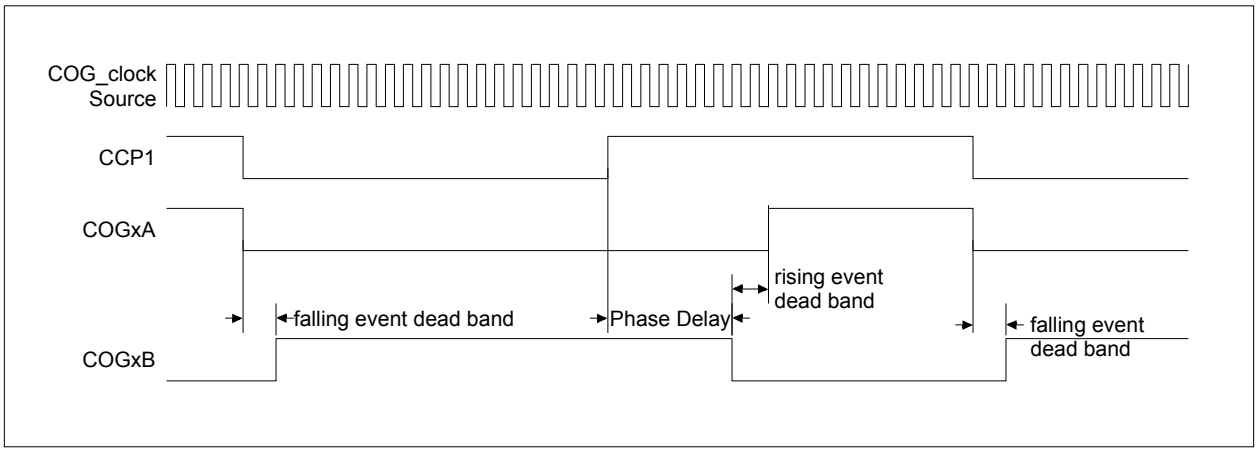

FIGURE 27-11: PUSH-PULL MODE COG OPERATION WITH CCP1

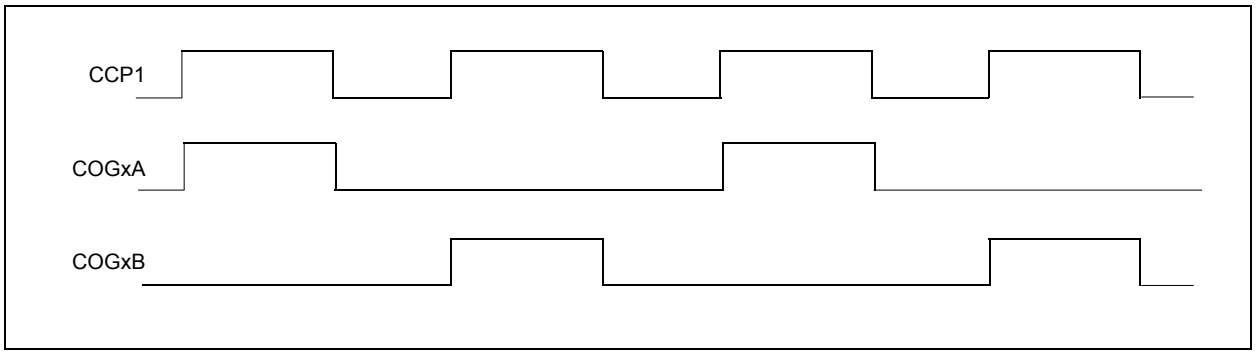

TABLE 27-7: SUMMARY OF REGISTERS ASSOCIATED WITH COGx(1)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	177
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	182
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—	187
COGxASD0	ASE	ARSEN	ASDBD<1:0>		ASDAC<1:0>		—	—	384
COGxASD1	AS7E	AS6E	AS5E	AS4E	AS3E	AS2E	AS1E	AS0E	385
COGxBLKR	—	—	BLKR<5:0>						388
COGxBLKF	—	—	BLKF<5:0>						388
COGxCON0	EN	LD	—	CS<1:0>		MD<2:0>			378
COGxCON1	RDBS	FDBS	—	—	POLD	POLC	POLB	POLA	379
COGxDBR	—	—	DBR<5:0>						387
COGxDBF	—	—	DBF<5:0>						387
COGxFIS0	FIS7	FIS6	FIS5	FIS4	FIS3	FIS2	FIS1	FIS0	382
COGxFIS1	FIS15	FIS14	FIS13	FIS12	FIS11	FIS10	FIS9	FIS8	382
COGxFSIM0	FSIM7	FSIM6	FSIM5	FSIM4	FSIM3	FSIM2	FSIM1	FSIM0	383
COGxFSIM1	FSIM15	FSIM14	FSIM13	FSIM12	FSIM11	FSIM10	FSIM9	FSIM8	383
COGxPHR	—	—	PHR<5:0>						389
COGxPHF	—	—	PHF<5:0>						389
COGxPPS	—	—	COG1PPS<5:0>						205, 207
COGxRIS0	RIS7	RIS6	RIS5	RIS4	RIS3	RIS2	RIS1	RIS0	380
COGxRIS1	RIS15	RIS14	RIS13	RIS12	RIS11	RIS10	RIS9	RIS8	380
COGxRSIM0	RSIM7	RSIM6	RSIM5	RSIM4	RSIM3	RSIM2	RSIM1	RSIM0	381
COGxRSIM1	RSIM15	RSIM14	RSIM13	RSIM12	RSIM11	RSIM10	RSIM9	RSIM8	381
COGxSTR	SDATD	SDATC	SDATB	SDATA	STRD	STRC	STRB	STRA	386
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	132
RxyPPS	—	—	RxyPPS<5:0>						205

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by COG.

Note 1: COG4 is available on PIC16(L)F1777/9 only.

The MSSP consists of a transmit/receive shift register (SSPSR) and a buffer register (SSPxBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPxBUF holds the data that was written to the SSPSR until the received data is ready. Once the eight bits of data have been received, that byte is moved to the SSPxBUF register. Then, the Buffer Full Detect bit, BF of the SSPxSTAT register, and the interrupt flag bit, SSPxIF, are set. This double-buffering of the received data (SSPxBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPxBUF register during transmission/reception of data will be ignored and the Write Collision Detect bit WCOL of the SSPxCON1 register, will be set. User software must clear the WCOL bit to allow the following write(s) to the SSPxBUF register to complete successfully.

When the application software is expecting to receive valid data, the SSPxBUF should be read before the next byte of data to transfer is written to the SSPxBUF. The Buffer Full bit, BF of the SSPxSTAT register, indicates when SSPxBUF has been loaded with the received data (transmission is complete). When the SSPxBUF is read, the BF bit is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally, the MSSP interrupt is used to determine when the transmission/reception has completed. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur.

The SSPSR is not directly readable or writable and can only be accessed by addressing the SSPxBUF register. Additionally, the SSPxSTAT register indicates the various Status conditions.

FIGURE 32-5: SPI MASTER/SLAVE CONNECTION

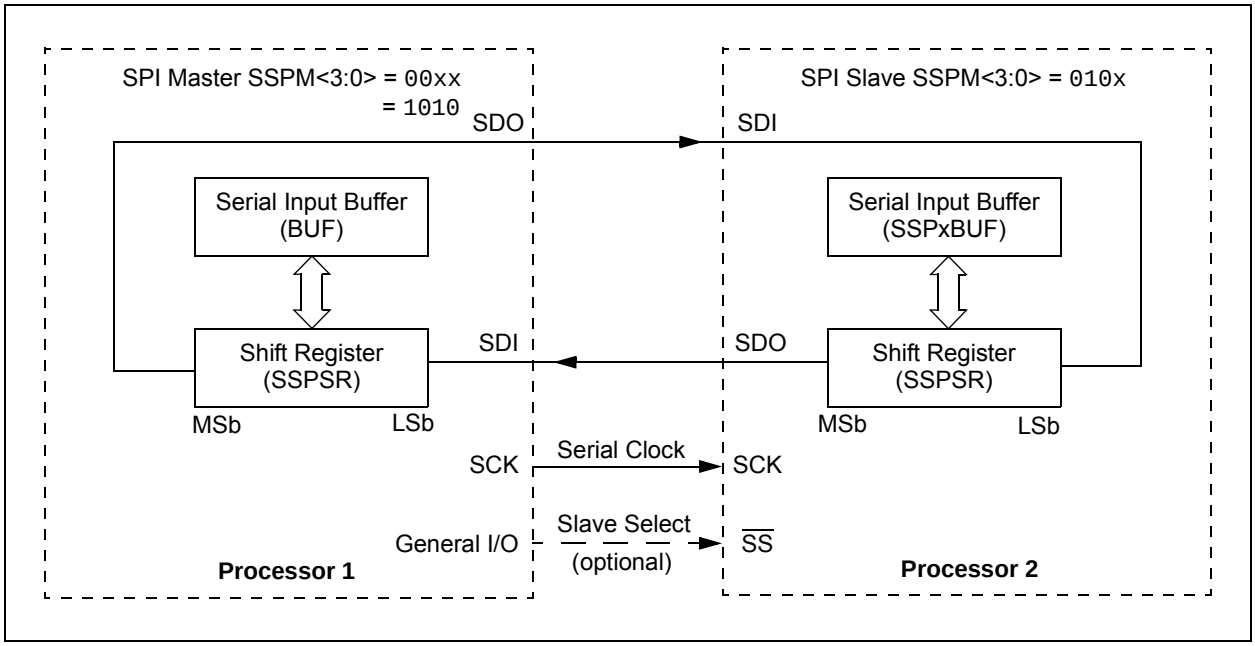

TABLE 36-27: I^2C BUS DATA REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Symbol**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
SP100*	THIGH	Clock high time	100 kHz mode	4.0	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Device must operate at a minimum of 10 MHz
			SSP module	1.5TCY	—		
SP101*	TLOW	Clock low time	100 kHz mode	4.7	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	μs	Device must operate at a minimum of 10 MHz
			SSP module	1.5TCY	—		
SP102*	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1CB	300	ns	CB is specified to be from 10-400 pF
SP103*	TF	SDA and SCL fall time	100 kHz mode	—	250	ns	
			400 kHz mode	20 + 0.1CB	250	ns	CB is specified to be from 10-400 pF
SP106*	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
SP107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	**(Note 2)**
			400 kHz mode	100	—	ns	
SP109*	TAA	Output valid from clock	100 kHz mode	—	3500	ns	**(Note 1)**
			400 kHz mode	—	—	ns	
SP110*	TBUF	Bus free time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
SP111	CB	Bus capacitive loading		—	400	pF	

* These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

2: A Fast mode (400 kHz) I^2C bus device can be used in a Standard mode (100 kHz) I^2C bus system, but the requirement $T_{SU:DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line T_R max. + $T_{SU:DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification), before the SCL line is released.

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

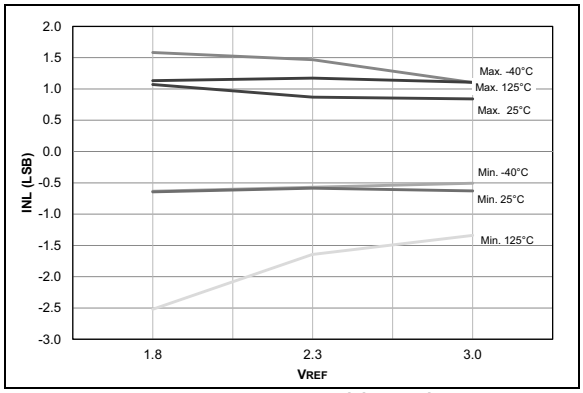

FIGURE 37-85: *ADC 10-bit Mode, Single-Ended INL, VDD = 3.0V, TAD = 1 µS.*

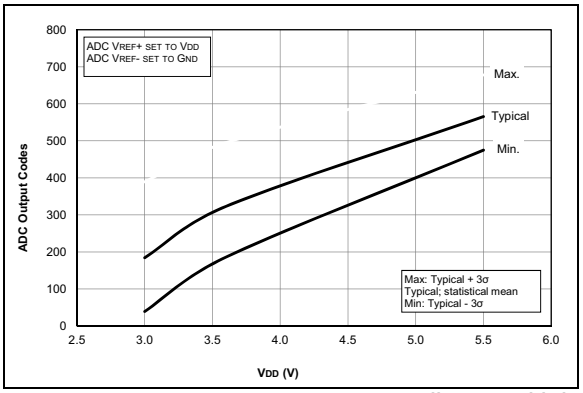

FIGURE 37-86: *Temperature Indicator Initial Offset, High Range, Temp. = 20°C, PIC16F1777/8/9 only.*

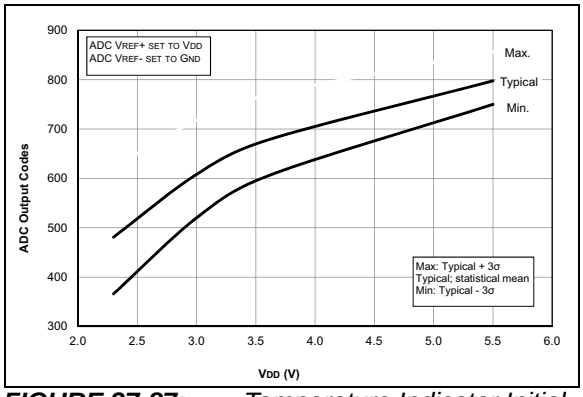

FIGURE 37-87: *Temperature Indicator Initial Offset, Low Range, Temp. = 20°C, PIC16F1777/8/9 only.*

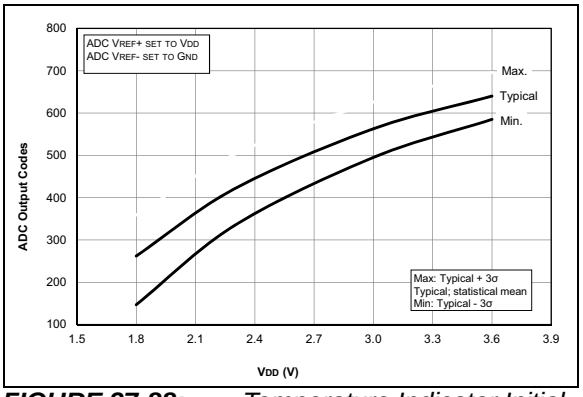

FIGURE 37-88: *Temperature Indicator Initial Offset, Low Range, Temp. = 20°C, PIC16LF1773/6 only.*

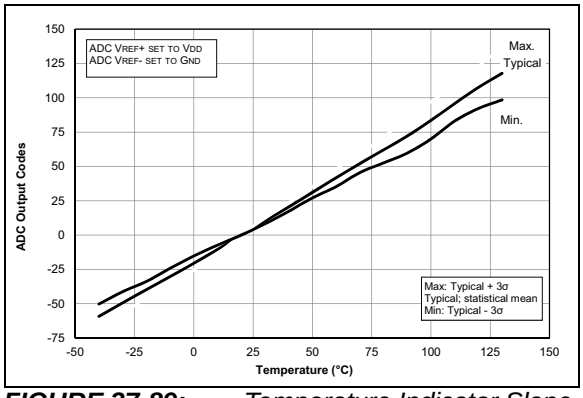

FIGURE 37-89: *Temperature Indicator Slope Normalized to 20°C, PIC16F1777/8/9 only.*

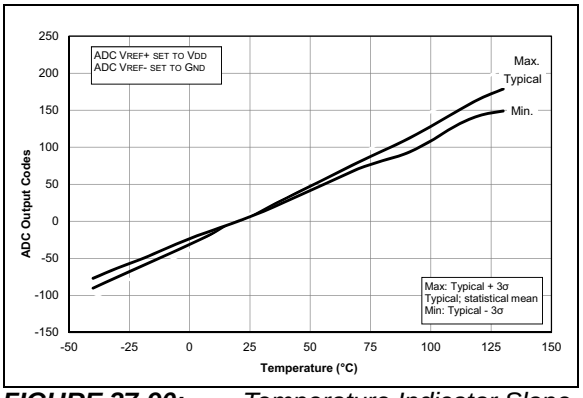

FIGURE 37-90: *Temperature Indicator Slope Normalized to 20°C, High Range, VDD = 3.6V, PIC16F1777/8/9 only.*

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

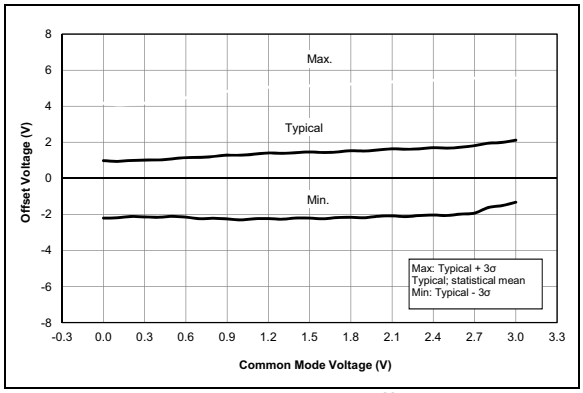

FIGURE 37-97: *Op Amp, Offset over Common Mode Voltage, V_{DD} = 3.0V, Temp. = 25°C*

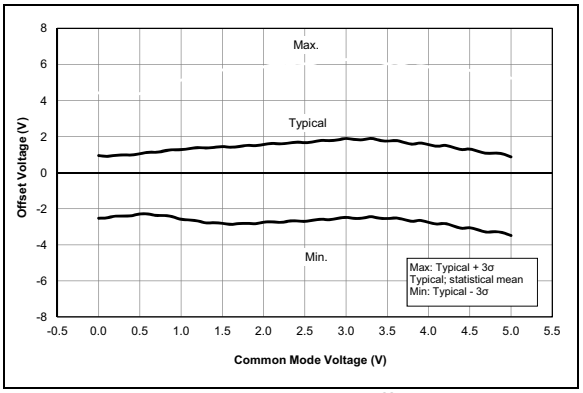

FIGURE 37-98: *Op Amp, Offset over Common Mode Voltage, V_{DD} = 5.0V, Temp. = 25°C, PIC16F1777/8/9 Only.*

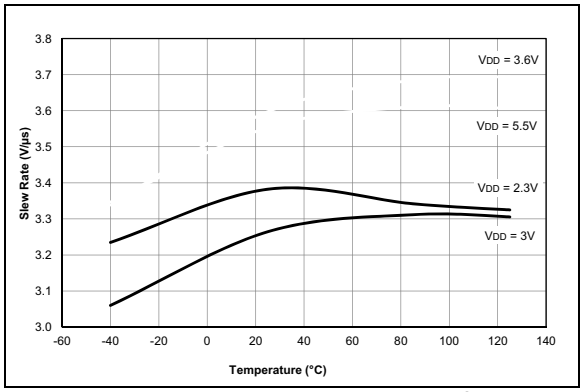

FIGURE 37-99: *Op Amp, Output Slew Rate, Rising Edge, PIC16F1777/8/9 Only.*

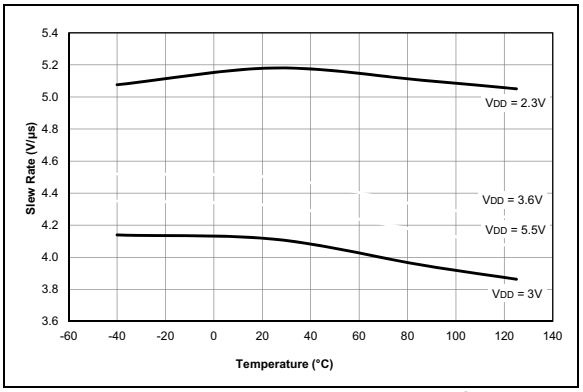

FIGURE 37-100: *Op Amp, Output Slew Rate, Falling Edge, PIC16F1777/8/9 Only.*

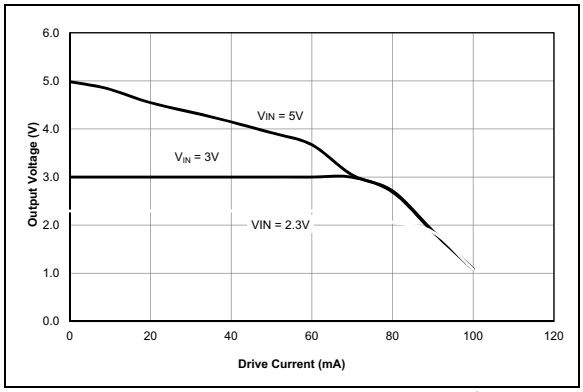

FIGURE 37-101: *Op Amp, Output Drive Strength, V_{DD} = 5.0V, Temp. = 25°C, PIC16F1777/8/9 Only.*

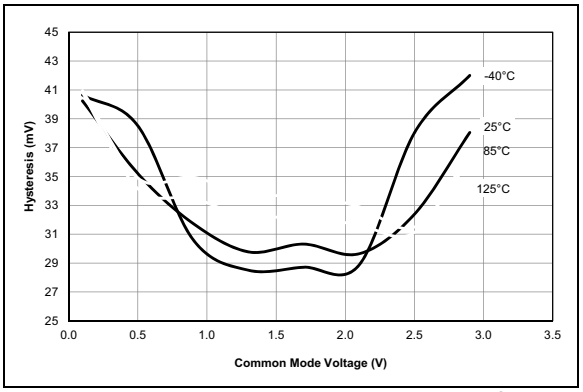

FIGURE 37-102: *Comparator Hysteresis, NP Mode (CxSP = 1), V_{DD} = 3.0V, Typical Measured Values.*