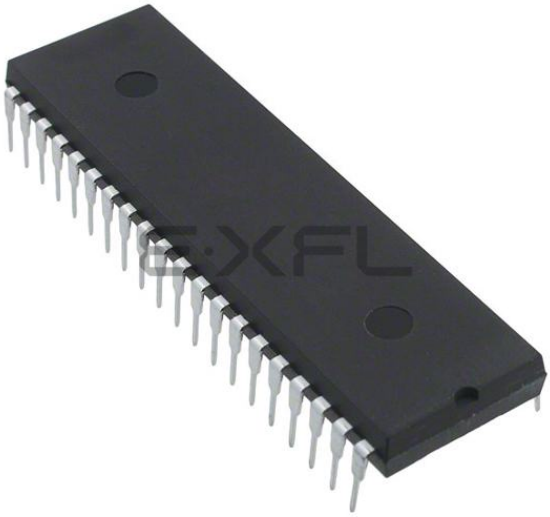

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Applications of "Embedded - Microcontrollers"

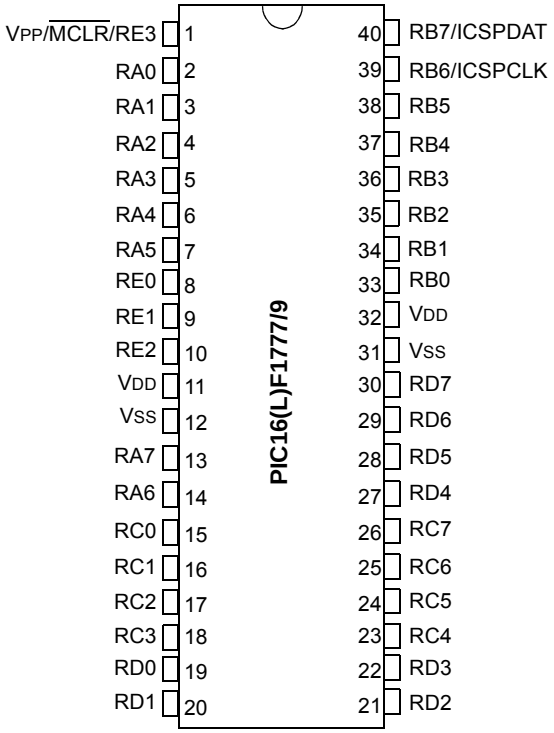
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x10b; D/A 4x5b, 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1777-i-p

TABLE 2: PACKAGES

Packages	SPDIP	PDIP	SOIC	SSOP	UQFN	QFN	TQFP
PIC16(L)F1778	●		●	●	●		
PIC16(L)F1777/9		●			●	●	●

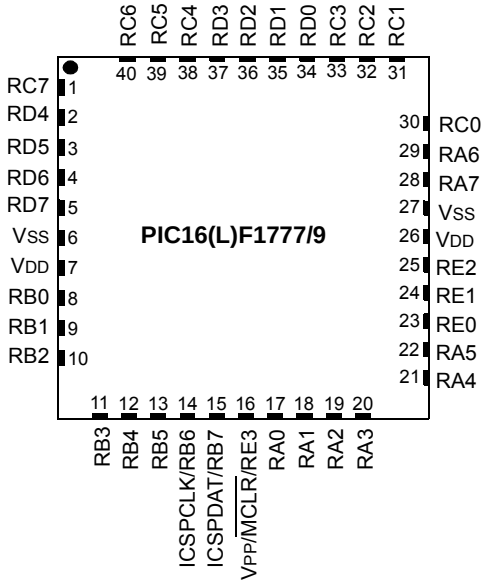
Note: Pin details are subject to change.

FIGURE 3: 40-PIN PDIP



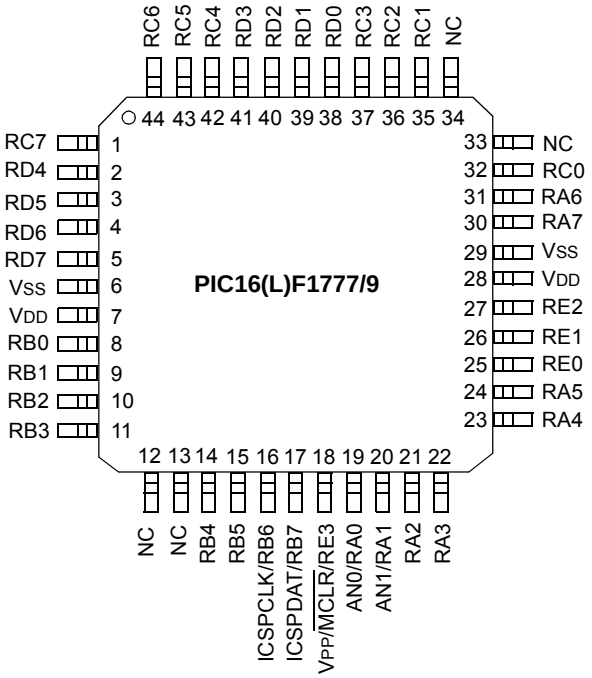
Note: See Table 4 for location of all peripheral functions.

FIGURE 4: 40-PIN UQFN (5x5x0.5 mm)



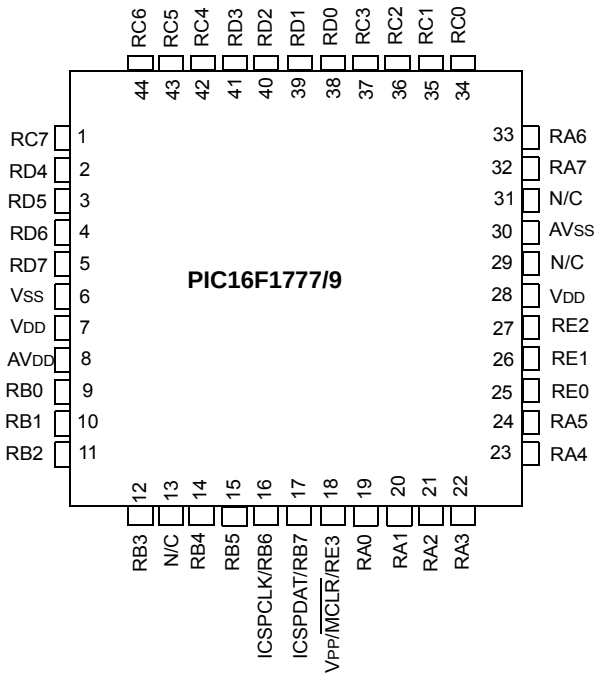
Note: See Table 4 for location of all peripheral functions.

FIGURE 5: 44-PIN TQFP (10x10 mm)



Note: See Table 4 for location of all peripheral functions.

FIGURE 6: 44-PIN QFN (8X8 mm)



Note: See Table 4 for location of all peripheral functions.

TABLE 4: 40/44-PIN ALLOCATION TABLE (PIC16(L)F1777/9)

I/O	40-Pin PDIP	40-Pin (U)QFN	44-Pin TQFP	44-Pin QFN	ADC	VREF	DAC	Op Amp	Comparator	ZCD	PRG	Timers	PWM	CCP	COG	CLC	Modulator	EUSART	MSSP	Interrupt	Pull-ups	High Current	Basic
RA0	2	17	19	19	AN0	—	—	—	C1IN0- C2IN0- C3IN0- C4IN0- C5IN0- C6IN0- C7IN0- C8IN0-	—	—	—	—	—	—	CLCIN0(1)	—	—	—	IOC	Y	—	—
RA1	3	18	20	20	AN1	—	—	OPA1OUT OPA2IN1+ OPA2IN1-	C1IN1- C2IN1- C3IN1- C4IN1-	—	PRG1IN0 PRG2IN1	—	—	—	—	CLCIN1(1)	—	—	—	IOC	Y	—	—
RA2	4	19	21	21	AN2	DAC1REF0- DAC2REF0- DAC3REF0- DAC4REF0- DAC5REF0- DAC6REF0- DAC7REF0- DAC8REF0-	DAC1OUT1	—	C1IN0+ C2IN0+ C3IN0+ C4IN0+ C5IN0+ C6IN0+ C7IN0+ C8IN0+	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	—
RA3	5	20	22	22	AN3	DAC1REF0+ DAC2REF0+ DAC3REF0+ DAC4REF0+ DAC5REF0+ DAC6REF0+ DAC7REF0+ DAC8REF0+	—	—	C1IN1+	—	—	—	—	—	—	—	MD1CL(1)	—	—	IOC	Y	—	—
RA4	6	21	23	23	—	—	—	OPA1IN0+	—	—	PRG1R(1)	—	—	—	—	—	MD1CH(1)	—	—	IOC	Y	—	—
RA5	7	22	24	24	AN4	—	DAC2OUT1	OPA1IN0-	—	—	PRG1F(1)	—	—	—	—	—	MD1MOD(1)	—	$\overline{SS}$	IOC	Y	—	—
RA6	14	29	31	33	—	—	—	—	C6IN1+	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	OSC2 CLKOUT
RA7	13	28	30	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	OSC1 CLKIN
RB0	33	8	8	9	AN12	—	—	—	C2IN1+	ZCD	—	—	—	CCP8(1)	COG1IN(1)	—	MD4CL(1)	—	—	IOC INT	Y	HIB0	—
RB1	34	9	9	10	AN10	—	—	OPA2OUT OPA1IN1+ OPA1IN1-	C1IN3- C2IN3- C3IN3- C4IN3-	—	PRG2IN0 PRG1IN1 PRG4R(1)	—	—	—	COG2IN(1)	—	MD4CH(1)	—	—	IOC	Y	HIB1	—
RB2	35	10	10	11	AN8	—	DAC3OUT1	OPA2IN0-	—	—	PRG4F(1)	—	—	—	COG3IN(1)	—	MD4MOD(1)	—	—	IOC	Y	—	—
RB3	36	11	11	12	AN9	—	—	OPA2IN0+	C1IN2- C2IN2- C3IN2-	—	—	—	—	—	—	—	MD3CL(1)	—	—	IOC	Y	—	—
RB4	37	12	14	14	AN11	—	—	—	C3IN1+	—	—	—	—	—	—	—	MD3CH(1)	—	—	IOC	Y	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection register.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F1778 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB6/DAC5REF1+/DAC7REF1+/ C4IN1+/CLCIN2/ICSPCLK	RB6	TTL/ST	CMOS	General purpose I/O.
	DAC5REF1+	AN	—	DAC5 positive reference.
	DAC7REF1+	AN	—	DAC7 positive reference.
	C4IN1+	AN	—	Comparator 2 positive input.
	CLCIN2(1)	TTL/ST	—	CLC input 2.
	ICSPCLK	ST	—	Serial Programming Clock.
RB7/C5IN1+/DAC1OUT2/ DAC2OUT2/DAC3OUT2/ DAC4OUT2/DAC5OUT2/ DAC7OUT2/T6IN/CLCIN3/ ICSPDAT	RB7	TTL/ST	CMOS	General purpose I/O.
	C5IN1+	AN	—	Comparator 5 positive input.
	DAC1OUT2	—	AN	DAC1 voltage output.
	DAC2OUT2	—	AN	DAC2 voltage output.
	DAC3OUT2	—	AN	DAC3 voltage output.
	DAC4OUT2	—	AN	DAC4 voltage output.
	DAC5OUT2	—	AN	DAC5 voltage output.
	DAC7OUT2	—	AN	DAC7 voltage output.
	T6IN(1)	TTL/ST	—	Timer6 gate input.
	CLCIN3(1)	TTL/ST	—	CLC input 3.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RC0/DAC5OUT1/T1CKI/T3CKI/ T3G/SOSCO	RC0	TTL/ST	CMOS	General purpose I/O.
	DAC5OUT1	—	AN	DAC5 voltage output.
	T1CKI(1)	AN	—	Comparator 4 negative input.
	T3CKI(1)	TTL/ST	—	Timer3 clock input.
	T3G(1)	TTL/ST	—	Timer3 gate input.
	SOSCO	—	XTAL	Secondary oscillator output.
RC1/DAC7OUT1/PRG2R/CCP2/ SOSCI	RC1	TTL/ST	CMOS	General purpose I/O.
	DAC7OUT1	—	AN	DAC7 voltage output.
	PRG2R(1)	TTL/ST	—	Ramp generator set_rising input.
	CCP2(1)	TTL/ST	—	CCP2 capture input.
	SOSCI	XTAL	—	Secondary oscillator input.
RC2/AN14/C5IN2-/C6IN2-/ PRG2F/CCP1/T5CKI	RC2	TTL/ST	CMOS	General purpose I/O.
	AN14	AN	—	ADC Channel 14 input.
	C5IN2-	AN	—	Comparator 5 negative input.
	C6IN2-	AN	—	Comparator 6 negative input.
	PRG2F(1)	TTL/ST	—	Ramp generator set_falling input.
	CCP1(1)	TTL/ST	—	CCP1 capture input.
	T5CKI(1)	TTL/ST	—	Timer5 clock input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HP = High Power XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

REGISTER 7-10: PIR3: PERIPHERAL INTERRUPT REQUEST REGISTER 3

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	COG2IF	ZCDIF	CLC4IF	CLC3IF	CLC2IF	CLC1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **COG2IF:** COG2 Auto-Shutdown Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 4 **ZCDIF:** Zero-Cross Detection Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 3 **CLC4IF:** CLC4 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 2 **CLC3IF:** CLC3 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 1 **CLC2IF:** CLC2 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 0 **CLC1IF:** CLC1 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

TABLE 12-2: AVAILABLE PORTS FOR OUTPUT BY PERIPHERAL(2)

RxyPPS<5:0>	Output Signal	PIC16(L)F1778			PIC16(L)F1777/9				
		A	B	C	A	B	C	D	E
110001	MD4_out(3)				—	●	—	●	
110000	MD3_out		●	●	—	●	—	●	—
101111	MD2_out	●		●	●	—	—	●	—
101110	MD1_out	●		●	●	—	—	●	—
101101	sync_C8OUT(3)				—	●	—	●	—
101100	sync_C7OUT(3)				—	●	—	●	—
101011	sync_C6OUT	●		●	●	—	—	—	●
101010	sync_C5OUT	●		●	●	—	—	●	—
101001	sync_C4OUT		●	●	—	●	—	●	—
101000	sync_C3OUT		●	●	—	●	—	●	—
100111	sync_C2OUT	●		●	●	—	—		●
100110	sync_C1OUT	●		●	●	—	—	●	—
100101	DT		●	●	—	●	●	—	—
100100	TX/CK		●	●	—	●	●	—	—
100011	SDO		●	●	—	●	●	—	—
100010	SDA		●	●	—	●	●	—	—
100001	SCK/SCL(1)		●	●	—	●	●	—	—
100000	PWM12_out(3)				—	●	—	●	—
011111	PWM11_out		●	●	—	●	—	●	—
011110	PWM6_out	●		●	●	—	—	●	—
011101	PWM5_out	●		●	●	—		●	—
011100	PWM10_out(3)				●	—	●	—	—
011011	PWM9_out	●		●	●	—	●		—
011010	PWM4_out	●		●	●	—		●	—
011001	PWM3_out	●		●	●	—		—	●
011000	CCP8_out(3)				—	●	—	●	—
010111	CCP7_out		●	●	—	●	—	●	—
010110	CCP2_out		●	●	—	●	●	—	—
010101	CCP1_out		●	●	—	●	●	—	—
010100	COG4D(1,3)				●	—		●	—
010011	COG4C(1,3)				●	—		●	—
010010	COG4B(1,3)				●	—		—	●
010001	COG4A(1,3)					●	●	—	—
010000	COG3D(1)	●		●	●	—	—	●	—
001111	COG3C(1)	●		●	●	—	—	●	—
001110	COG3B(1)	●		●	●	—	—	—	●
001101	COG3A(1)	●		●	—	●	●	—	—
001100	COG2D(1)		●	●	—	●	—	●	—
001011	COG2C(1)		●	●	—	●	—	●	—
001010	COG2B(1)		●	●		●		●	

Note 1: TRIS control is overridden by the peripheral as required.
2: Unsupported peripherals will output a '0'.
3: PIC16(L)F1777/9 only.

20.0 ZERO-CROSS DETECTION (ZCD) MODULE

The ZCD module detects when an A/C signal crosses through the ground potential. The actual zero-crossing threshold is the zero-crossing reference voltage, ZCPINV, which is typically 0.75V above ground.

The connection to the signal to be detected is through a series current limiting resistor. The module applies a current source or sink to the ZCD pin to maintain a constant voltage on the pin, thereby preventing the pin voltage from forward biasing the ESD protection diodes. When the applied voltage is greater than the reference voltage, the module sinks current. When the applied voltage is less than the reference voltage, the module sources current. The current source and sink action keeps the pin voltage constant over the full range of the applied voltage. The ZCD module is shown in the simplified block diagram Figure 20-2.

The ZCD module is useful when monitoring an AC waveform for, but not limited to, the following purposes:

- A/C period measurement
- Accurate long term time measurement
- Dimmer phase delayed drive
- Low EMI cycle switching

20.1 External Resistor Selection

The ZCD module requires a current limiting resistor in series with the external voltage source. The impedance and rating of this resistor depends on the external source peak voltage. Select a resistor value that will drop all of the peak voltage when the current through the resistor is nominally 300 µA. Refer to Equation 20-1 and Figure 20-1. Make sure that the ZCD I/O pin internal weak pull-up is disabled so it does not interfere with the current source and sink.

EQUATION 20-1: EXTERNAL RESISTOR

$$R_{series} = \frac{V_{peak}}{3\times10^{-4}}$$

FIGURE 20-1: EXTERNAL VOLTAGE

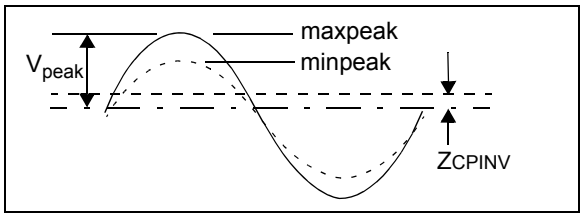
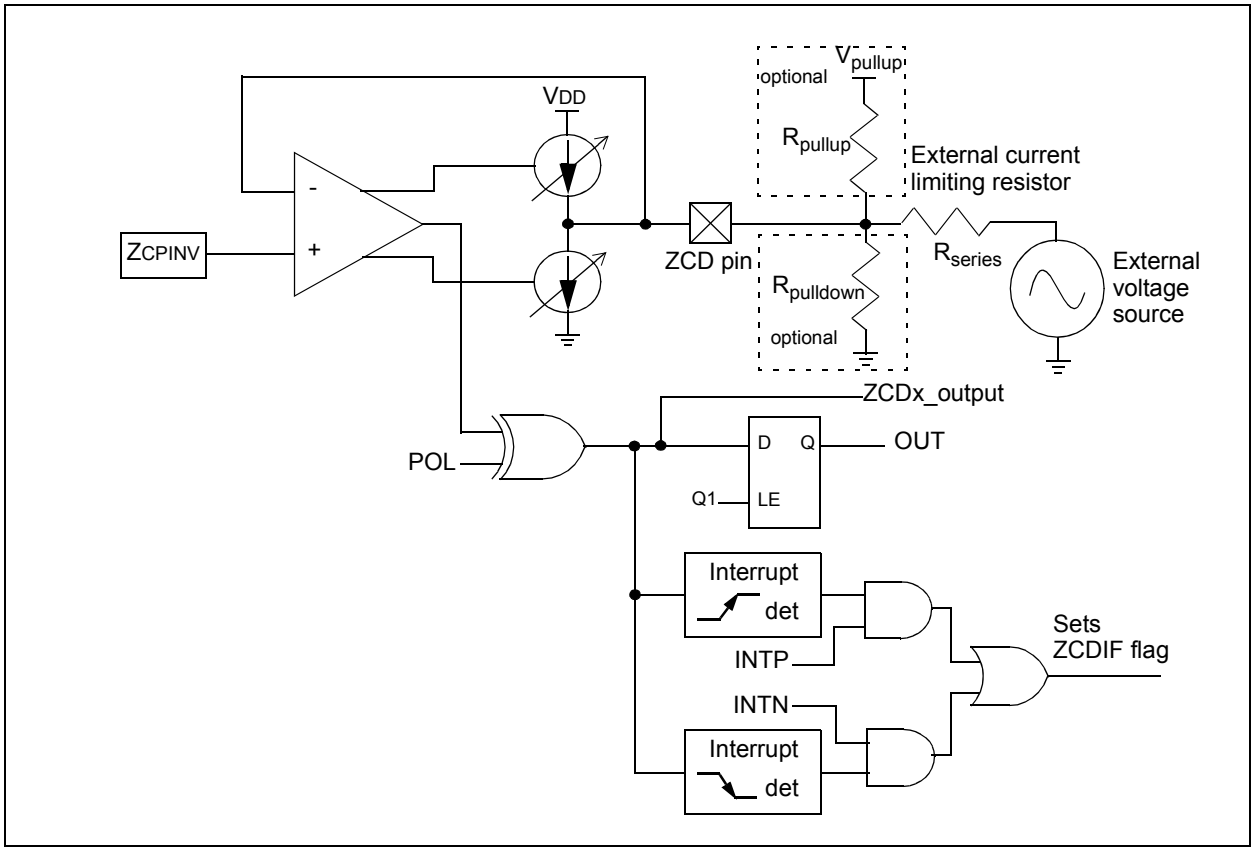


FIGURE 20-2: SIMPLIFIED ZCD BLOCK DIAGRAM



23.7 PR2 Period Register

The PR2 period register (T2PR) is double-buffered. Software reads and writes the PR2 register. However, the timer uses a buffered PR2 register for operation. Software does not have direct access to the buffered PR2 register. The contents of the PR2 register are transferred to the buffer by any of the following events:

- A write to the TMR2 register
- A write to the TMR2CON register
- When TMR2 = PR2 buffer and the prescaler rolls over
- An external Reset event

23.8 Timer2 Operation During Sleep

When PSYNC = 1, Timer2 cannot be operated while the processor is in Sleep mode. The contents of the TMR2 and T2PR registers will remain unchanged while processor is in Sleep mode.

When PSYNC = 0, Timer2 will operate in Sleep as long as the clock source selected is also still running. Selecting the LFINTOSC, MFINTOSC, or HFINTOSC oscillator as the timer clock source will keep the selected oscillator running during Sleep.

24.6 CCP/PWM Clock Selection

This device allows each individual CCP and PWM module to select the timer source that controls the module. Each module has an independent selection.

As there are four 8-bit timers with auto-reload (Timer2, Timer4, Timer6 and Timer8). The PWM mode on the CCP and 10-bit PWM modules can use any of these timers.

The CCPTMRS register is used to select which timer is used.

24.7 Register Definitions: CCP/PWM Timers Control

REGISTER 24-5: CCPTMRS1: PWM TIMER SELECTION CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
C8TSEL<1:0>(1)		C7TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **C8TSEL<1:0>:** CCP8 (PWM8) Timer Selection bits(1)
- 11 = CCP8 is based off Timer8 in PWM mode
- 10 = CCP8 is based off Timer6 in PWM mode
- 01 = CCP8 is based off Timer4 in PWM mode
- 00 = CCP8 is based off Timer2 in PWM mode

bit 5-4 **C7TSEL<1:0>:** CCP7 (PWM7) Timer Selection bits
- 11 = CCP7 is based off Timer8 in PWM mode
- 10 = CCP7 is based off Timer6 in PWM mode
- 01 = CCP7 is based off Timer4 in PWM mode
- 00 = CCP7 is based off Timer2 in PWM mode

bit 3-2 **C2TSEL<1:0>:** CCP2 (PWM2) Timer Selection bits
- 11 = CCP2 is based off Timer8 in PWM mode
- 10 = CCP2 is based off Timer6 in PWM mode
- 01 = CCP2 is based off Timer4 in PWM mode
- 00 = CCP2 is based off Timer2 in PWM mode

bit 1-0 **C1TSEL<1:0>:** CCP1 (PWM1) Timer Selection bits
- 11 = CCP1 is based off Timer8 in PWM mode
- 10 = CCP1 is based off Timer6 in PWM mode
- 01 = CCP1 is based off Timer4 in PWM mode
- 00 = CCP1 is based off Timer2 in PWM mode

Note 1: PIC16(L)F1777/9 only.

TABLE 24-4: SUMMARY OF REGISTERS ASSOCIATED WITH STANDARD PWM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CCPxCAP	—	—	—	—	CTS<3:0>				321
CCPxCON	EN	—	OUT	FMT	MODE<3:0>				319
CCPRxL	Capture/Compare/PWM Register x (LSB)								320
CCPRxH	Capture/Compare/PWM Register x (MSB)								320
CCPTMRS1	C8TSEL<1:0>(1)		C7TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>		323
CCPTMRS2	P10TSEL<1:0>(1)		P9TSEL<1:0>		P4TSEL<1:0>		P3TSEL<1:0>		323
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	132
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	133
PIE2	OSFIE	C2IE	C1IE	COG1IE	BCL1IE	C4IE	C3IE	CCP2IE	134
PIE5	CCP8IE(1)	CCP7IE	COG4IE(1)	COG3IE	C8IE(1)	C7IE(1)	C6IE	C5IE	137
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	139
PIR2	OSFIF	C2IF	C1IF	COG1IF	BCL1IF	C4IF	C3IF	CCP2IF	140
PIR5	CCP8IF(1)	CCP7IF	COG4IF(1)	COG3IF	C8IF(1)	C7IF(1)	C6IF	C5IF	143
T2PR	Timer2 Period Register								287*
T2CON	ON	CKPS<2:0>			OUTPS<3:0>				307
TMR2	Timer2 Module Register								287
T4PR	Timer4 Period Register								287*
T4CON	ON	CKPS<2:0>			OUTPS<3:0>				307
TMR4	Timer4 Module Register								287
T6PR	Timer6 Period Register								287*
T6CON	ON	CKPS<2:0>			OUTPS<3:0>				307
TMR6	Timer6 Module Register								287
T8PR	Timer8 Period Register								287*
T8CON	ON	CKPS<2:0>			OUTPS<3:0>				307
TMR8	Timer8 Module Register								287

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the PWM.
* Page provides register information.
Note 1: PIC16(L)F1777/9 only.

EXAMPLE 27-1: TIMER UNCERTAINTY

Given:

$$Count = Ah = 10d$$

$$F_{COG\_\text{Clock}} = 8\text{MHz}$$

Therefore:

$$T_{\text{uncertainty}} = \frac{1}{F_{COG\_\text{clock}}}$$

$$= \frac{1}{8MHz} = 125ns$$

Proof:

$$T_{\min} = \frac{Count}{F_{COG\_\text{clock}}}$$

$$= 125ns \bullet 10d = 1.25\mu s$$

$$T_{\max} = \frac{Count + 1}{F_{COG\_\text{clock}}}$$

$$= 125ns \bullet (10d + 1)$$

$$= 1.375\mu s$$

Therefore:

$$T_{\text{uncertainty}} = T_{\max} - T_{\min}$$

$$= 1.375\mu s - 1.25\mu s$$

$$= 125ns$$

27.10 Auto-Shutdown Control

Auto-shutdown is a method to immediately override the COG output levels with specific overrides that allow for safe shutdown of the circuit.

The shutdown state can be either cleared automatically or held until cleared by software. In either case, the shutdown overrides remain in effect until the first rising event after the shutdown is cleared.

27.10.1 SHUTDOWN

The shutdown state can be entered by either of the following two mechanisms:

- Software generated
- External Input

27.10.1.1 Software Generated Shutdown

Setting the ASE bit of the COGxASD0 register (Register 27-11) will force the COG into the shutdown state.

When auto-restart is disabled, the shutdown state will persist until the first rising event after the ASE bit is cleared by software.

When auto-restart is enabled, the ASE bit will clear automatically and resume operation on the first rising event after the shutdown input clears. See Figure 27-15 and **Section 27.10.3.2 "Auto-Restart"**.

27.10.1.2 External Shutdown Source

External shutdown inputs provide the fastest way to safely suspend COG operation in the event of a Fault condition. When any of the selected shutdown inputs go true, the output drive latches are reset and the COG outputs immediately go to the selected override levels without software delay.

Any combination of the input sources can be selected to cause a shutdown condition. Shutdown occurs when the selected source is low. Shutdown input sources include:

- Any input pin selected with the COGxINPPS control
- Comparator 1
- Comparator 2
- Comparator 3
- Comparator 4
- CLC2 output/CLC4 output
- Timer2 output/Timer6 output
- Timer4 output/Timer8 output

Shutdown inputs are selected independently with bits of the COGxASD1 register (Register 27-12).

Note:	Shutdown inputs are level sensitive, not edge sensitive. The shutdown state cannot be cleared as long as the shutdown input level persists, except by disabling auto-shutdown,

27.10.2 PIN OVERRIDE LEVELS

The levels driven to the output pins, while the shutdown is active, are controlled by the ASDAC<1:0> and ASDBC<1:0> bits of the COGxASD0 register (Register 27-11). ASDAC<1:0> controls the COGxA and COGxC override levels and ASDBC<1:0> controls the COGxB and COGxD override levels. There are four override options for each output pair:

- Forced low
- Forced high
- Tri-state
- PWM inactive state (same state as that caused by a falling event)

Note:	The polarity control does not apply to the forced low and high override levels but does apply to the PWM inactive state.

REGISTER 28-10: CLCxGLS3: GATE 4 LOGIC SELECT REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **G4D4T:** Gate 4 Data 4 True (non-inverted) bit
1 = d4T is gated into g4
0 = d4T is not gated into g4

bit 6 **G4D4N:** Gate 4 Data 4 Negated (inverted) bit
1 = d4N is gated into g4
0 = d4N is not gated into g4

bit 5 **G4D3T:** Gate 4 Data 3 True (non-inverted) bit
1 = d3T is gated into g4
0 = d3T is not gated into g4

bit 4 **G4D3N:** Gate 4 Data 3 Negated (inverted) bit
1 = d3N is gated into g4
0 = d3N is not gated into g4

bit 3 **G4D2T:** Gate 4 Data 2 True (non-inverted) bit
1 = d2T is gated into g4
0 = d2T is not gated into g4

bit 2 **G4D2N:** Gate 4 Data 2 Negated (inverted) bit
1 = d2N is gated into g4
0 = d2N is not gated into g4

bit 1 **G4D1T:** Gate 4 Data 1 True (non-inverted) bit
1 = d1T is gated into g4
0 = d1T is not gated into g4

bit 0 **G4D1N:** Gate 4 Data 1 Negated (inverted) bit
1 = d1N is gated into g4
0 = d1N is not gated into g4

TABLE 30-5: PROGRAMMABLE RAMP GENERATOR TIMING SOURCES

RTSS<3:0>/ FTSS<3:0>	PRG1 Timing Source	PRG2 Timing Source	PRG3 Timing Source	PRG4 Timing Source(2)
1111	Reserved	Reserved	PWM12_output(2)	PWM12_output
1110	Reserved	Reserved	PWM11_output	PWM11_output
1101	LC2_out	LC2_out	PWM6_output	PWM6_output
1100	LC1_out	LC1_out	PWM5_output	PWM5_output
1011	PWM10_output(2)	PWM10_output(2)	Reserved	Reserved
1010	PWM9_output	PWM9_output	Reserved	Reserved
1001	PWM4_output	PWM4_output	LC4_out(2)	LC4_out
1000	PWM3_output	PWM3_output	LC3_out	LC3_out
0111	PRGxR/PRGxF Pin(1)	PRGxR/PRGxF Pin(1)	PRGxR/PRGxF Pin(1)	PRGxR/PRGxF Pin(1)
0110	Reserved	Reserved	sync_C7OUT(2)	sync_C7OUT
0101	Reserved	Reserved	sync_C6OUT	sync_C6OUT
0100	Reserved	Reserved	sync_C5OUT	sync_C5OUT
0011	sync_C4OUT	sync_C4OUT	Reserved	Reserved
0010	sync_C3OUT	sync_C3OUT	Reserved	Reserved
0001	sync_C2OUT	sync_C2OUT	Reserved	Reserved
0000	sync_C1OUT	sync_C1OUT	Reserved	Reserved

Note 1: Input pin is selected with the PRGxRPPS or PRGxFPPS register.
2: PIC16(L)F1777/9 only.

32.5.6 CLOCK STRETCHING

Clock stretching occurs when a device on the bus holds the SCL line low, effectively pausing communication. The slave may stretch the clock to allow more time to handle data or prepare a response for the master device. A master device is not concerned with stretching as anytime it is active on the bus and not transferring data it is stretching. Any stretching done by a slave is invisible to the master software and handled by the hardware that generates SCL.

The CKP bit of the SSPxCON1 register is used to control stretching in software. Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. Setting CKP will release SCL and allow more communication.

32.5.6.1 Normal Clock Stretching

Following an $\overline{ACK}$ if the R/$\overline{W}$ bit of SSPxSTAT is set, a read request, the slave hardware will clear CKP. This allows the slave time to update SSPxBUF with data to transfer to the master. If the SEN bit of SSPxCON2 is set, the slave hardware will always stretch the clock after the $\overline{ACK}$ sequence. Once the slave is ready; CKP is set by software and communication resumes.

Note 1: The BF bit has no effect on if the clock will be stretched or not. This is different than previous versions of the module that would not stretch the clock, clear CKP, if SSPxBUF was read before the ninth falling edge of SCL.

2: Previous versions of the module did not stretch the clock for a transmission if SSPxBUF was loaded before the ninth falling edge of SCL. It is now always cleared for read requests.

32.5.6.2 10-bit Addressing Mode

In 10-bit Addressing mode, when the UA bit is set the clock is always stretched. This is the only time the SCL is stretched without CKP being cleared. SCL is released immediately after a write to SSPxADD.

Note: Previous versions of the module did not stretch the clock if the second address byte did not match.

32.5.6.3 Byte NACKing

When AHEN bit of SSPxCON3 is set; CKP is cleared by hardware after the eighth falling edge of SCL for a received matching address byte. When DHEN bit of SSPxCON3 is set; CKP is cleared after the eighth falling edge of SCL for received data.

Stretching after the eighth falling edge of SCL allows the slave to look at the received address or data and decide if it wants to ACK the received data.

32.5.6.4 Clock Synchronization and the CKP Bit

Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. However, clearing the CKP bit will not assert the SCL output low until the SCL output is already sampled low. Therefore, the CKP bit will not assert the SCL line until an external I^2C master device has already asserted the SCL line. The SCL output will remain low until the CKP bit is set and all other devices on the I^2C bus have released SCL. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCL (see Figure 32-23).

FIGURE 32-23: CLOCK SYNCHRONIZATION TIMING

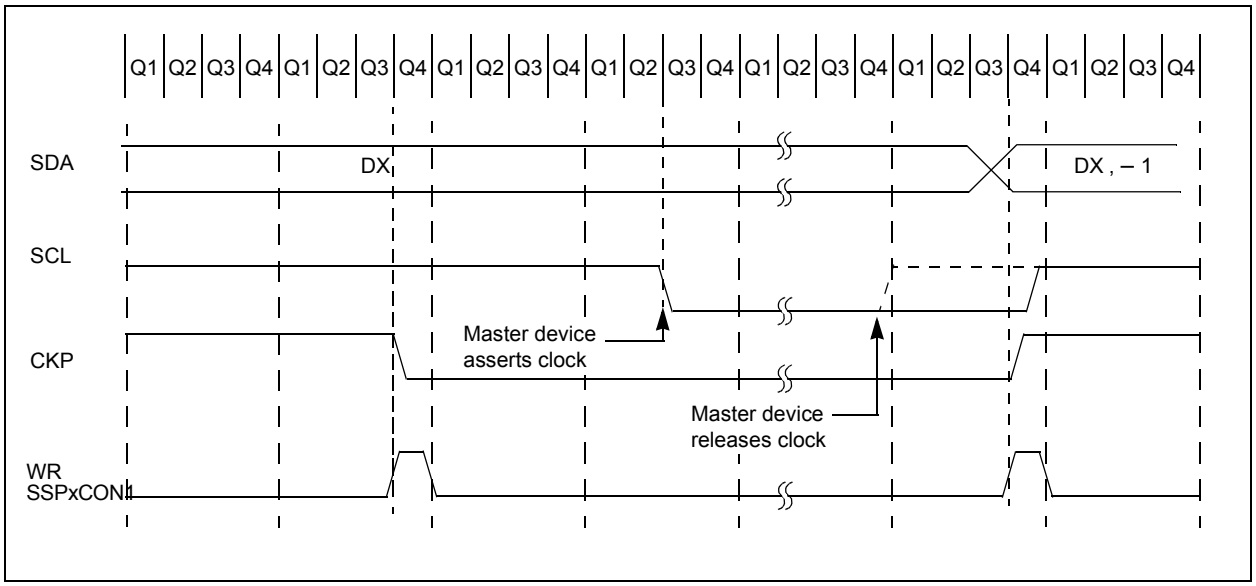


TABLE 33-2: SUMMARY OF REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	177
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	182
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—	187
BAUD1CON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	505
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	132
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	133
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	139
RC1REG	EUSART Receive Data Register								498*
RC1STA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	504
RxyPPS	—	—	RxyPPS<5:0>						205
SP1BRGL	SP1BRG<7:0>								506
SP1BRGH	SP1BRG<15:8>								506
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	176
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	181
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	186
TX1STA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	503

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for asynchronous reception.

* Page provides register information.

33.5.2 SYNCHRONOUS SLAVE MODE

The following bits are used to configure the EUSART for synchronous slave operation:

- SYNC = 1
- CSRC = 0
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXxSTA register configures the device for synchronous operation. Clearing the CSRC bit of the TXxSTA register configures the device as a slave. Clearing the SREN and CREN bits of the RCxSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCxSTA register enables the EUSART.

33.5.2.1 EUSART Synchronous Slave Transmit

The operation of the Synchronous Master and Slave modes are identical (see **Section 33.5.1.3 "Synchronous Master Transmission")**, except in the case of the Sleep mode.

If two words are written to the TXxREG and then the SLEEP instruction is executed, the following will occur:

1. The first character will immediately transfer to the TSR register and transmit.
2. The second word will remain in the TXxREG register.
3. The TXIF bit will not be set.
4. After the first character has been shifted out of TSR, the TXxREG register will transfer the second character to the TSR and the TXIF bit will now be set.
5. If the PEIE and TXIE bits are set, the interrupt will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will call the Interrupt Service Routine.

33.5.2.2 Synchronous Slave Transmission Set-up:

1. Set the SYNC and SPEN bits and clear the CSRC bit.
2. Clear the ANSEL bit for the CK pin (if applicable).
3. Clear the CREN and SREN bits.
4. If interrupts are desired, set the TXIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
5. If 9-bit transmission is desired, set the TX9 bit.
6. Enable transmission by setting the TXEN bit.
7. If 9-bit transmission is selected, insert the Most Significant bit into the TX9D bit.
8. Start transmission by writing the Least Significant eight bits to the TXxREG register.

36.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:

Operating Voltage: $V_{DDMIN} \leq V_{DD} \leq V_{DDMAX}$
Operating Temperature: $T_{A\_MIN} \leq T_A \leq T_{A\_MAX}$

V_{DD} — Operating Supply Voltage(1)

PIC16LF1777/8/9

- V_{DDMIN} (Fosc ≤ 16 MHz) ..... +1.8V
- V_{DDMIN} (Fosc > 16 MHz) ..... +2.5V
- V_{DDMAX} ..... +3.6V

PIC16F1777/8/9

- V_{DDMIN} (Fosc ≤ 16 MHz) ..... +2.3V
- V_{DDMIN} (Fosc > 16 MHz) ..... +2.5V
- V_{DDMAX} ..... +5.5V

T_A — Operating Ambient Temperature Range

Industrial Temperature

- T_{A_MIN} ..... -40°C
- T_{A_MAX} ..... +85°C

Extended Temperature

- T_{A_MIN} ..... -40°C
- T_{A_MAX} ..... +125°C

Note 1: See Parameter D001, DS Characteristics: Supply Voltage.

37.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified V_{DD} range). This is for **information only** and devices are ensured to operate properly only within the specified range.

Unless otherwise noted, all graphs apply to both the L and LF devices.

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum", "Max.", "Minimum" or "Min." represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

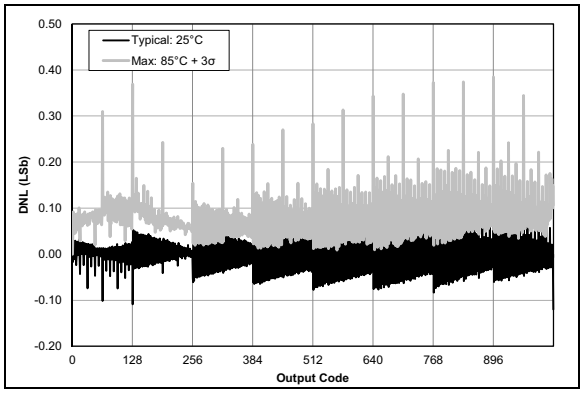


FIGURE 37-121: *DAC DNL Error, V_{DD} = 3.0V, V_{REF} = External 3V.*

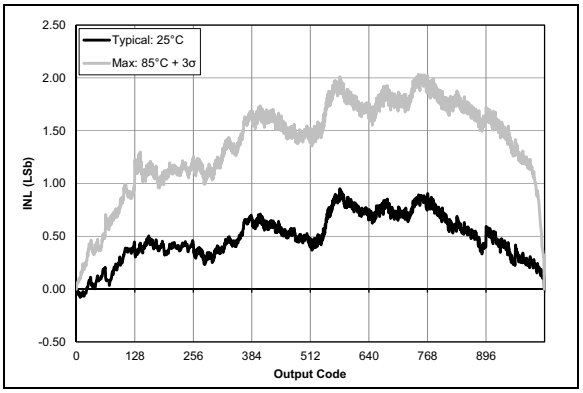


FIGURE 37-122: *DAC INL Error, V_{DD} = 3.0V, V_{REF} = External 3V.*

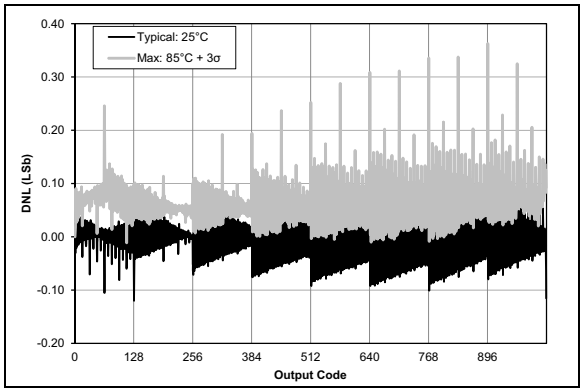


FIGURE 37-123: *DAC DNL Error, V_{DD} = 5.0V, V_{REF} = External 5V, PIC16F1777/8/9 Only.*

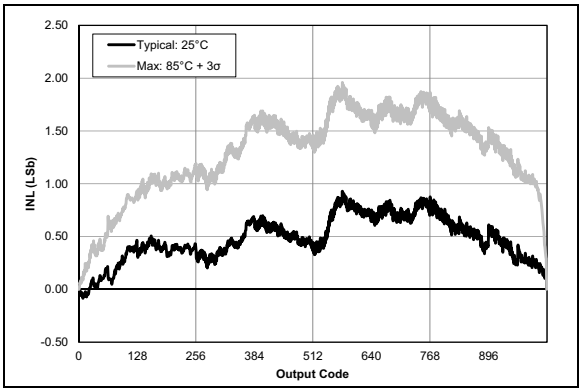


FIGURE 37-124: *Typical DAC INL Error, V_{DD} = 5.0V, V_{REF} = External 5V, PIC16F1777/8/9 Only.*

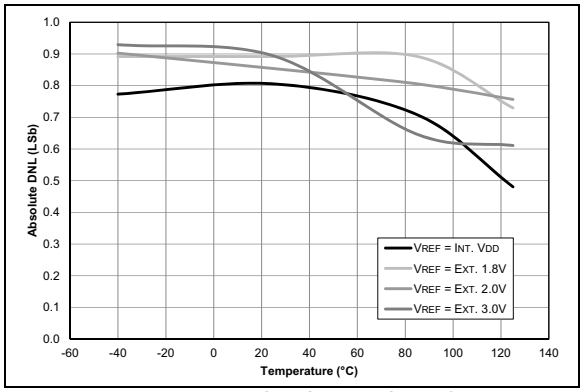


FIGURE 37-125: *Absolute Value of DAC DNL Error, V_{DD} = 3.0V, V_{REF} = V_{DD}.*

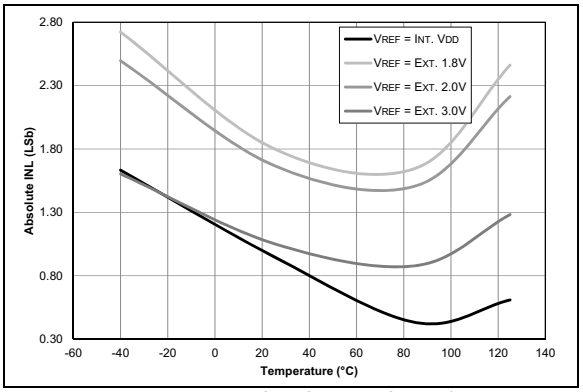


FIGURE 37-126: *Absolute Value of DAC INL Error, V_{DD} = 3.0V, V_{REF} = V_{DD}.*