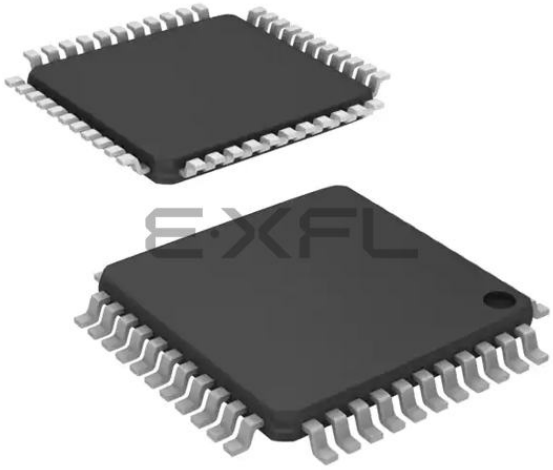

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x10b; D/A 4x5b, 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1777-i-pt

4.6 Device ID and Revision ID

The 14-bit device ID word is located at 8006h and the 14-bit revision ID is located at 8005h. These locations are read-only and cannot be erased or modified. See **Section 10.4 "User ID, Device ID and Configuration Word Access"** for more information on accessing these memory locations.

Development tools, such as device programmers and debuggers, may be used to read the Device ID and Revision ID.

4.7 Register Definitions: Device and Revision

REGISTER 4-3: DEVID: DEVICE ID REGISTER

R	R	R	R	R	R
DEV<13:8>					
bit 13					bit 8

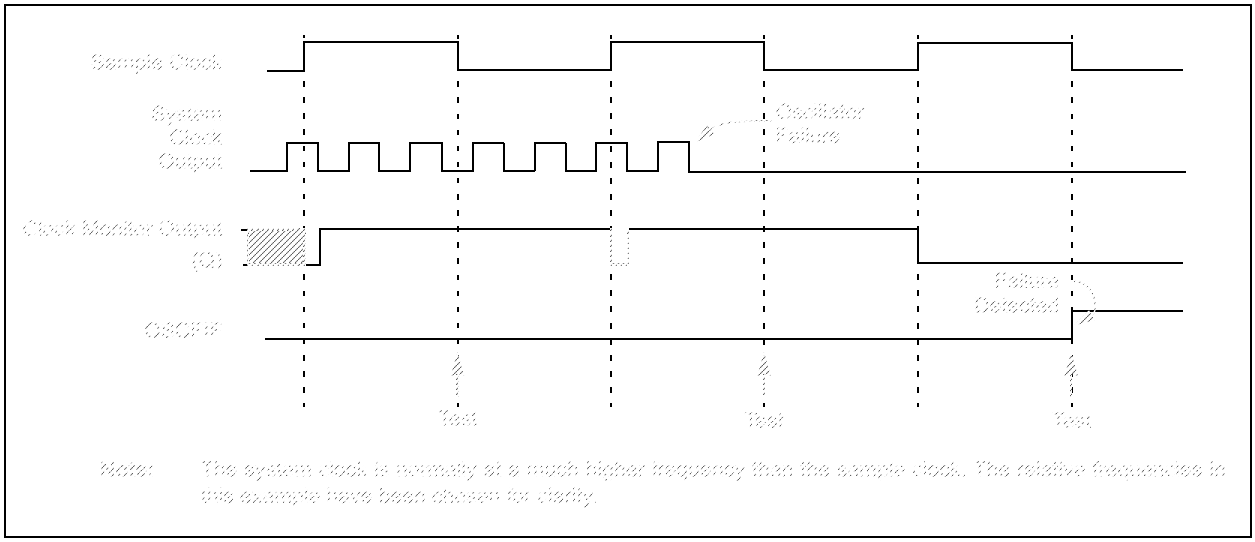
R	R	R	R	R	R	R	R
DEV<7:0>							
bit 7							bit 0

Legend:	
R = Readable bit	
'1' = Bit is set	'0' = Bit is cleared

bit 13-0 **DEV<13:0>:** Device ID bits

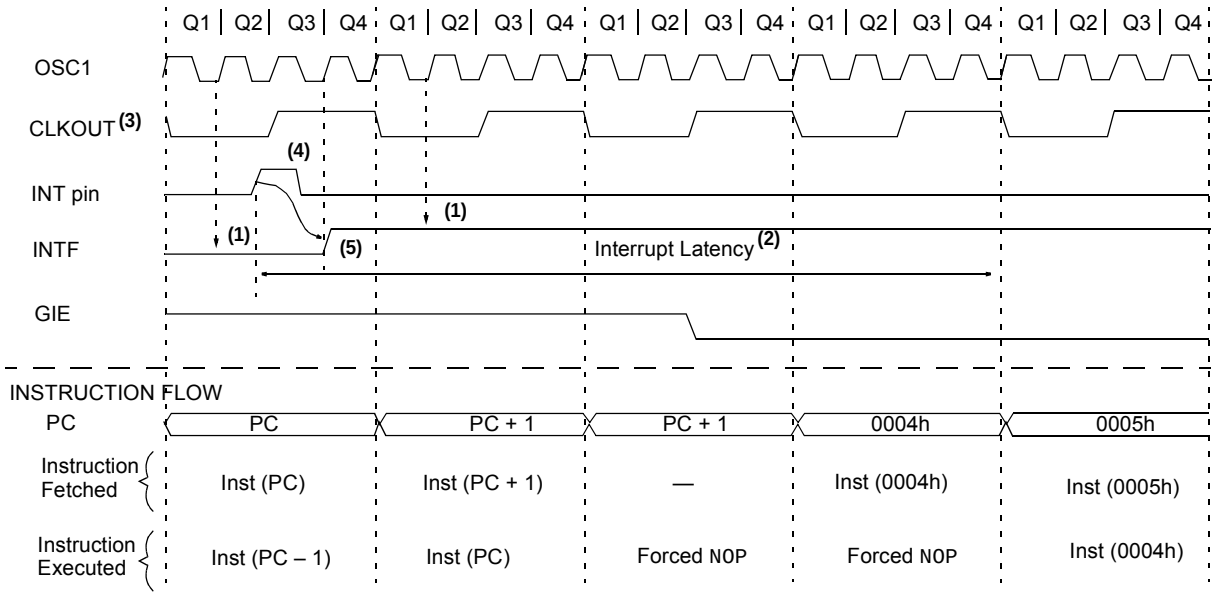
Device	DEVID<13:0> Values
PIC16F1777	11 0000 1000 1110 (308E)
PIC16F1778	11 0000 1000 1111 (308F)
PIC16F1779	11 0000 1001 0000 (3090)
PIC16LF1777	11 0000 1001 0001 (3091)
PIC16LF1778	11 0000 1001 0010 (3092)
PIC16LF1779	11 0000 1001 0011 (3093)

FIGURE 5-10: FSCM TIMING DIAGRAM



Note: The system clock is normally at a much higher frequency than the sample clock. The relative frequencies in this example have been chosen for clarity.

FIGURE 7-3: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).

2: Asynchronous interrupt latency = 3-5 TCY. Synchronous latency = 3-4 TCY, where TCY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: CLKOUT not available in all oscillator modes.

4: For minimum width of INT pulse, refer to AC specifications in **Section 36.0 "Electrical Specifications"**".

5: INTF is enabled to be set any time during the Q4-Q1 cycles.

EXAMPLE 10-3: WRITING TO FLASH PROGRAM MEMORY

```
; This write routine assumes the following:
; 1. 64 bytes of data are loaded, starting at the address in DATA_ADDR
; 2. Each word of data to be written is made up of two adjacent bytes in DATA_ADDR,
; stored in little endian format
; 3. A valid starting address (the least significant bits = 00000) is loaded in ADDRH:ADDRL
; 4. ADDRH and ADDRL are located in shared data memory 0x70 - 0x7F (common RAM)
;
        BCF         INTCON,GIE      ; Disable ints so required sequences will execute properly
        BANKSEL     PMADRH          ; Bank 3
        MOVF        ADDRH,W         ; Load initial address
        MOVWF       PMADRH          ;
        MOVF        ADDRL,W         ;
        MOVWF       PMADRL          ;
        MOVLW       LOW DATA_ADDR   ; Load initial data address
        MOVWF       FSR0L           ;
        MOVLW       HIGH DATA_ADDR  ; Load initial data address
        MOVWF       FSR0H           ;
        BCF         PMCON1,CFGS     ; Not configuration space
        BSF         PMCON1,WREN     ; Enable writes
        BSF         PMCON1,LWLO     ; Only Load Write Latches
LOOP
        MOVIW       FSR0++          ; Load first data byte into lower
        MOVWF       PMDATL          ;
        MOVIW       FSR0++          ; Load second data byte into upper
        MOVWF       PMDATH          ;

        MOVF        PMADRL,W        ; Check if lower bits of address are '00000'
        XORLW       0x1F            ; Check if we're on the last of 32 addresses
        ANDLW       0x1F            ;
        BTFSC       STATUS,Z        ; Exit if last of 32 words,
        GOTO        START_WRITE     ;

  Required Sequence
        MOVLW       55h             ; Start of required write sequence:
        MOVWF       PMCON2          ; Write 55h
        MOVLW       0AAh            ;
        MOVWF       PMCON2          ; Write AAh
        BSF         PMCON1,WR       ; Set WR bit to begin write
        NOP                         ; NOP instructions are forced as processor
                                    ; loads program memory write latches
        NOP                         ;

        INCF        PMADRL,F        ; Still loading latches Increment address
        GOTO        LOOP            ; Write next latches

START_WRITE
        BCF         PMCON1,LWLO     ; No more loading latches - Actually start Flash program
                                    ; memory write

  Required Sequence
        MOVLW       55h             ; Start of required write sequence:
        MOVWF       PMCON2          ; Write 55h
        MOVLW       0AAh            ;
        MOVWF       PMCON2          ; Write AAh
        BSF         PMCON1,WR       ; Set WR bit to begin write
        NOP                         ; NOP instructions are forced as processor writes
                                    ; all the program memory write latches simultaneously
        NOP                         ; to program memory.
                                    ; After NOPs, the processor
                                    ; stalls until the self-write process in complete
                                    ; after write processor continues with 3rd instruction
        BCF         PMCON1,WREN     ; Disable writes
        BSF         INTCON,GIE      ; Enable interrupts
```

REGISTER 11-22: WPUC: WEAK PULL-UP PORTC REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **WPUC<7:0>**: Weak Pull-up Register bits(1, 2)
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: Global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is configured as an output.

REGISTER 11-23: ODCONC: PORTC OPEN-DRAIN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ODC7	ODC6	ODC5	ODC4	ODC3	ODC2	ODC1	ODC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ODC<7:0>:** PORTC Open-Drain Enable bits
For RC<7:0> pins
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

REGISTER 18-4: DACLD: DAC BUFFER LOAD REGISTER

U-0	U-0	U-0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
—	—	DAC6LD(1)	DAC5LD	—	—	DAC2LD	DAC1LD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = value depends on configuration bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **DAC6LD:** DAC6 Double Buffer Load bit(1)
- 1 = DAC6REFHL:DAC6REFL values are transfered to the double buffer. Bit is cleared automatically by hardware.
- 0 = DAC6REFHL:DAC6REFL double buffers remain unchanged.

bit 4 **DAC5LD:** DAC5 Double Buffer Load bit
- 1 = DAC5REFHL:DAC5REFL values are transfered to the double buffer. Bit is cleared automatically by hardware.
- 0 = DAC5REFHL:DAC5REFL double buffers remain unchanged.

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **DAC2LD:** DAC2 Double Buffer Load bit
- 1 = DAC2REFHL:DAC2REFL values are transfered to the double buffer. Bit is cleared automatically by hardware.
- 0 = DAC2REFHL:DAC2REFL double buffers remain unchanged.

bit 0 **DAC1LD:** DAC1 Double Buffer Load bit
- 1 = DAC1REFHL:DAC1REFL values are transfered to the double buffer. Bit is cleared automatically by hardware.
- 0 = DAC1REFHL:DAC1REFL double buffers remain unchanged.

Note 1: PIC16LF1777/9 only.

TABLE 18-3: SUMMARY OF REGISTERS ASSOCIATED WITH THE DACx MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
DAC1CON0	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC2CON0	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC5CON0	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC6CON0(1)	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC1REFH	REF<9:x> (x Depends on FM bit)								250
DAC2REFH	REF<9:x> (x Depends on FM bit)								250
DAC5REFH	REF<9:x> (x Depends on FM bit)								250
DAC6REFH(1)	REF<9:x> (x Depends on FM bit)								250
DAC1REFL	REF<x-1:0> (x Depends on FM bit)								250
DAC2REFL	REF<x-1:0> (x Depends on FM bit)								250
DAC5REFL	REF<x-1:0> (x Depends on FM bit)								250
DAC6REFL(1)	REF<x-1:0> (x Depends on FM bit)								250
DACLD	—	—	—	DAC5LD	—	—	DAC2LD	DAC1LD	251

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used with the DACx module.

Note 1: PIC16LF1777/9 only.

TABLE 19-6: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	177
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	182
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—	187
CM1CON0	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	258
CM2CON0	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	258
CM3CON0	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	258
CM4CON0	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	258
CM5CON0	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	258
CM6CON0	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	258
CM1CON1	—	—	—	—	—	—	INTP	INTN	259
CM2CON1	—	—	—	—	—	—	INTP	INTN	259
CM3CON1	—	—	—	—	—	—	INTP	INTN	259
CM4CON1	—	—	—	—	—	—	INTP	INTN	259
CM5CON1	—	—	—	—	—	—	INTP	INTN	259
CM6CON1	—	—	—	—	—	—	INTP	INTN	259
CM7CON1(1)	—	—	—	—	—	—	INTP	INTN	259
CM8CON1(1)	—	—	—	—	—	—	INTP	INTN	259
CM1NSEL	—	—	—	—	NCH<3:0>				260
CM2NSEL	—	—	—	—	NCH<3:0>				260
CM3NSEL	—	—	—	—	NCH<3:0>				260
CM4NSEL	—	—	—	—	NCH<3:0>				260
CM5NSEL	—	—	—	—	NCH<3:0>				260
CM6NSEL	—	—	—	—	NCH<3:0>				260
CM7NSEL(1)	—	—	—	—	NCH<3:0>				260
CM8NSEL(1)	—	—	—	—	NCH<3:0>				260
CM1PSEL	—	—	—	—	PCH<3:0>				261
CM2PSEL	—	—	—	—	PCH<3:0>				261
CM3PSEL	—	—	—	—	PCH<3:0>				261
CM4PSEL	—	—	—	—	PCH<3:0>				261
CM5PSEL	—	—	—	—	PCH<3:0>				261
CM6PSEL	—	—	—	—	PCH<3:0>				261
CM7PSEL(1)	—	—	—	—	PCH<3:0>				261
CM8PSEL(1)	—	—	—	—	PCH<3:0>				261
CMOUT	MC8OUT(1)	MC7OUT(1)	MC6OUT	MC5OUT	MC4OUT	MC3OUT	MC2OUT	MC1OUT	262
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		223
DAC1CON0	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC2CON0	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC5CON0	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC6CON0(1)	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC3CON0	EN	—	OE1	OE2	PSS<1:0>		NSS<1:0>		244
DAC4CON0	EN	—	OE1	OE2	PSS<1:0>		NSS<1:0>		244
DAC7CON0	EN	—	OE1	OE2	PSS<1:0>		NSS<1:0>		244
DAC8CON0(1)	EN	—	OE1	OE2	PSS<1:0>		NSS<1:0>		244
DAC3REF	---	---	---	REF<4:0>					245
DAC4REF	---	---	---	REF<4:0>					245
DAC7REF	---	---	---	REF<4:0>					245
DAC8REF(1)	---	---	---	REF<4:0>					245
DAC1REFH	REF<9:x> (x Depends on FM bit)								250

Legend: — = unimplemented location, read as '0'. Shaded cells are unused by the comparator module.
Note 1: PIC16LF1777/9 only.

REGISTER 26-2: PWMxINTE: PWM INTERRUPT ENABLE REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	OFIE	PHIE	DCIE	PRIE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **OFIE**: Offset Interrupt Enable bit
1 = Interrupt CPU on Offset Match
0 = Do not interrupt CPU on Offset Match

bit 2 **PHIE:** Phase Interrupt Enable bit
1 = Interrupt CPU on Phase Match
0 = Do not Interrupt CPU on Phase Match

bit 1 **DCIE:** Duty Cycle Interrupt Enable bit
1 = Interrupt CPU on Duty Cycle Match
0 = Do not interrupt CPU on Duty Cycle Match

bit 0 **PRIE:** Period Interrupt Enable bit
1 = Interrupt CPU on Period Match
0 = Do not interrupt CPU on Period Match

REGISTER 26-3: PWMxINTF: PWM INTERRUPT REQUEST REGISTER

U-0	U-0	U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
—	—	—	—	OFIF	PHIF	DCIF	PRIF
bit 7							bit 0

Legend:		
HC = Bit is cleared by hardware		HS = Bit is set by hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **OFIF**: Offset Interrupt Flag bit(1)
1 = Offset Match Event occurred
0 = Offset Match Event did not occur

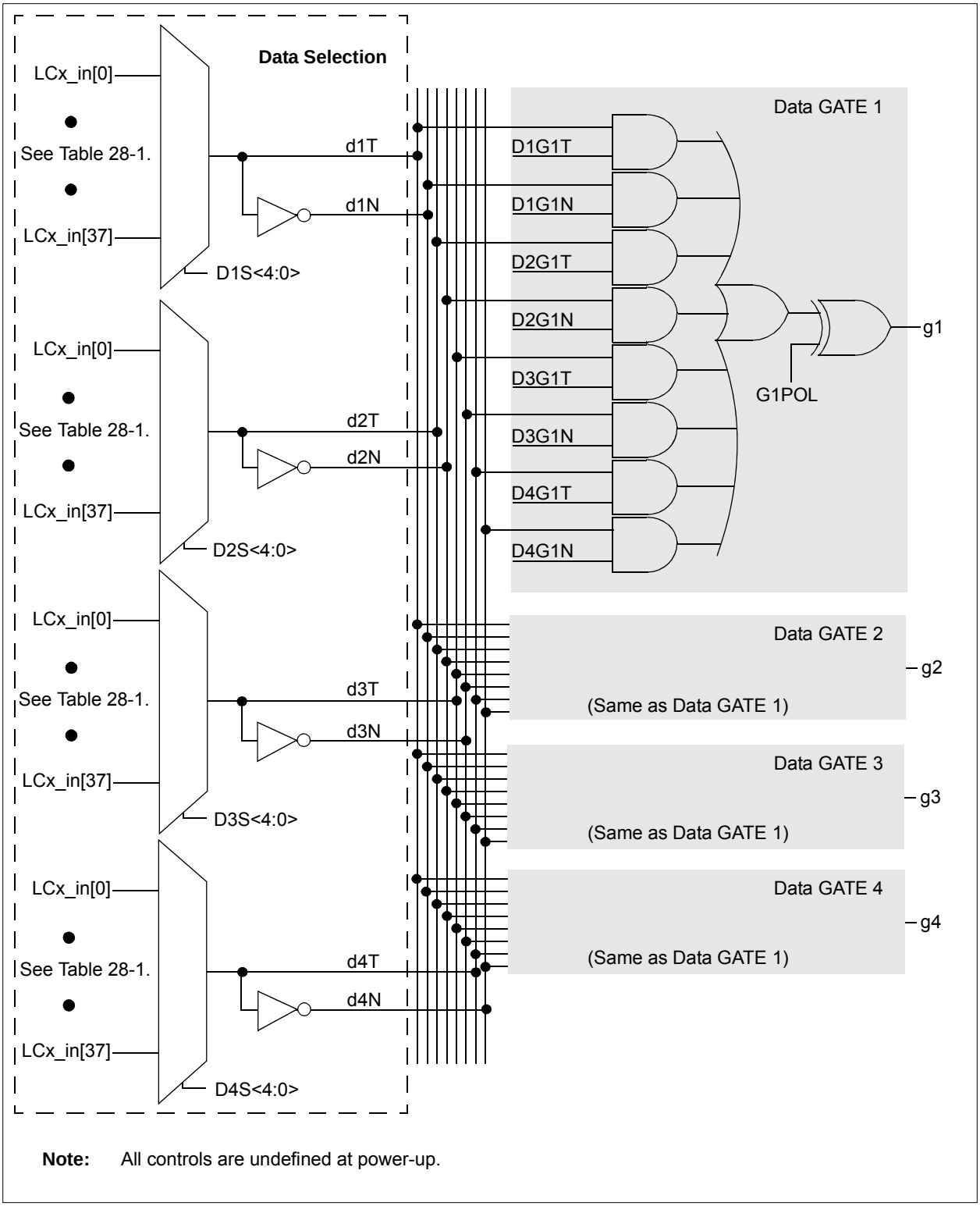
bit 2 **PHIF:** Phase Interrupt Flag bit(1)
1 = Phase Match Event occurred
0 = Phase Match Event did not occur

bit 1 **DCIF:** Duty Cycle Interrupt Flag bit(1)
1 = Duty Cycle Match Event occurred
0 = Duty Cycle Match Event did not occur

bit 0 **PRIF:** Period Interrupt Flag bit(1)
1 = Period Match Event occurred
0 = Period Match Event did not occur

Note 1: Bit is forced clear by hardware while module is disabled (EN = 0).

FIGURE 28-2: INPUT DATA SELECTION AND GATING



Note: All controls are undefined at power-up.

REGISTER 29-4: OPAxPCHS: OP AMP POSITIVE CHANNEL SOURCE SELECT REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	PCH<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-4 **Unimplemented:** Read as '0'

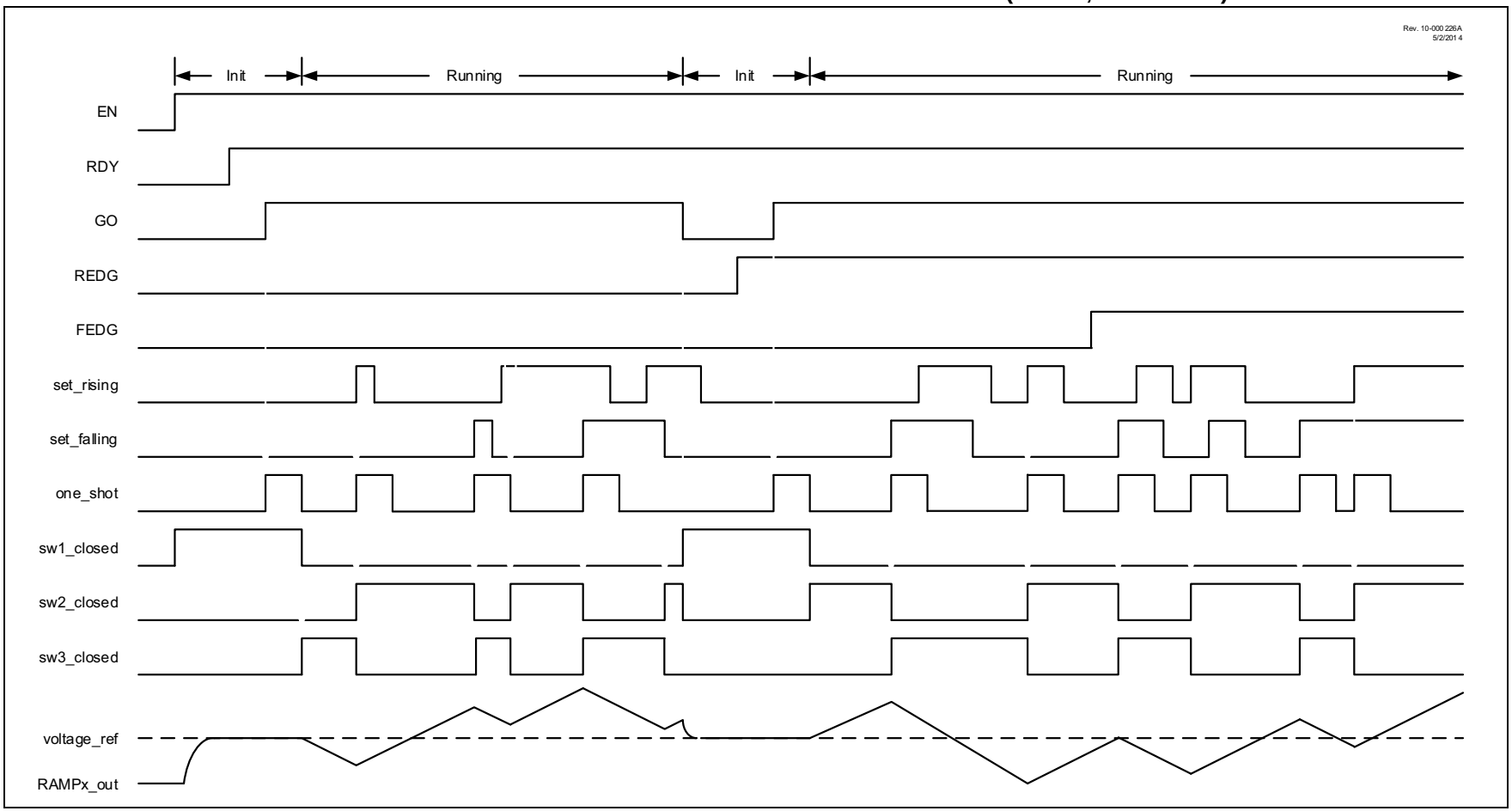
bit 3-0 **PCH<3:0>:** Op Amp Non-Inverting Input Channel Selection bits
See Table 29-5: Non-Inverting Input Sources

TABLE 29-5: NON-INVERTING INPUT SOURCES

NCH<3:0>	OPA1	OPA2	OPA3	OPA4(1)
1111	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use
1110	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use
1101	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use
1100	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use
1011	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use
1010	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use
1001	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use	Reserved. Do not use
1000	PRG2_out	PRG2_out	PRG4_out(1)	PRG4_out
0111	PRG1_out	PRG1_out	PRG3_out	PRG3_out
0110	FVR_Buffer1	FVR_Buffer1	FVR_Buffer2	FVR_Buffer2
0101	DAC4_out	DAC4_out	DAC8_out(1)	DAC8_out
0100	DAC3_out	DAC3_out	DAC7_out	DAC7_out
0011	DAC2_out	DAC2_out	DAC6_out(1)	DAC6_out
0010	DAC1_out	DAC1_out	DAC5_out	DAC5_out
0001	OPA1IN1+	OPA2IN1+	OPA3IN1+(1)	OPA4IN1+
0000	OPA1IN0+	OPA2IN0+	OPA3IN0+	OPA4IN0+

Note 1: PIC16(L)F1777/9 only.

FIGURE 30-4: ALTERNATING RISING/FALLING RAMP GENERATION TIMING DIAGRAM (OS = 1, MODE = 01)



REGISTER 31-2: MDxCON1: MODULATION CONTROL REGISTER 1

U-0	U-0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
—	—	CHPOL	CHSYNC	—	—	CLPOL	CLSYNC
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **CHPOL:** Modulation High Carrier Polarity Select bit
1 = Selected high carrier source is inverted
0 = Selected high carrier source is not inverted

bit 4 **CHSYNC:** Modulation High Carrier Synchronization Enable bit
1 = Modulator waits for a low edge on the high carrier before allowing a switch to the low carrier
0 = Modulator output is not synchronized to the high carrier(1)

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1 **CLPOL:** Modulation Low Carrier Polarity Select bit
1 = Selected low carrier source is inverted
0 = Selected low carrier source is not inverted

bit 0 **CLSYNC:** Modulation Low Carrier Synchronization Enable bit
1 = Modulator waits for a low edge on the low carrier before allowing a switch to the high carrier
0 = Modulator output is not synchronized to the low carrier(1)

Note 1: Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

REGISTER 31-3: MDxSRC: MODULATION SOURCE CONTROL REGISTER

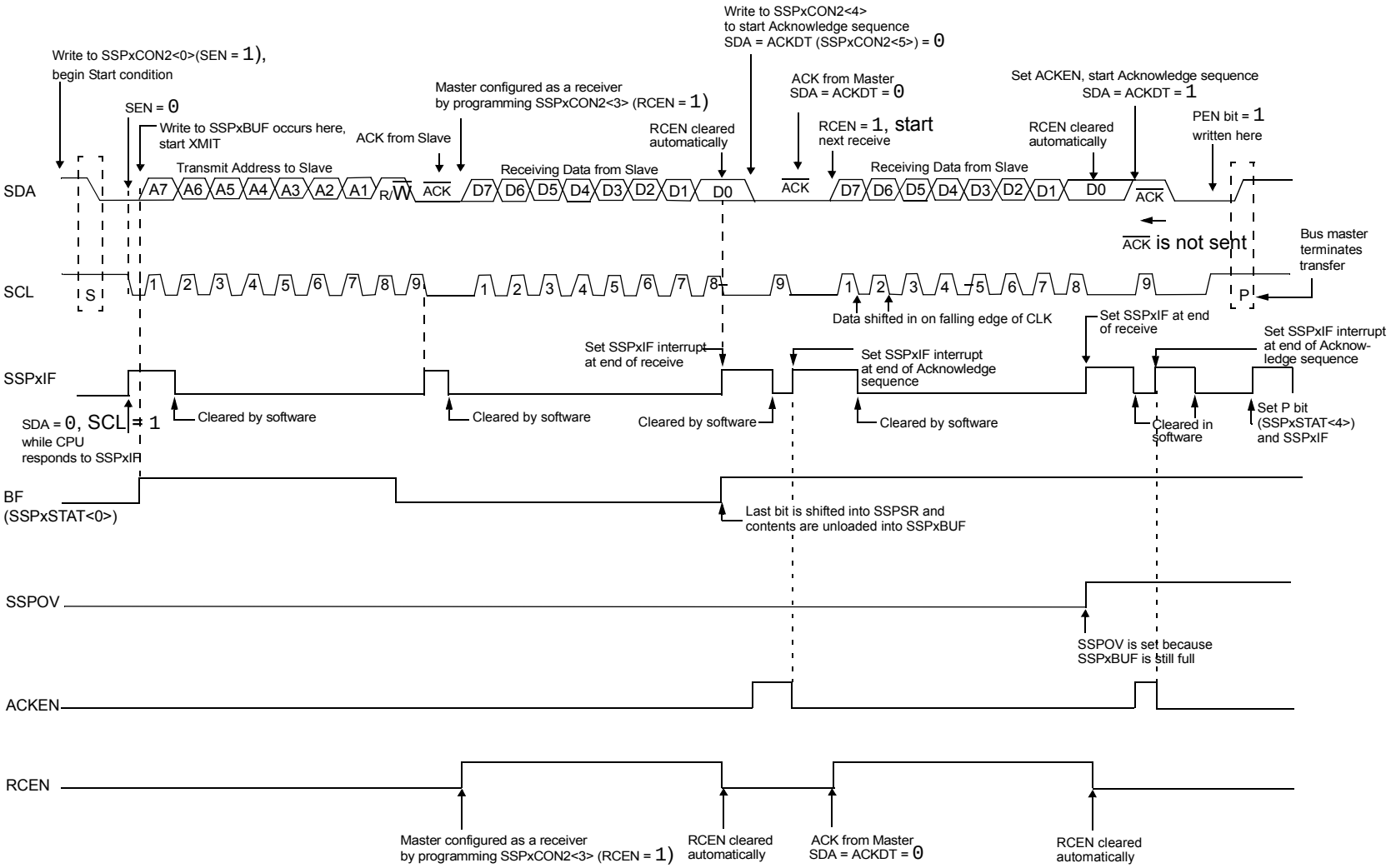
U-0	U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	MS<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **MS<4:0>** Modulation Source Selection bits
See Table 31-4 or Table 31-5.

FIGURE 32-29: I²C MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESS)



33.1 EUSART Asynchronous Mode

The EUSART transmits and receives data using the standard non-return-to-zero (NRZ) format. NRZ is implemented with two levels: a VOH Mark state which represents a '1' data bit, and a VOL Space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the Mark state. Each character transmission consists of one Start bit followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is eight bits. Each transmitted bit persists for a period of 1/(baud rate). An on-chip dedicated 8-bit/16-bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. See Table 33-5 for examples of baud rate configurations.

The EUSART transmits and receives the LSb first. The EUSART's transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is not supported by the hardware, but can be implemented in software and stored as the ninth data bit.

33.1.1 EUSART ASYNCHRONOUS TRANSMITTER

The EUSART transmitter block diagram is shown in Figure 33-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the TXxREG register.

33.1.1.1 Enabling the Transmitter

The EUSART transmitter is enabled for asynchronous operations by configuring the following three control bits:

- TXEN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the TXEN bit of the TXxSTA register enables the transmitter circuitry of the EUSART. Clearing the SYNC bit of the TXxSTA register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCxSTA register enables the EUSART and automatically configures the TX/CK I/O pin as an output. If the TX/CK pin is shared with an analog peripheral, the analog I/O function must be disabled by clearing the corresponding ANSEL bit.

Note:	The TXIF Transmitter Interrupt flag is set when the TXEN enable bit is set.

33.1.1.2 Transmitting Data

A transmission is initiated by writing a character to the TXxREG register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXxREG is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TXxREG until the Stop bit of the previous character has been transmitted. The pending character in the TXxREG is then transferred to the TSR in one TCY immediately following the Stop bit transmission. The transmission of the Start bit, data bits and Stop bit sequence commences immediately following the transfer of the data to the TSR from the TXxREG.

33.1.1.3 Transmit Data Polarity

The polarity of the transmit data can be controlled with the SCKP bit of the BAUDxCON register. The default state of this bit is '0', which selects high true transmit idle and data bits. Setting the SCKP bit to '1' will invert the transmit data resulting in low true idle and data bits. The SCKP bit controls transmit data polarity in Asynchronous mode only. In Synchronous mode, the SCKP bit has a different function. See **Section 33.5.1.2 "Clock Polarity"**.

33.1.1.4 Transmit Interrupt Flag

The TXIF interrupt flag bit of the PIR1 register is set whenever the EUSART transmitter is enabled and no character is being held for transmission in the TXxREG. In other words, the TXIF bit is only clear when the TSR is busy with a character and a new character has been queued for transmission in the TXxREG. The TXIF flag bit is not cleared immediately upon writing TXxREG. TXIF becomes valid in the second instruction cycle following the write execution. Polling TXIF immediately following the TXxREG write will return invalid results. The TXIF bit is read-only, it cannot be set or cleared by software.

The TXIF interrupt can be enabled by setting the TXIE interrupt enable bit of the PIE1 register. However, the TXIF flag bit will be set whenever the TXxREG is empty, regardless of the state of the TXIE enable bit.

To use interrupts when transmitting data, set the TXIE bit only when there is more data to send. Clear the TXIE interrupt enable bit upon writing the last character of the transmission to the TXxREG.

33.6 EUSART Operation During Sleep

The EUSART will remain active during Sleep only in the Synchronous Slave mode. All other modes require the system clock and therefore cannot generate the necessary signals to run the Transmit or Receive Shift registers during Sleep.

Synchronous Slave mode uses an externally generated clock to run the Transmit and Receive Shift registers.

33.6.1 SYNCHRONOUS RECEIVE DURING SLEEP

To receive during Sleep, all the following conditions must be met before entering Sleep mode:

- RCxSTA and TXxSTA Control registers must be configured for Synchronous Slave Reception (see **Section 33.5.2.4 "Synchronous Slave Reception Set-up:"**).
- If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- The RCIF interrupt flag must be cleared by reading RCxREG to unload any pending characters in the receive buffer.

Upon entering Sleep mode, the device will be ready to accept data and clocks on the RX/DT and TX/CK pins, respectively. When the data word has been completely clocked in by the external device, the RCIF interrupt flag bit of the PIR1 register will be set. Thereby, waking the processor from Sleep.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the Global Interrupt Enable (GIE) bit of the INTCON register is also set, then the Interrupt Service Routine at address 004h will be called.

33.6.2 SYNCHRONOUS TRANSMIT DURING SLEEP

To transmit during Sleep, all the following conditions must be met before entering Sleep mode:

- The RCxSTA and TXxSTA Control registers must be configured for synchronous slave transmission (see **Section 33.5.2.2 "Synchronous Slave Transmission Set-up:"**).
- The TXIF interrupt flag must be cleared by writing the output data to the TXxREG, thereby filling the TSR and transmit buffer.
- If interrupts are desired, set the TXIE bit of the PIE1 register and the PEIE bit of the INTCON register.
- Interrupt enable bits TXIE of the PIE1 register and PEIE of the INTCON register must set.

Upon entering Sleep mode, the device will be ready to accept clocks on TX/CK pin and transmit data on the RX/DT pin. When the data word in the TSR has been completely clocked out by the external device, the pending byte in the TXxREG will transfer to the TSR and the TXIF flag will be set. Thereby, waking the processor from Sleep. At this point, the TXxREG is available to accept another character for transmission, which will clear the TXIF flag.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the Global Interrupt Enable (GIE) bit is also set then the Interrupt Service Routine at address 0004h will be called.

RRF **Rotate Right f through Carry**

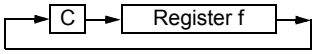
Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



SLEEP **Enter Sleep mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$,
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Description: The power-down Status bit, $\overline{PD}$ is cleared. Time-out Status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared.
The processor is put into Sleep mode with the oscillator stopped.

SUBLW **Subtract W from literal**

Syntax: [*label*] SUBLW k

Operands: $0 \le k \le 255$

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Description: The W register is subtracted (2's complement method) from the 8-bit literal 'k'. The result is placed in the W register.

C = 0	W > k
C = 1	W ≤ k
DC = 0	W<3:0> > k<3:0>
DC = 1	W<3:0> ≤ k<3:0>

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - (W) → (destination)

Status Affected: C, DC, Z

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f.

C = 0	W > f
C = 1	W ≤ f
DC = 0	W<3:0> > f<3:0>
DC = 1	W<3:0> ≤ f<3:0>

SUBWFB **Subtract W from f with Borrow**

Syntax: SUBWFB f {,d}

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) – (W) – ($\overline{B}$) → dest

Status Affected: C, DC, Z

Description: Subtract W and the BORROW flag (CARRY) from register 'f' (2's complement method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.

TABLE 36-2: SUPPLY CURRENT (I_{DD})(1,2)

PIC16LF1777/8/9		Standard Operating Conditions (unless otherwise stated)					
PIC16F1777/8/9							
Param No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
						V_{DD}	Note
D009	LDO Regulator	—	75	—	µA	—	High-Power mode, normal operation
		—	15	—	µA	—	Sleep, VREGCON<1> = 0
		—	0.3	—	µA	—	Sleep, VREGCON<1> = 1
D010		—	8	25	µA	1.8	F_{OSC} = 32 kHz, LP Oscillator mode **(Note 4)**, -40°C ≤ T_A ≤ +85°C
		—	12	30	µA	3.0	
D010		—	21	30	µA	2.3	F_{OSC} = 32 kHz, LP Oscillator mode **(Note 4,5)** -40°C ≤ T_A ≤ +85°C
		—	25	34	µA	3.0	
		—	26	35	µA	5.0	
D012		—	210	440	µA	1.8	F_{OSC} = 4 MHz, XT Oscillator mode
		—	390	620	µA	3.0	
D012		—	320	530	µA	2.3	F_{OSC} = 4 MHz, XT Oscillator mode **(Note 5)**
		—	430	680	µA	3.0	
		—	530	790	µA	5.0	
D014		—	170	380	µA	1.8	F_{OSC} = 4 MHz, External Clock (ECM), Medium Power mode
		—	320	550	µA	3.0	
D014		—	250	513	µA	2.3	F_{OSC} = 4 MHz, External Clock (ECM), Medium Power mode
		—	360	645	µA	3.0	
		—	430	735	µA	5.0	
D015		—	2.5	3.8	mA	3.0	F_{OSC} = 32 MHz, External Clock (ECH), High-Power mode **(Note 5)**
		—	3.1	4.0	mA	3.6	
D015		—	2.5	4.3	mA	3.0	F_{OSC} = 32 MHz, External Clock (ECH), High-Power mode **(Note 5)**
		—	2.7	4.6	mA	5.0	

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD}; $\overline{MCLR}$ = V_{DD}; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For EXTRC oscillator configurations, current through R_{EXT} is not included. The current through the resistor can be extended by the formula $I_R = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in kΩ.

4: FVR and BOR are disabled.

5: 8 MHz crystal/oscillator with 4x PLL enabled.

TABLE 36-2: SUPPLY CURRENT (I_{DD})(1,2) (CONTINUED)

PIC16LF1777/8/9		Standard Operating Conditions (unless otherwise stated)					
PIC16F1777/8/9							
Param No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
						V_{DD}	Note
D017		—	115	190	μA	1.8	F_{OSC} = 500 kHz, MFINTOSC mode
		—	145	320	μA	3.0	
D017		—	160	215	μA	2.3	F_{OSC} = 500 kHz, MFINTOSC mode
		—	180	340	μA	3.0	
		—	230	420	μA	5.0	
D019		—	0.9	1.5	mA	1.8	F_{OSC} = 16 MHz, HFINTOSC mode
		—	1.5	2.3	mA	3.0	
D019		—	1.2	2.0	mA	2.3	F_{OSC} = 16 MHz, HFINTOSC mode
		—	1.5	2.5	mA	3.0	
		—	1.7	2.6	mA	5.0	
D020		—	2.9	4.2	mA	3.0	F_{OSC} = 32 MHz, HFINTOSC mode **(Note 5)**
		—	3.5	4.3	mA	3.6	
D020		—	2.9	4.2	mA	3.0	F_{OSC} = 32 MHz, HFINTOSC mode **(Note 5)**
		—	3.0	5.0	mA	5.0	
D022		—	2.8	4	mA	3.0	F_{OSC} = 32 MHz, HS Oscillator mode **(Note 5)**
		—	3.4	4.7	mA	3.6	
D022		—	2.9	4	mA	3.0	F_{OSC} = 32 MHz HS Oscillator mode **(Note 5)**
		—	3.1	4.5	mA	5.0	

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD}; $\overline{MCLR}$ = V_{DD}; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For EXTRC oscillator configurations, current through R_{EXT} is not included. The current through the resistor can be extended by the formula $I_R = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in kΩ.

4: FVR and BOR are disabled.

5: 8 MHz crystal/oscillator with 4x PLL enabled.

TABLE 36-4: I/O PORTS (CONTINUED) (CONTINUED)

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
		Capacitive Loading Specs on Output Pins					
D101*	COSC2	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101A*	CIO	All I/O pins	—	—	50	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in EXTRC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: Including OSC2 in CLKOUT mode.

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

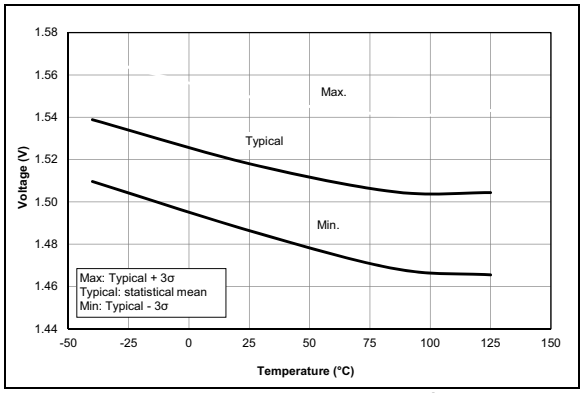


FIGURE 37-73: *POR Rearm Voltage, NP Mode (VREGPM1 = 0), PIC16F1773/6 Only.*

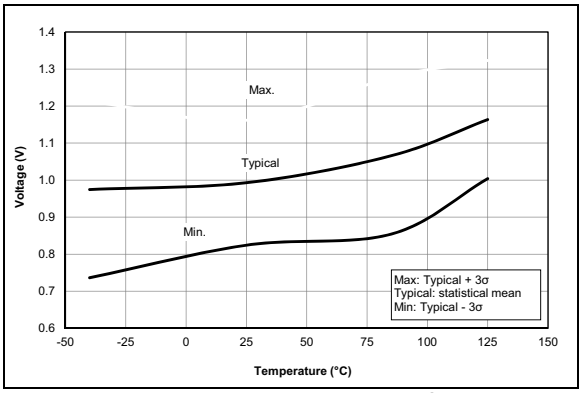


FIGURE 37-74: *POR Rearm Voltage, NP Mode, PIC16LF1777/8/9 Only.*

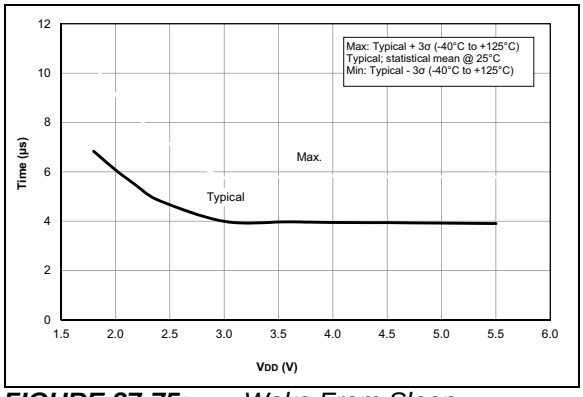


FIGURE 37-75: *Wake From Sleep, VREGPM = 0.*

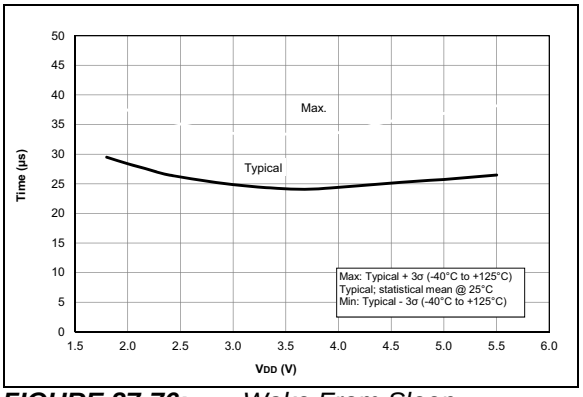


FIGURE 37-76: *Wake From Sleep, VREGPM = 1.*

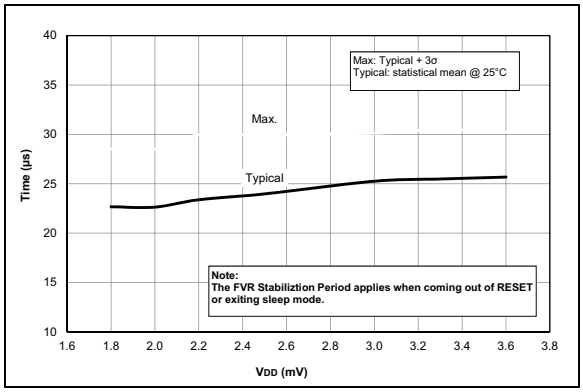


FIGURE 37-77: FVR Stabilization Period, *PIC16LF1777/8/9 Only.*

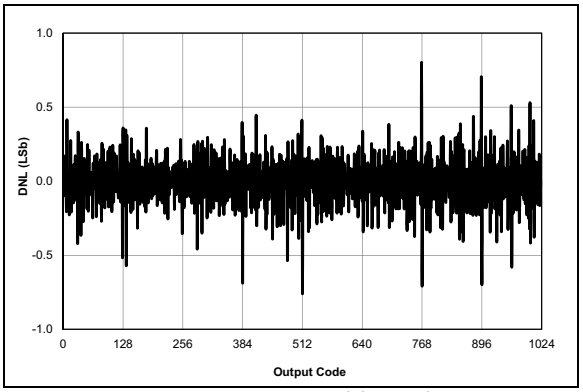


FIGURE 37-78: *ADC 10-bit Mode, Single-Ended DNL, V_{DD} = 3.0V, T_{AD} = 1 µS, 25°C.*