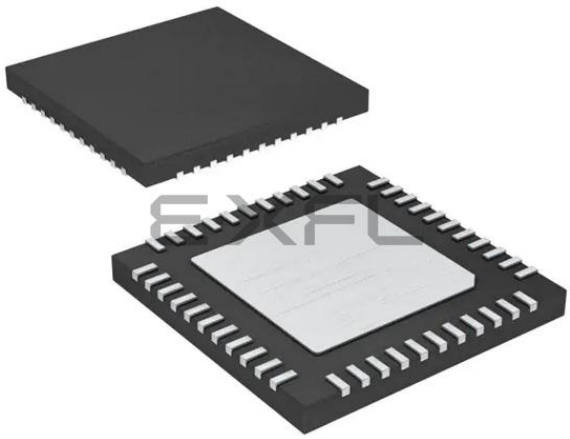
Microchip Technology - PIC16LF1777T-I/ML Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x10b; D/A 4x5b, 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1777t-i-ml

TABLE 1-2: PIC16(L)F1778 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB6/DAC5REF1+/DAC7REF1+/ C4IN1+/CLCIN2/ICSPCLK	RB6	TTL/ST	CMOS	General purpose I/O.
	DAC5REF1+	AN	—	DAC5 positive reference.
	DAC7REF1+	AN	—	DAC7 positive reference.
	C4IN1+	AN	—	Comparator 2 positive input.
	CLCIN2(1)	TTL/ST	—	CLC input 2.
	ICSPCLK	ST	—	Serial Programming Clock.
RB7/C5IN1+/DAC1OUT2/ DAC2OUT2/DAC3OUT2/ DAC4OUT2/DAC5OUT2/ DAC7OUT2/T6IN/CLCIN3/ ICSPDAT	RB7	TTL/ST	CMOS	General purpose I/O.
	C5IN1+	AN	—	Comparator 5 positive input.
	DAC1OUT2	—	AN	DAC1 voltage output.
	DAC2OUT2	—	AN	DAC2 voltage output.
	DAC3OUT2	—	AN	DAC3 voltage output.
	DAC4OUT2	—	AN	DAC4 voltage output.
	DAC5OUT2	—	AN	DAC5 voltage output.
	DAC7OUT2	—	AN	DAC7 voltage output.
	T6IN(1)	TTL/ST	—	Timer6 gate input.
	CLCIN3(1)	TTL/ST	—	CLC input 3.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RC0/DAC5OUT1/T1CKI/T3CKI/ T3G/SOSCO	RC0	TTL/ST	CMOS	General purpose I/O.
	DAC5OUT1	—	AN	DAC5 voltage output.
	T1CKI(1)	AN	—	Comparator 4 negative input.
	T3CKI(1)	TTL/ST	—	Timer3 clock input.
	T3G(1)	TTL/ST	—	Timer3 gate input.
	SOSCO	—	XTAL	Secondary oscillator output.
RC1/DAC7OUT1/PRG2R/CCP2/ SOSCI	RC1	TTL/ST	CMOS	General purpose I/O.
	DAC7OUT1	—	AN	DAC7 voltage output.
	PRG2R(1)	TTL/ST	—	Ramp generator set_rising input.
	CCP2(1)	TTL/ST	—	CCP2 capture input.
	SOSCI	XTAL	—	Secondary oscillator input.
RC2/AN14/C5IN2-/C6IN2-/ PRG2F/CCP1/T5CKI	RC2	TTL/ST	CMOS	General purpose I/O.
	AN14	AN	—	ADC Channel 14 input.
	C5IN2-	AN	—	Comparator 5 negative input.
	C6IN2-	AN	—	Comparator 6 negative input.
	PRG2F(1)	TTL/ST	—	Ramp generator set_falling input.
	CCP1(1)	TTL/ST	—	CCP1 capture input.
	T5CKI(1)	TTL/ST	—	Timer5 clock input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HP = High Power XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

3.4.5 CORE FUNCTION REGISTERS SUMMARY

The Core Function registers listed in Table 3-17 can be addressed from any Bank.

TABLE 3-17: CORE FUNCTION REGISTERS SUMMARY(1)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 0-31											
x00h or x80h	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
x01h or x81h	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
x02h or x82h	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
x03h or x83h	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
x04h or x84h	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
x05h or x85h	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
x06h or x86h	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
x07h or x87h	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
x08h or x88h	BSR	—	—	—	BSR4	BSR3	BSR2	BSR1	BSR0	---0 0000	---0 0000
x09h or x89h	WREG	Working Register								0000 0000	uuuu uuuu
x0Ah or x8Ah	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
x0Bh or x8Bh	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 14											
70Ch	—	Unimplemented								—	—
70Dh	COG2PHR	—	—	COG Rising Edge Phase Delay Count Register						--00 0000	--00 0000
70Eh	COG2PHF	—	—	COG Falling Edge Phase Delay Count Register						--00 0000	--00 0000
70Fh	COG2BLKR	—	—	COG Rising Edge Blanking Count Register						--00 0000	--00 0000
710h	COG2BLKF	—	—	COG Falling Edge Blanking Count Register						--00 0000	--00 0000
711h	COG2DBR	—	—	COG Rising Edge Dead-band Count Register						--00 0000	--00 0000
712h	COG2DBF	—	—	COG Falling Edge Dead-band Count Register						--00 0000	--00 0000
713h	COG2CON0	EN	LD	—	CS<1:0>		MD<2:0>			00-0 0000	00-0 0000
714h	COG2CON1	RDBS	FDBS	—	—	POLD	POLC	POLB	POLA	00-- 0000	00-- 0000
715h	COG2RIS0	RIS7	RIS6	RIS5	RIS4	RIS3	RIS2	RIS1	RIS0	0000 0000	0000 0000
716h	COG2RIS1	RIS15	RIS14	RIS13	RIS12	RIS11	RIS10	RIS9	RIS8	0000 0000	0000 0000
717h	COG2RSIM0	RSIM7	RSIM6	RSIM5	RSIM4	RSIM3	RSIM2	RSIM1	RSIM0	0000 0000	0000 0000
718h	COG2RSIM1	RSIM15	RSIM14	RSIM13	RSIM12	RSIM11	RSIM10	RSIM9	RSIM8	0000 0000	0000 0000
719h	COG2FIS0	FIS7	FIS6	FIS5	FIS4	FIS3	FIS2	FIS1	FIS0	0000 0000	0000 0000
71Ah	COG2FIS1	FIS15	FIS14	FIS13	FIS12	FIS11	FIS10	FIS9	FIS8	0000 0000	0000 0000
71Bh	COG2FSIM0	FSIM7	FSIM6	FSIM5	FSIM4	FSIM3	FSIM2	FSIM1	FSIM0	0000 0000	0000 0000
71Ch	COG2FSIM1	FSIM15	FSIM14	FSIM13	FSIM12	FSIM11	FSIM10	FSIM9	FSIM8	0000 0000	0000 0000
71Dh	COG2ASD0	ASE	ARSEN	ASDBD<1:0>		ASDAC<1:0>		—	—	0001 01--	0001 01--
71Eh	COG2ASD1	AS7E	AS6E	AS5E	AS4E	AS3E	AS2E	AS1E	AS0E	0000 0000	0000 0000
71Fh	COG2STR	SDATD	SDATC	SDATB	SDATA	STRD	STRC	STRB	STRA	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

REGISTER 4-2: CONFIG2: CONFIGURATION WORD 2

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
LVP(1)	$\overline{\text{DEBUG}}$(2)	$\overline{\text{LPBOR}}$	BORV(3)	STVREN	PLLEN
bit 13					bit 8

R/P-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1	R/P-1
$\overline{\text{ZCD}}$	—	—	—	—	PPS1WAY	WRT<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	-n = Value when blank or after Bulk Erase

bit 13 **LVP:** Low-Voltage Programming Enable bit(1)
- 1 = ON Low-voltage programming enabled
- 0 = OFF High-voltage on $\overline{\text{MCLR}}$ must be used for programming

bit 12 **$\overline{\text{DEBUG}}$:** In-Circuit Debugger Mode bit(2)
- 1 = OFF In-Circuit Debugger disabled, ICSPCLK and ICSPDAT are general purpose I/O pins
- 0 = ON In-Circuit Debugger enabled, ICSPCLK and ICSPDAT are dedicated to the debugger

bit 11 **$\overline{\text{LPBOR}}$:** Low-Power BOR Enable bit
- 1 = OFF Low-Power Brown-out Reset is disabled
- 0 = ON Low-Power Brown-out Reset is enabled

bit 10 **BORV:** Brown-out Reset Voltage Selection bit(3)
- 1 = LO Brown-out Reset voltage (V_{BOR}), low trip point selected
- 0 = HI Brown-out Reset voltage (V_{BOR}), high trip point selected

bit 9 **STVREN:** Stack Overflow/Underflow Reset Enable bit
- 1 = ON Stack Overflow or Underflow will cause a Reset
- 0 = OFF Stack Overflow or Underflow will not cause a Reset

bit 8 **PLLEN:** PLL Enable bit
- 1 = ON 4xPLL enabled
- 0 = OFF 4xPLL disabled

bit 7 **$\overline{\text{ZCD}}$:** ZCD Enable bit
- 1 = OFF ZCD disabled. ZCD can be enabled by setting the ZCDSEN bit of ZCDCON
- 0 = ON ZCD always enabled

bit 6-3 **Unimplemented:** Read as '1'

bit 2 **PPS1WAY**: PPSLOCK Bit One-Way Set Enable bit
- 1 = ON The PPSLOCK bit can only be set once after an unlocking sequence is executed; once PPSLOCK is set, all future changes to PPS registers are prevented
- 0 = OFF The PPSLOCK bit can be set and cleared as needed (provided an unlocking sequence is executed)

bit 1-0 **WRT<1:0>:** Flash Memory Self-Write Protection bits

4 kW Flash memory (PIC16(L)F1764/8)
- 11 = OFF Write protection off
- 10 = BOOT 0000h to 01FFh write protected, 0200h to 0FFFh may be modified by PMCON control
- 01 = HALF 0000h to 07FFh write protected, 0800h to 0FFFh may be modified by PMCON control
- 00 = ALL 0000h to 0FFFh write protected, no addresses may be modified by PMCON control

8 kW Flash memory (PIC16(L)F1765/9)
- 11 = OFF Write protection off
- 10 = BOOT 0000h to 01FFh write protected, 0200h to 1FFFh may be modified by PMCON control
- 01 = HALF 0000h to 0FFFh write protected, 1000h to 1FFFh may be modified by PMCON control
- 00 = ALL 0000h to 1FFFh write protected, no addresses may be modified by PMCON control

Note 1: The $\overline{\text{LVP}}$ bit cannot be programmed to '0' when Programming mode is entered via LVP.
2: The $\overline{\text{DEBUG}}$ bit in Configuration Words is managed automatically by device development tools including debuggers and programmers. For normal device operation, this bit should be maintained as a '1'.
3: See V_{BOR} parameter for specific trip point voltages.

TABLE 11-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	177
INLVLA	INLVLA7	INLVLA6	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	178
LATA	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	176
ODCONA	ODA7	ODA6	ODA5	ODA4	ODA3	ODA2	ODA1	ODA0	178
OPTION_REG	$\overline{\text{WPUEN}}$	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			274
PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	176
SLRCONA	SLRA7	SLRA6	SLRA5	SLRA4	SLRA3	SLRA2	SLRA1	SLRA0	178
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	176
WPUA	WPUA7	WPUA6	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	177

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

TABLE 11-3: SUMMARY OF CONFIGURATION WORD WITH PORTA

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	IESO	$\overline{\text{CLKOUTEN}}$	BOREN<1:0>		—	95
	7:0	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE<1:0>		FOSC<2:0>			

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by PORTA.

REGISTER 11-30: WPUD: WEAK PULL-UP PORTD REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
WPUD7	WPUD6	WPUD5	WPUD4	WPUD3	WPUD2	WPUD1	WPUD0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **WPUD<7:0>**: Weak Pull-up Register bits(1, 2)
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: Global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is configured as an output.

REGISTER 11-31: ODCOND: PORTD OPEN-DRAIN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ODD7	ODD6	ODD5	ODD4	ODD3	ODD2	ODD1	ODD0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ODD<7:0>:** PORTD Open-Drain Enable bits
For RD<7:0> pins
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

REGISTER 16-3: ADCON2: ADC CONTROL REGISTER 2

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	TRIGSEL<5:0>(1)					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **TRIGSEL<5:0>:** Auto-Conversion Trigger Selection bits(1)

101101 = PWM12 – OF12_match(2)
101100 = PWM12 – PH12_match(2)
101011 = PWM12 – PR12_match(2)
101010 = PWM12 – DC12_match(2)
101001 = PWM11 – OF11_match
101000 = PWM11 – PH11_match
100111 = PWM11 – PR11_match
100110 = PWM11 – DC11_match
100101 = PWM6 – OF6_match
100100 = PWM6 – PH6_match
100011 = PWM6 – PR6_match
100010 = PWM6 – DC6_match
100001 = PWM5 – PH5_match
100000 = PWM5 – PH5_match
011111 = PWM5 – PH5_match
011110 = PWM5 – PH5_match
011101 = PWM10 – PWM10OUT(2)
011100 = PWM9 – PWM9OUT
011011 = PWM4 – PWM4OUT
011010 = PWM3 – PWM3OUT
011001 = CCP8 – CCP8_trigger(2)
011000 = CCP7 – CCP7_trigger
010111 = CCP2 – CCP2_trigger
010110 = CCP1 – CCP1_trigger
010101 = CLC4 – LC4_out
010100 = CLC3 – LC3_out
010011 = CLC2 – LC2_out
010010 = CLC1 – LC1_out
010001 = Comparator C8 – sync_C8OUT(2)
010000 = Comparator C7 – sync_C7OUT(2)
001111 = Comparator C6 – sync_C6OUT
001110 = Comparator C5 – sync_C5OUT
001101 = Comparator C4 – sync_C4OUT
001100 = Comparator C3 – sync_C3OUT
001011 = Comparator C2 – sync_C2OUT
001010 = Comparator C1 – sync_C1OUT
001001 = Timer8 – T8_postscaled
001000 = Timer6 – T6_postscaled
000111 = Timer5 – T5_overflow
000110 = Timer4 – T4_postscaled
000101 = Timer3 – T3_overflow
000100 = Timer2 – T2_postscaled
000011 = Timer1 – T1_overflow
000010 = Timer0 – T0_overflow
000001 = ADCACT – ADCACTPPS Pin
000000 = No Auto-conversion Trigger selected

Note 1: This is a rising edge sensitive input for all sources.
2: PIC16(L)F1777/9 only.

REGISTER 16-6: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	—	—	—	ADRES<9:8>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-2 **Reserved**: Do not use.

bit 1-0 **ADRES<9:8>**: ADC Result Register bits
Upper two bits of 10-bit conversion result

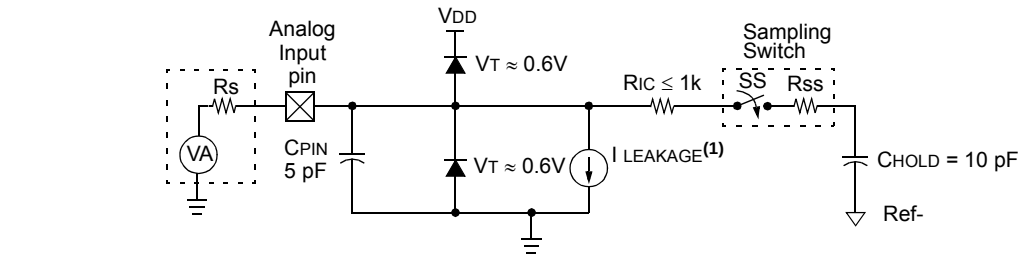
REGISTER 16-7: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1

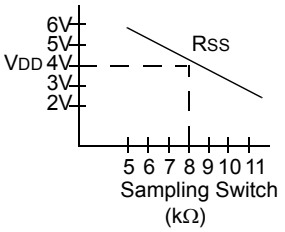
R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ADRES<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **ADRES<7:0>**: ADC Result Register bits
Lower eight bits of 10-bit conversion result

FIGURE 16-4: ANALOG INPUT MODEL



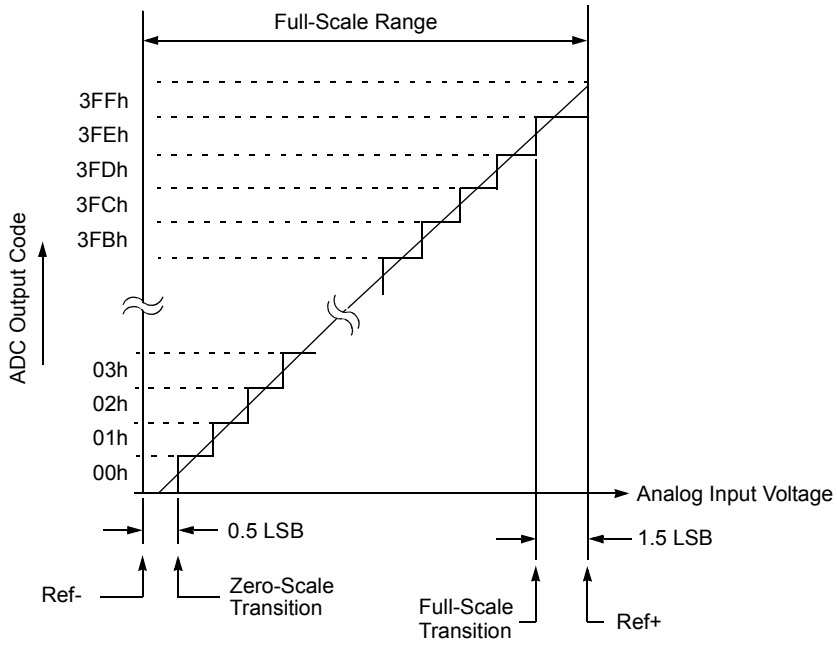


Legend:

CHOLD	= Sample/Hold Capacitance
CPIN	= Input Capacitance
I LEAKAGE	= Leakage current at the pin due to various junctions
RIC	= Interconnect Resistance
RSS	= Resistance of Sampling Switch
SS	= Sampling Switch
VT	= Threshold Voltage

Note 1: Refer to Table 36-4: I/O Ports (parameter D060).

FIGURE 16-5: ADC TRANSFER FUNCTION



17.6 Register Definitions: DAC Control

Long bit name prefixes for the 5-bit DAC peripherals are shown in Table 17-2. Refer to **Section 1.1 "Register and Bit naming conventions"** for more information

TABLE 17-2:

Peripheral	Bit Name Prefix
DAC3	DAC3
DAC4	DAC4
DAC7	DAC7
DAC8(1)	DAC8

Note 1: PIC16(L)F1777/9 only.

REGISTER 17-1: DACxCON0: DACx CONTROL REGISTER 0

R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0
EN	—	OE1	OE2	PSS<1:0>		NSS<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **EN:** DAC Enable bit
1 = DAC is enabled
0 = DAC is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **OE1:** DAC Voltage Output Enable bit
1 = DAC voltage level is also an output on the DACxOUT1 pin
0 = DAC voltage level is disconnected from the DACxOUT1 pin

bit 4 **OE2:** DAC Voltage Output Enable bit
1 = DAC voltage level is also an output on the DACxOUT2 pin
0 = DAC voltage level is disconnected from the DACxOUT2 pin

bit 3-2 **PSS<1:0>:** DAC Positive Source Select bits
11 = Reserved, do not use
10 = FVR Buffer2 output
01 = V_{REF+} pin
00 = V_{DD}

bit 1-0 **NSS<1:0>:** DAC Negative Source Select bits
11 = Reserved, do not use
10 = DACxREF1- (DAC7/8) or Reserved (DAC3/4)
01 = DACxREF0-
00 = AG_{ND} (AV_{SS})

REGISTER 18-2: DACxREFH: DAC REFERENCE VOLTAGE SELECT HIGH REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
REF<9:x> (x Depends on FM bit)							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

When FM = 1 (left justified)

bit 7-0 **REF<9:2>**: DAC Reference Voltage Output Select bits
DACxOUT1 = f(REF<9:0>) (See Equation 18-1)

When FM = 0 (right justified)

bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **REF<9:8>**: DAC Reference Voltage Output Select bits
DACxOUT1 = f(REF<9:0>) (See Equation 18-1)

REGISTER 18-3: DACxREFL: DAC REFERENCE VOLTAGE SELECT LOW REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
REF<x-1:0> (x Depends on FM bit)							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

When FM = 1 (left justified)

bit 7-6 **REF<1:0>**: DAC Reference Voltage Output Select bits
DACxOUT1 = f(REF<9:0>) (See Equation 18-1)

bit 5-0 **Unimplemented:** Read as '0'

When FM = 0 (right justified)

bit 7-0 **REF<7:0>**: DAC Reference Voltage Output Select bits
DACxOUT1 = f(REF<9:0>) (See Equation 18-1)

Note:	There are no long and short bit name variants for the following mirror register

REGISTER 19-5: CMOUT: COMPARATOR OUTPUT REGISTER

R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0
MC8OUT(1)	MC7OUT(1)	MC6OUT	MC5OUT	MC4OUT	MC3OUT	MC2OUT	MC1OUT
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **MC8OUT:** Mirror Copy of C8OUT bit(1)

bit 6 **MC7OUT:** Mirror Copy of C7OUT bit(1)

bit 5 **MC6OUT:** Mirror Copy of C6OUT bit

bit 4 **MC5OUT:** Mirror Copy of C5OUT bit

bit 3 **MC4OUT:** Mirror Copy of C4OUT bit

bit 2 **MC3OUT:** Mirror Copy of C3OUT bit

bit 1 **MC2OUT:** Mirror Copy of C2OUT bit

bit 0 **MC1OUT:** Mirror Copy of C1OUT bit

Note 1: PIC16LF1777/9 only.

REGISTER 27-12: COGxASD1: COG AUTO-SHUTDOWN CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
AS7E	AS6E	AS5E	AS4E	AS3E	AS2E	AS1E	AS0E
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-0 **AS<7:0>E:** Auto-shutdown Source <n> Enable bits(1). See Table 27-6.
1 = COGx is shutdown when source <n> output is low
0 = Source <n> has no effect on shutdown

Note 1: Any combination of <n> bits can be selected.

TABLE 27-6: AUTO-SHUTDOWN SOURCES

Bit <n>	COG1	COG2	COG3(2)	COG3(3)	COG4(2)
7	TMR4_postscaled(1)	TMR4_postscaled(1)	TMR8_postscaled(1)	TMR8_postscaled(1)	TMR8_postscaled(1)
6	TMR2_postscaled(1)	TMR2_postscaled(1)	TMR6_postscaled(1)	TMR6_postscaled(1)	TMR6_postscaled(1)
5	LC2_out	LC2_out	LC4_out	LC4_out	LC4_out
4	sync_CM4_out	sync_CM4_out	sync_CM8_out	sync_CM6_out	sync_CM8_out
3	sync_CM3_out	sync_CM3_out	sync_CM7_out	sync_CM5_out	sync_CM7_out
2	sync_CM2_out	sync_CM2_out	sync_CM6_out	sync_CM2_out	sync_CM6_out
1	sync_CM1_out	sync_CM1_out	sync_CM5_out	sync_CM1_out	sync_CM5_out
0	Pin selected by COG1PPS	Pin selected by COG2PPS	Pin selected by COG3PPS	Pin selected by COG3PPS	Pin selected by COG4PPS

Note 1: Shutdown when source is high.
2: PIC16(L)F1777/9 only.
3: PIC16(L)F1778 only.

28.0 CONFIGURABLE LOGIC CELL (CLC)

The Configurable Logic Cell (CLCx) provides programmable logic that operates outside the speed limitations of software execution. The logic cell takes up to 32 input signals and, through the use of configurable gates, reduces the 32 inputs to four logic lines that drive one of eight selectable single-output logic functions.

Input sources are a combination of the following:

- I/O pins
- Internal clocks
- Peripherals
- Register bits

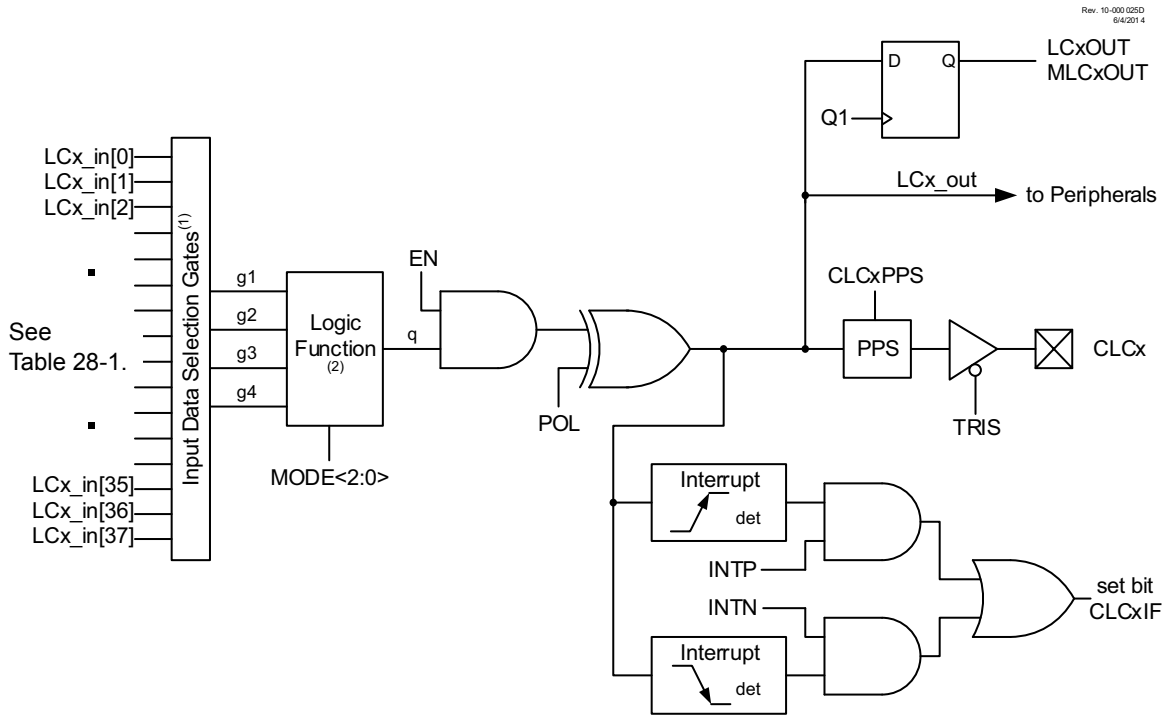
The output can be directed internally to peripherals and to an output pin.

Refer to Figure 28-1 for a simplified diagram showing signal flow through the CLCx.

Possible configurations include:

- Combinatorial Logic
  - AND
  - NAND
  - AND-OR
  - AND-OR-INVERT
  - OR-XOR
  - OR-XNOR
- Latches
  - S-R
  - Clocked D with Set and Reset
  - Transparent D with Set and Reset
  - Clocked J-K with Reset

FIGURE 28-1: CLCx SIMPLIFIED BLOCK DIAGRAM



Note 1: See Figure 28-2: Input Data Selection and Gating.
2: See Figure 28-3: Programmable Logic Functions.

32.6.13.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

a) A low level is sampled on SDA when SCL goes from low level to high level (Case 1).
b) SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data '1' (Case 2).

When the user releases SDA and the pin is allowed to float high, the BRG is loaded with SSPxADD and counts down to zero. The SCL pin is then deasserted and when sampled high, the SDA pin is sampled.

If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', Figure 32-36). If SDA is sampled high, the BRG is reloaded and begins counting. If SDA goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDA at exactly the same time.

If SCL goes from high-to-low before the BRG times out and SDA has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition, see Figure 32-37.

If, at the end of the BRG time-out, both SCL and SDA are still high, the SDA pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated Start condition is complete.

FIGURE 32-36: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

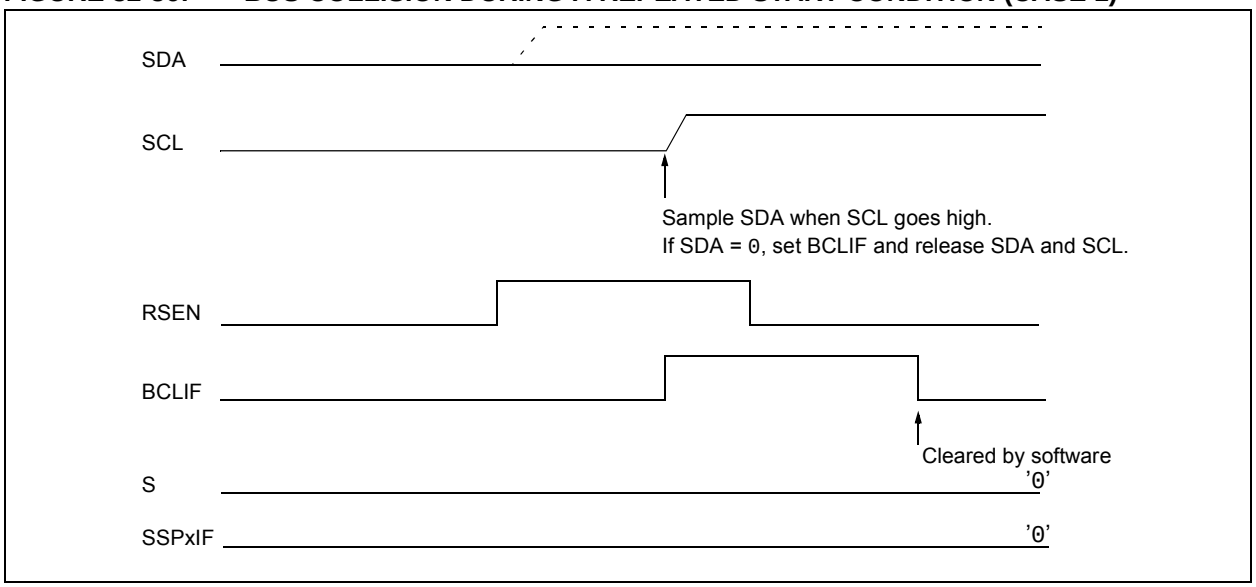


FIGURE 32-37: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)

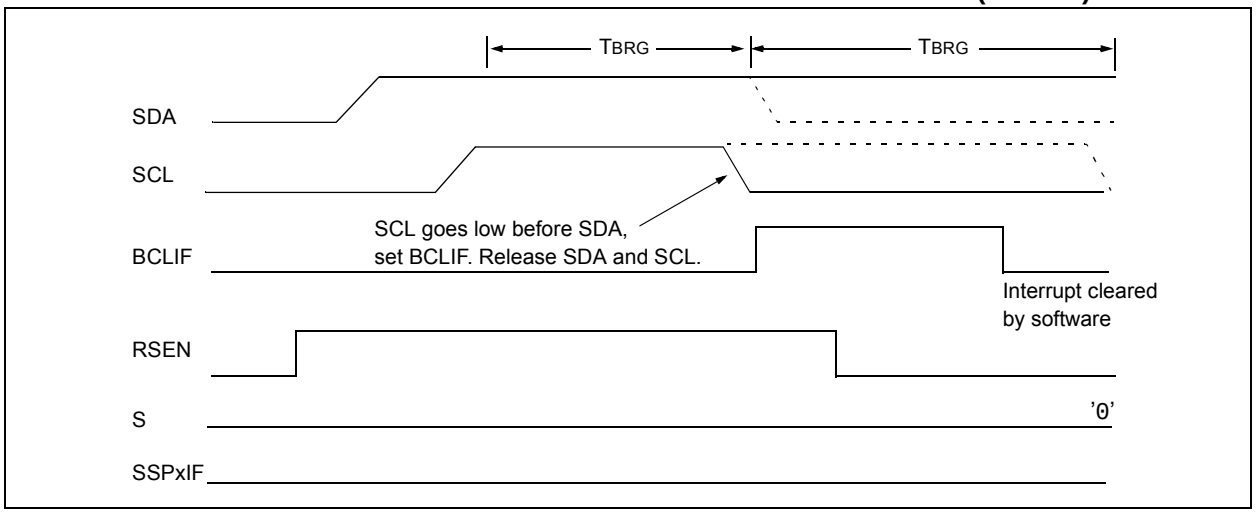


TABLE 32-3: SUMMARY OF REGISTERS ASSOCIATED WITH I^2C OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	177
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	182
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—	187
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	132
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	133
PIE2	OSFIE	C2IE	C1IE	COG1IE	BCL1IE	C4IE	C3IE	CCP2IE	134
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	139
PIR2	OSFIF	C2IF	C1IF	COG1IF	BCL1IF	C4IF	C3IF	CCP2IF	140
RxyPPS	—	—	RxyPPS<5:0>						205
SSPCLKPPS	—	—	SSPCLKPPS<5:0>						205, 207
SSPDATPPS	—	—	SSPDATPPS<5:0>						205, 207
SSPSSPPS	—	—	SSPSSPPS<5:0>						205, 207
SSP1ADD	ADD<7:0>								492
SSP1BUF	Synchronous Serial Port Receive Buffer/Transmit Register								444*
SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				489
SSP1CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	490
SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	491
SSP1MSK	MSK<7:0>								492
SSP1STAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	488
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	176
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	181
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	186

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by the MSSP module in I^2C mode.

* Page provides register information.

33.3 Register Definitions: EUSART Control

REGISTER 33-1: TX1STA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-1/1	R/W-0/0
CSRC	TX9	TXEN(1)	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **CSRC:** Clock Source Select bit
Asynchronous mode:
Don't care
Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

bit 6 **TX9:** 9-bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5 **TXEN:** Transmit Enable bit(1)
1 = Transmit enabled
0 = Transmit disabled

bit 4 **SYNC:** EUSART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3 **SENDB:** Send Break Character bit
Asynchronous mode:
1 = Send Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission completed
Synchronous mode:
Don't care

bit 2 **BRGH:** High Baud Rate Select bit
Asynchronous mode:
1 = High speed
0 = Low speed
Synchronous mode:
Unused in this mode

bit 1 **TRMT:** Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

bit 0 **TX9D:** Ninth bit of Transmit Data
Can be address/data bit or a parity bit.

Note 1: SREN/CREN overrides TXEN in Sync mode.

33.4.4 BREAK CHARACTER SEQUENCE

The EUSART module has the capability of sending the special Break character sequences that are required by the LIN bus standard. A Break character consists of a Start bit, followed by 12 '0' bits and a Stop bit.

To send a Break character, set the SENDB and TXEN bits of the TXxSTA register. The Break character transmission is then initiated by a write to the TXxREG. The value of data written to TXxREG will be ignored and all '0's will be transmitted.

The SENDB bit is automatically reset by hardware after the corresponding Stop bit is sent. This allows the user to preload the transmit FIFO with the next transmit byte following the Break character (typically, the Sync character in the LIN specification).

The TRMT bit of the TXxSTA register indicates when the transmit operation is active or idle, just as it does during normal transmission. See Figure 33-9 for the timing of the Break character sequence.

33.4.4.1 Break and Sync Transmit Sequence

The following sequence will start a message frame header made up of a Break, followed by an auto-baud Sync byte. This sequence is typical of a LIN bus master.

1. Configure the EUSART for the desired mode.
2. Set the TXEN and SENDB bits to enable the Break sequence.
3. Load the TXxREG with a dummy character to initiate transmission (the value is ignored).
4. Write '55h' to TXxREG to load the Sync character into the transmit FIFO buffer.
5. After the Break has been sent, the SENDB bit is reset by hardware and the Sync character is then transmitted.

When the TXxREG becomes empty, as indicated by the TXIF, the next data byte can be written to TXxREG.

33.4.5 RECEIVING A BREAK CHARACTER

The Enhanced EUSART module can receive a Break character in two ways.

The first method to detect a Break character uses the FERR bit of the RCxSTA register and the received data as indicated by RCxREG. The Baud Rate Generator is assumed to have been initialized to the expected baud rate.

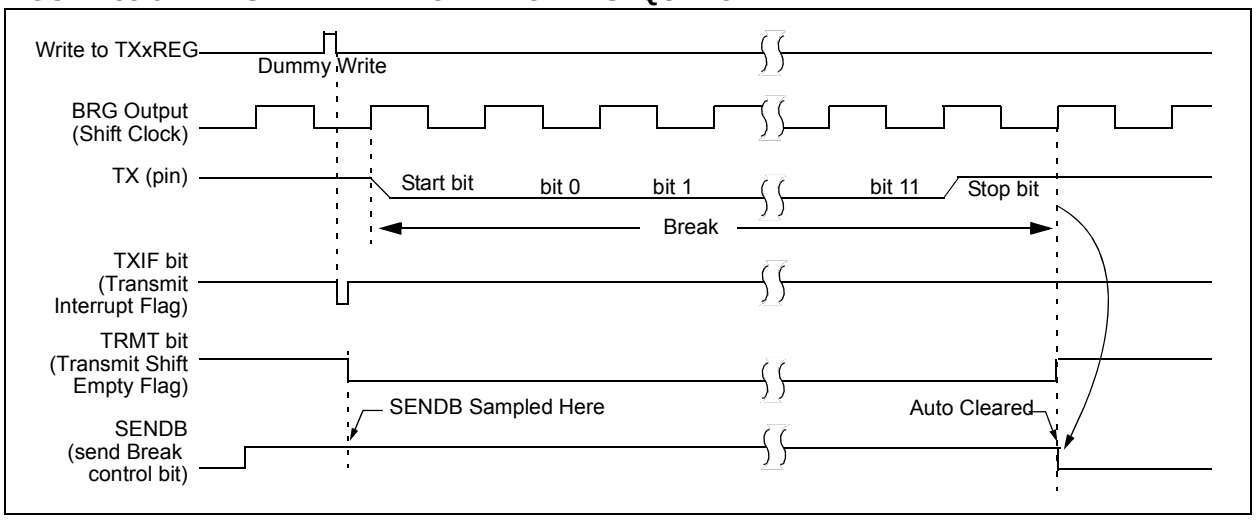
A Break character has been received when:

- RCIF bit is set
- FERR bit is set
- RCxREG = 00h

The second method uses the Auto-Wake-up feature described in **Section 33.4.3 "Auto-Wake-up on Break"**. By enabling this feature, the EUSART will sample the next two transitions on RX/DT, cause an RCIF interrupt, and receive the next data byte followed by another interrupt.

Note that following a Break character, the user will typically want to enable the Auto-Baud Detect feature. For both methods, the user can set the ABDEN bit of the BAUDxCON register before placing the EUSART in Sleep mode.

FIGURE 33-9: SEND BREAK CHARACTER SEQUENCE



38.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

38.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradeable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

38.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

38.9 PICkit 3 In-Circuit Debugger/ Programmer

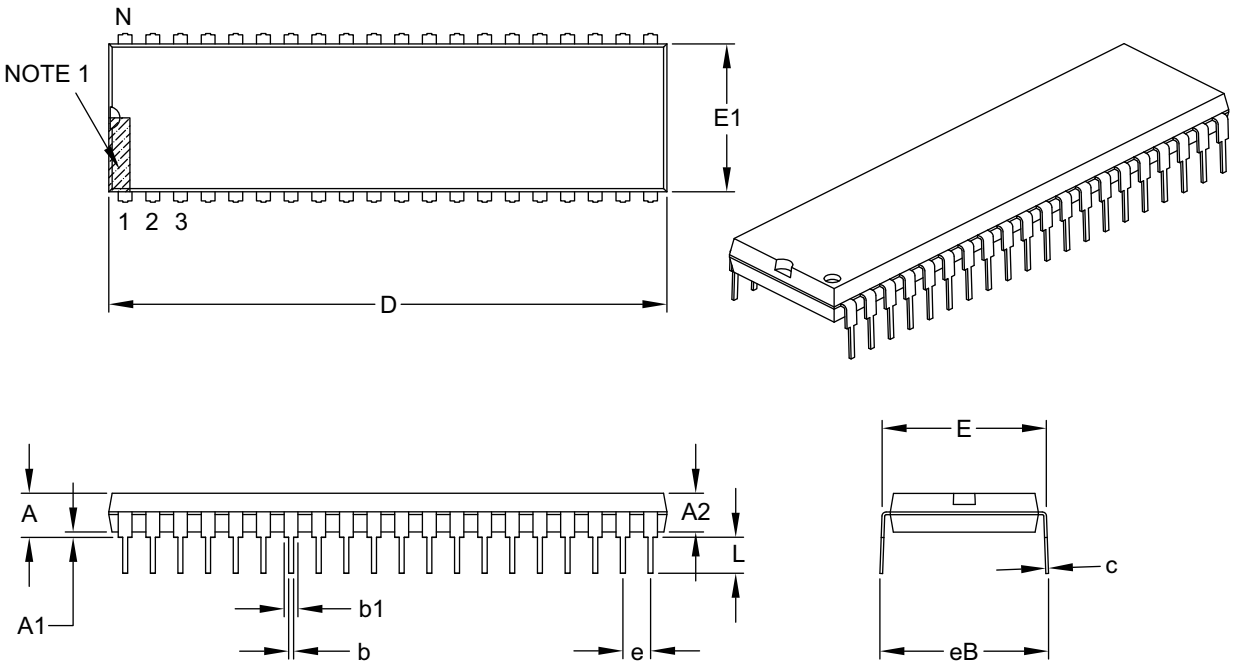
The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

38.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

40-Lead Plastic Dual In-Line (P) – 600 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		40	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.250
Molded Package Thickness	A2	.125	–	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.590	–	.625
Molded Package Width	E1	.485	–	.580
Overall Length	D	1.980	–	2.095
Tip to Seating Plane	L	.115	–	.200
Lead Thickness	c	.008	–	.015
Upper Lead Width	b1	.030	–	.070
Lower Lead Width	b	.014	–	.023
Overall Row Spacing §	eB	–	–	.700

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-016B