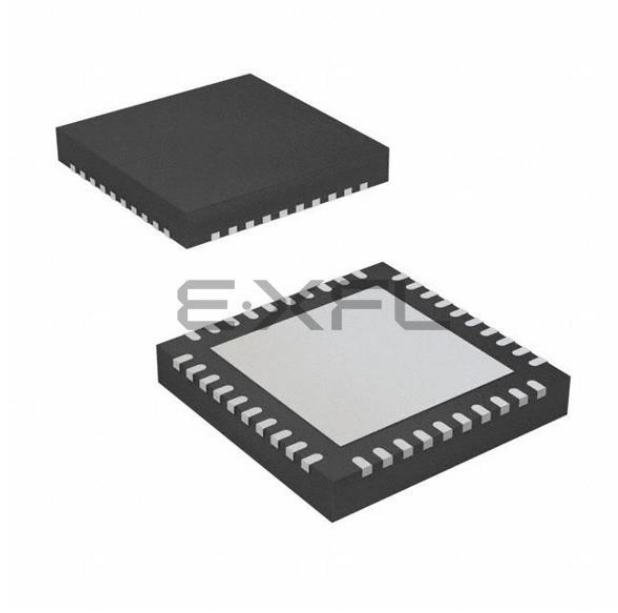

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x10b; D/A 4x5b, 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1777t-i-mv

TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 7											
38Ch	INLVLA	INLVLA7	INLVLA6	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	1111 1111	1111 1111
38Dh	INLVLB	INLVLB7	INLVLB6	INLVLB5	INLVLB4	INLVLB3	INLVLB2	INLVLB1	INLVLB0	1111 1111	1111 1111
38Eh	INLVLC	INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	1111 1111	1111 1111
38Fh	INLVLD(3)	INLVLD7	INLVLD6	INLVLD5	INLVLD4	INLVLD3	INLVLD2	INLVLD1	INLVLD0	1111 1111	1111 1111
390h	INLVLE(3)	—	—	—	—	INLVLE3	INLVLE2	INLVLE1	INLVLE0	---- 1111	---- 1111
391h	IOCAP	IOCAP7	IOCAP6	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	0000 0000	0000 0000
392h	IOCAN	IOCAN7	IOCAN6	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	0000 0000	0000 0000
393h	IOCAF	IOCAF7	IOCAF6	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	0000 0000	0000 0000
394h	IOCBP	IOCBP7	IOCBP6	IOCBP5	IOCBP4	IOCBP3	IOCBP2	IOCBP1	IOCBP0	0000 0000	0000 0000
395h	IOCBN	IOCBN7	IOCBN6	IOCBN5	IOCBN4	IOCBN3	IOCBN2	IOCBN1	IOCBN0	0000 0000	0000 0000
396h	IOCBF	IOCBF7	IOCBF6	IOCBF5	IOCBF4	IOCBF3	IOCBF2	IOCBF1	IOCBF0	0000 0000	0000 0000
397h	IOCCP	IOCCP7	IOCCP6	IOCCP5	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0	0000 0000	0000 0000
398h	IOCCN	IOCCN7	IOCCN6	IOCCN5	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0	0000 0000	0000 0000
399h	IOCCF	IOCCF7	IOCCF6	IOCCF5	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0	0000 0000	0000 0000
39Ah	—	Unimplemented								—	—
39Bh	—	Unimplemented								—	—
39Ch	—	Unimplemented								—	—
39Dh	IOCEP	—	—	—	—	IOCEP3	—	—	—	---- 0---	---- 0---
39Eh	IOCEN	—	—	—	—	IOCEN3	—	—	—	---- 0---	---- 0---
39Fh	IOCEF	—	—	—	—	IOCEF3	—	—	—	---- 0---	---- 0---

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

4.6 Device ID and Revision ID

The 14-bit device ID word is located at 8006h and the 14-bit revision ID is located at 8005h. These locations are read-only and cannot be erased or modified. See **Section 10.4 "User ID, Device ID and Configuration Word Access"** for more information on accessing these memory locations.

Development tools, such as device programmers and debuggers, may be used to read the Device ID and Revision ID.

4.7 Register Definitions: Device and Revision

REGISTER 4-3: DEVID: DEVICE ID REGISTER

R	R	R	R	R	R
DEV<13:8>					
bit 13					bit 8

R	R	R	R	R	R	R	R
DEV<7:0>							
bit 7							bit 0

Legend:	
R = Readable bit	
'1' = Bit is set	'0' = Bit is cleared

bit 13-0 **DEV<13:0>:** Device ID bits

Device	DEVID<13:0> Values
PIC16F1777	11 0000 1000 1110 (308E)
PIC16F1778	11 0000 1000 1111 (308F)
PIC16F1779	11 0000 1001 0000 (3090)
PIC16LF1777	11 0000 1001 0001 (3091)
PIC16LF1778	11 0000 1001 0010 (3092)
PIC16LF1779	11 0000 1001 0011 (3093)

TABLE 6-5: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BORCON	SBOREN	BORFS	—	—	—	—	—	BORRDY	121
PCON	STKOVF	STKUNF	—	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	125
STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	40
WDTCON	—	—	WDTPS<4:0>					SWDTEN	154

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Resets.

REGISTER 7-5: PIE4: PERIPHERAL INTERRUPT ENABLE REGISTER 4

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	TMR8IE	TMR5GIE	TMR5IE	TMR3GIE	TMR3IE	TMR6IE	TRM4IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **TMR8IE:** TMR8 to T8PR Match Interrupt Enable bit
1 = Enables the Timer8 to T8PR match interrupt
0 = Disables the Timer8 to T8PR match interrupt

bit 5 **TMR5GIE:** Timer5 Gate Interrupt Enable bit
1 = Enables the Timer5 gate acquisition interrupt
0 = Disables the Timer5 gate acquisition interrupt

bit 4 **TMR5IE:** TMR5 to Overflow Interrupt Enable bit
1 = Enables the Timer5 to T5PR match interrupt
0 = Disables the Timer5 to T5PR match interrupt

bit 3 **TMR3GIE:** Timer3 Gate Interrupt Enable bit
1 = Enables the Timer3 gate acquisition interrupt
0 = Disables the Timer3 gate acquisition interrupt

bit 2 **TMR3IE:** TMR3 to Overflow Interrupt Enable bit
1 = Enables the Timer3 to T3PR match interrupt
0 = Disables the Timer3 to T3PR match interrupt

bit 1 **TMR6IE:** TMR6 to T6PR Match Interrupt Enable bit
1 = Enables the Timer6 to T6PR match interrupt
0 = Disables the Timer6 to T6PR match interrupt

bit 0 **TMR4IE:** TMR4 to T4PR Match Interrupt Enable bit
1 = Enables the Timer4 to T4PR match interrupt
0 = Disables the Timer4 to T4PR match interrupt

10.2.2 FLASH MEMORY UNLOCK SEQUENCE

The unlock sequence is a mechanism that protects the Flash program memory from unintended self-write programming or erasing. The sequence must be executed and completed without interruption to successfully complete any of the following operations:

- Row Erase
- Load program memory write latches
- Write of program memory write latches to program memory
- Write of program memory write latches to User IDs

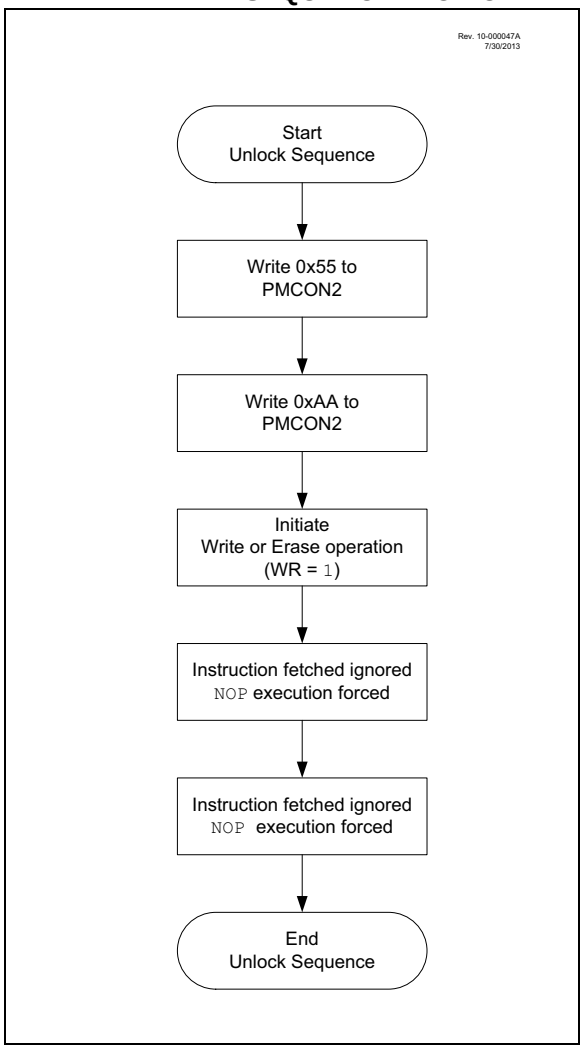
The unlock sequence consists of the following steps:

1. Write 55h to PMCON2
2. Write AAh to PMCON2
3. Set the WR bit in PMCON1
4. NOP instruction
5. NOP instruction

Once the WR bit is set, the processor will always force two NOP instructions. When an Erase Row or Program Row operation is being performed, the processor will stall internal operations (typical 2 ms), until the operation is complete and then resume with the next instruction. When the operation is loading the program memory write latches, the processor will always force the two NOP instructions and continue uninterrupted with the next instruction.

Since the unlock sequence must not be interrupted, global interrupts should be disabled prior to the unlock sequence and re-enabled after the unlock sequence is completed.

FIGURE 10-3: FLASH PROGRAM MEMORY UNLOCK SEQUENCE FLOWCHART



11.3 PORTB Registers

11.3.1 DATA REGISTER

PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB (Register 11-10). Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 11-1 shows how to initialize an I/O port.

Reading the PORTB register (Register 11-9) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATB).

11.3.2 DIRECTION CONTROL

The TRISB register (Register 11-10) controls the PORTB pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISB register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

11.3.3 OPEN-DRAIN CONTROL

The ODCONB register (Register 11-14) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONB bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCONB bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

11.3.4 SLEW RATE CONTROL

The SLRCONB register (Register 11-15) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONB bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONB bit is cleared, The corresponding port pin drive slews at the maximum rate possible.

11.3.5 INPUT THRESHOLD CONTROL

The INLVLB register (Register 11-16) controls the input voltage threshold for each of the available PORTB input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTB register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Table 36-4: I/O Ports for more information on threshold levels.

Note:	Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

11.3.6 ANALOG CONTROL

The ANSELB register (Register 11-12) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELB bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELB bits has no effect on digital output functions. A pin with TRIS clear and ANSELB set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELB bits default to the Analog mode after reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

11.3.7 PORTB FUNCTIONS AND OUTPUT PRIORITIES

Each pin defaults to the PORT latch data after reset. Other functions are selected with the peripheral pin select logic. See **Section 12.0 "Peripheral Pin Select (PPS) Module"** for more information. Analog input functions, such as ADC and op amp inputs, are not shown in the peripheral pin select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELB register. Digital output functions may continue to control the pin when it is in Analog mode.

11.3.8 HIGH CURRENT DRIVE CONTROL

The output drivers on RB1 and RB0 are capable of sourcing and sinking up to 100 mA. This extra drive capacity can be enabled and disabled with the control bits in the HIDRVB register (Register 11-17).

TABLE 11-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD(1)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELD	ANSD7	ANSD6	ANSD5	ANSD4	ANSD3	ANSD2	ANSD1	ANSD0	193
INLVLD	INLVLD7	INLVLD6	INLVLD5	INLVLD4	INLVLD3	INLVLD2	INLVLD1	INLVLD0	195
LATD	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	193
ODCOND	ODD7	ODD6	ODD5	ODD4	ODD3	ODD2	ODD1	ODD0	194
PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	195
SLRCOND	SLRD7	SLRD6	SLRD5	SLRD4	SLRD3	SLRD2	SLRD1	SLRD0	195
TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	192
WPUD	WPUD7	WPUD6	WPUD5	WPUD4	WPUD3	WPUD2	WPUD1	WPUD0	194

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTD.

Note 1: PIC16(L)F1777/9 only.

REGISTER 19-2: CMxCON1: COMPARATOR Cx CONTROL REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
—	—	—	—	—	—	INTP	INTN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **INTP:** Comparator Interrupt on Positive Going Edge Enable bits
1 = The CxIF interrupt flag will be set upon a positive going edge of the CxOUT bit
0 = No interrupt flag will be set on a positive going edge of the CxOUT bit

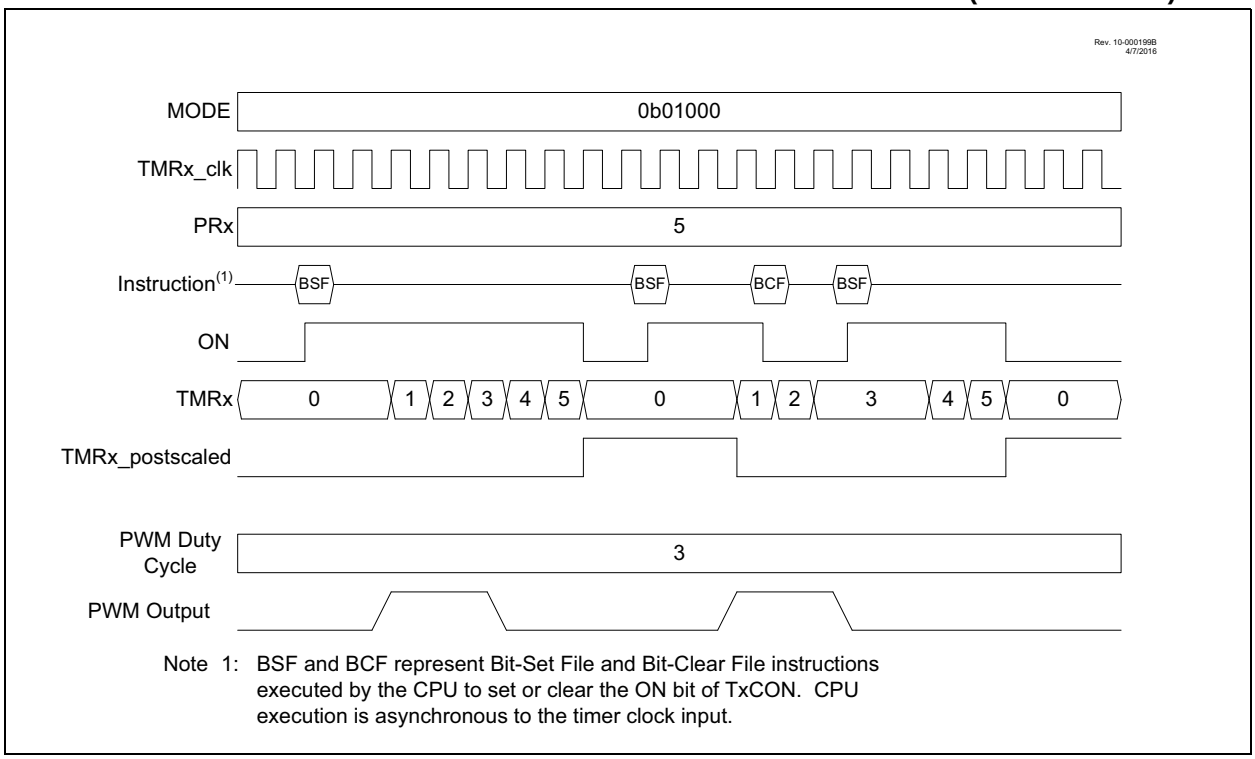
bit 0 **INTN:** Comparator Interrupt on Negative Going Edge Enable bits
1 = The CxIF interrupt flag will be set upon a negative going edge of the CxOUT bit
0 = No interrupt flag will be set on a negative going edge of the CxOUT bit

23.6.5 SOFTWARE START ONE-SHOT MODE

In One-Shot mode the timer resets and the ON bit is cleared when the timer value matches the PRx period value. The ON bit must be set by software to start another timer cycle. Setting MODE<4:0> = 01000 selects One-Shot mode which is illustrated in Figure 23-8. In the example, ON is controlled by BSF and BCF instructions. In the first case, a BSF instruction sets ON and the counter runs to completion and clears ON. In the second case, a BSF instruction starts the cycle, BCF/BSF instructions turn the counter off and on during the cycle, and then it runs to completion.

When One-Shot mode is used in conjunction with the CCP PWM operation the PWM pulse drive starts concurrent with setting the ON bit. Clearing the ON bit while the PWM drive is active will extend the PWM drive. The PWM drive will terminate when the timer value matches the CCPRx pulse width value. The PWM drive will remain off until software sets the ON bit to start another cycle. If software clears the ON bit after the CCPRx match but before the PRx match then the PWM drive will be extended by the length of time the ON bit remains cleared. Another timing cycle can only be initiated by setting the ON bit after it has been cleared by a PRx period count match.

FIGURE 23-8: SOFTWARE START ONE-SHOT MODE TIMING DIAGRAM (MODE = 01000)



Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

28.1 CLCx Setup

Programming the CLCx module is performed by configuring the four stages in the logic signal flow. The four stages are:

- Data selection
- Data gating
- Logic function selection
- Output polarity

Each stage is setup at run time by writing to the corresponding CLCx Special Function Registers. This has the added advantage of permitting logic reconfiguration on-the-fly during program execution.

28.1.1 DATA SELECTION

There are 32 signals available as inputs to the configurable logic. Four 32-input multiplexers are used to select the inputs to pass on to the next stage.

Data selection is through four multiplexers as indicated on the left side of Figure 28-2. Data inputs in the figure are identified by a generic numbered input name.

Table 28-1 correlates the generic input name to the actual signal for each CLC module. The column labeled dy indicates the MUX selection code for the selected data input. DxS is an abbreviation for the MUX select input codes: D1S<4:0> through D4S<4:0>.

Data inputs are selected with the CLCxSEL0 through CLCxSEL3 registers (Register 28-3 through Register 28-6).

Note:	Data selections are undefined at power-up.

TABLE 28-1: CLCx DATA INPUT SELECTION

Data Input	dy DxS	CLCx
LCx_in[54]	110110	MD1_OUT OR MD2_OUT OR MD3_OUT
LCx_in[53]	110101	FOSC
LCx_in[52]	110100	HFINTOSC
LCx_in[51]	110011	LFINTOSC
LCx_in[50]	110010	FRC (ADC RC clock)
LCx_in[49]	110001	IOCIF set
LCx_in[48]	110000	Timer8_postscaled
LCx_in[47]	101111	Timer6_postscaled
LCx_in[46]	101110	Timer4_postscaled
LCx_in[45]	101101	Timer2_postscaled
LCx_in[44]	101100	Timer5 overflow
LCx_in[43]	101011	Timer3 overflow
LCx_in[42]	101010	Timer1 overflow
LCx_in[41]	101001	Timer0 overflow
LCx_in[40]	101000	EUSART RX
LCx_in[39]	100111	EUSART TX
LCx_in[38]	100110	ZCD1_output
LCx_in[37]	100101	MSSP1 SDO/SDA
LCx_in[36]	100100	MSSP1 SCL/SCK

TABLE 28-1: CLCx DATA INPUT SELECTION

Data Input	dy DxS	CLCx
LCx_in[35]	100011	PWM12_out(1)
LCx_in[34]	100010	PWM11_out
LCx_in[33]	100001	PWM6_out
LCx_in[32]	100000	PWM5_out
LCx_in[31]	011111	PWM10_out(1)
LCx_in[30]	011110	PWM9_out
LCx_in[29]	011101	PWM4_out
LCx_in[28]	011100	PWM3_out
LCx_in[27]	011011	CCP8_out(1)
LCx_in[26]	011010	CCP7_out
LCx_in[25]	011001	CCP2_out
LCx_in[24]	011000	CCP1_out
LCx_in[23]	010111	COG4B(1)
LCx_in[22]	010110	COG4A(1)
LCx_in[21]	010101	COG3B
LCx_in[20]	010100	COG3A
LCx_in[19]	010011	COG2B
LCx_in[18]	010010	COG2A
LCx_in[17]	010001	COG1B
LCx_in[16]	010000	COG1A
LCx_in[15]	001111	sync_C8OUT(1)
LCx_in[14]	001110	sync_C7OUT(1)
LCx_in[13]	001101	sync_C6OUT
LCx_in[12]	001100	sync_C5OUT
LCx_in[11]	001011	sync_C4OUT
LCx_in[10]	001010	sync_C3OUT
LCx_in[9]	001001	sync_C2OUT
LCx_in[8]	001000	sync_C1OUT
LCx_in[7]	000111	LC4_out from the CLC4
LCx_in[6]	000110	LC3_out from the CLC3
LCx_in[5]	000101	LC2_out from the CLC2
LCx_in[4]	000100	LC1_out from the CLC1
LCx_in[3]	000011	CLCIN3 pin input selected in CLCIN3PPS register
LCx_in[2]	000010	CLCIN2 pin input selected in CLCIN2PPS register
LCx_in[1]	000001	CLCIN1 pin input selected in CLCIN1PPS register
LCx_in[0]	000000	CLCIN0 pin input selected in CLCIN0PPS register

Note 1: PIC16(L)F1777/9 only.

REGISTER 28-2: CLCxPOL: SIGNAL POLARITY CONTROL REGISTER

R/W-0/0	U-0	U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
POL	—	—	—	G4POL	G3POL	G2POL	G1POL
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **POL:** LCOUT Polarity Control bit
1 = The output of the logic cell is inverted
0 = The output of the logic cell is not inverted

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **G4POL:** Gate 4 Output Polarity Control bit
1 = The output of gate 4 is inverted when applied to the logic cell
0 = The output of gate 4 is not inverted

bit 2 **G3POL:** Gate 3 Output Polarity Control bit
1 = The output of gate 3 is inverted when applied to the logic cell
0 = The output of gate 3 is not inverted

bit 1 **G2POL:** Gate 2 Output Polarity Control bit
1 = The output of gate 2 is inverted when applied to the logic cell
0 = The output of gate 2 is not inverted

bit 0 **G1POL:** Gate 1 Output Polarity Control bit
1 = The output of gate 1 is inverted when applied to the logic cell
0 = The output of gate 1 is not inverted

REGISTER 28-11: CLCDATA: CLC DATA OUTPUT

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	MLC4OUT	MLC3OUT	MLC2OUT	MLC1OUT
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4	Unimplemented: Read as ‘0’
bit 3	MLC4OUT: Mirror copy of LC4OUT bit
bit 2	MLC3OUT: Mirror copy of LC3OUT bit
bit 1	MLC2OUT: Mirror copy of LC2OUT bit
bit 0	MLC1OUT: Mirror copy of LC1OUT bit

32.6.10 SLEEP OPERATION

While in Sleep mode, the I^2C slave module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSP interrupt is enabled).

32.6.11 EFFECTS OF A RESET

A Reset disables the MSSP module and terminates the current transfer.

32.6.12 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I^2C bus may be taken when the P bit of the SSPxSTAT register is set, or the bus is Idle, with both the S and P bits clear. When the bus is busy, enabling the SSP interrupt will generate the interrupt when the Stop condition occurs.

In multi-master operation, the SDA line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed by hardware with the result placed in the BCLIF bit.

The states where arbitration can be lost are:

- Address Transfer
- Data Transfer
- A Start Condition
- A Repeated Start Condition
- An Acknowledge Condition

32.6.13 MULTI -MASTER COMMUNICATION, BUS COLLISION AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, arbitration takes place when the master outputs a '1' on SDA, by letting SDA float high and another master asserts a '0'. When the SCL pin floats high, data should be stable. If the expected data on SDA is a '1' and the data sampled on the SDA pin is '0', then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCLIF and reset the I^2C port to its Idle state (Figure 32-32).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDA and SCL lines are deasserted and the SSPxBUF can be written to. When the user services the bus collision Interrupt Service Routine and if the I^2C bus is free, the user can resume communication by asserting a Start condition.

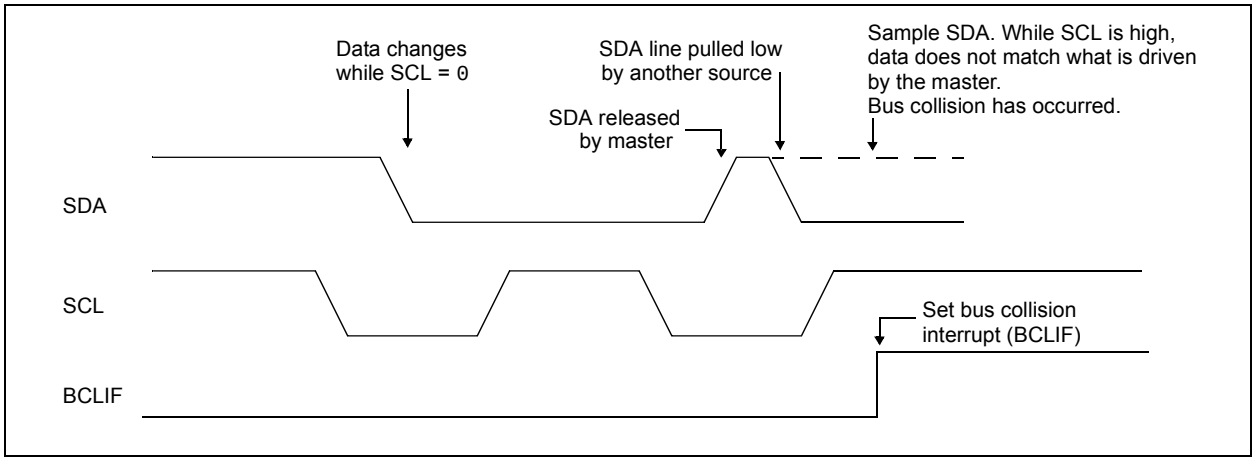
If a Start, Repeated Start, Stop or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDA and SCL lines are deasserted and the respective control bits in the SSPxCON2 register are cleared. When the user services the bus collision Interrupt Service Routine and if the I^2C bus is free, the user can resume communication by asserting a Start condition.

The master will continue to monitor the SDA and SCL pins. If a Stop condition occurs, the SSPxIF bit will be set.

A write to the SSPxBUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of Start and Stop conditions allows the determination of when the bus is free. Control of the I^2C bus can be taken when the P bit is set in the SSPxSTAT register, or the bus is Idle and the S and P bits are cleared.

FIGURE 32-32: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE



32.7 BAUD RATE GENERATOR

The MSSP module has a Baud Rate Generator available for clock generation in both I^2C and SPI Master modes. The Baud Rate Generator (BRG) reload value is placed in the SSPxADD register (Register 32-6). When a write occurs to SSPxBUF, the Baud Rate Generator will automatically begin counting down.

Once the given operation is complete, the internal clock will automatically stop counting and the clock pin will remain in its last state.

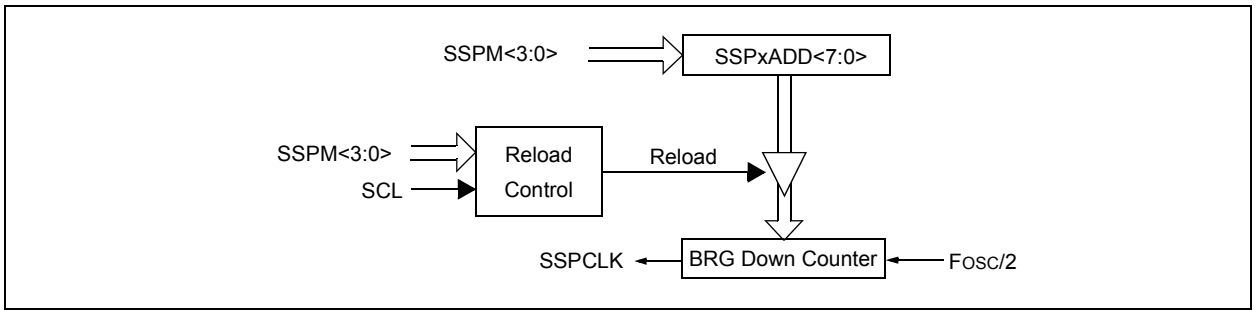
An internal signal “Reload” in Figure 32-40 triggers the value from SSPxADD to be loaded into the BRG counter. This occurs twice for each oscillation of the module clock line. The logic dictating when the reload signal is asserted depends on the mode the MSSP is being operated in.

Table 32-4 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSPxADD.

EQUATION 32-1:

$$F_{CLOCK} = \frac{F_{OSC}}{(SSPxADD + 1)(4)}$$

FIGURE 32-40: BAUD RATE GENERATOR BLOCK DIAGRAM



Note: Values of 0x00, 0x01 and 0x02 are not valid for SSPxADD when used as a Baud Rate Generator for I^2C. This is an implementation limitation.

TABLE 32-4: MSSP CLOCK RATE W/BRG

FOSC	FCY	BRG Value	FCLOCK (2 Rollovers of BRG)
32 MHz	8 MHz	13h	400 kHz
32 MHz	8 MHz	19h	308 kHz
32 MHz	8 MHz	4Fh	100 kHz
16 MHz	4 MHz	09h	400 kHz
16 MHz	4 MHz	0Ch	308 kHz
16 MHz	4 MHz	27h	100 kHz
4 MHz	1 MHz	09h	100 kHz

Note: Refer to the I/O port electrical specifications in Table 36-10 and Figure 32-7 to ensure the system is designed to support I/O requirements.

33.4.4 BREAK CHARACTER SEQUENCE

The EUSART module has the capability of sending the special Break character sequences that are required by the LIN bus standard. A Break character consists of a Start bit, followed by 12 '0' bits and a Stop bit.

To send a Break character, set the SENDB and TXEN bits of the TXxSTA register. The Break character transmission is then initiated by a write to the TXxREG. The value of data written to TXxREG will be ignored and all '0's will be transmitted.

The SENDB bit is automatically reset by hardware after the corresponding Stop bit is sent. This allows the user to preload the transmit FIFO with the next transmit byte following the Break character (typically, the Sync character in the LIN specification).

The TRMT bit of the TXxSTA register indicates when the transmit operation is active or idle, just as it does during normal transmission. See Figure 33-9 for the timing of the Break character sequence.

33.4.4.1 Break and Sync Transmit Sequence

The following sequence will start a message frame header made up of a Break, followed by an auto-baud Sync byte. This sequence is typical of a LIN bus master.

1. Configure the EUSART for the desired mode.
2. Set the TXEN and SENDB bits to enable the Break sequence.
3. Load the TXxREG with a dummy character to initiate transmission (the value is ignored).
4. Write '55h' to TXxREG to load the Sync character into the transmit FIFO buffer.
5. After the Break has been sent, the SENDB bit is reset by hardware and the Sync character is then transmitted.

When the TXxREG becomes empty, as indicated by the TXIF, the next data byte can be written to TXxREG.

33.4.5 RECEIVING A BREAK CHARACTER

The Enhanced EUSART module can receive a Break character in two ways.

The first method to detect a Break character uses the FERR bit of the RCxSTA register and the received data as indicated by RCxREG. The Baud Rate Generator is assumed to have been initialized to the expected baud rate.

A Break character has been received when:

- RCIF bit is set
- FERR bit is set
- RCxREG = 00h

The second method uses the Auto-Wake-up feature described in **Section 33.4.3 "Auto-Wake-up on Break"**. By enabling this feature, the EUSART will sample the next two transitions on RX/DT, cause an RCIF interrupt, and receive the next data byte followed by another interrupt.

Note that following a Break character, the user will typically want to enable the Auto-Baud Detect feature. For both methods, the user can set the ABDEN bit of the BAUDxCON register before placing the EUSART in Sleep mode.

FIGURE 33-9: SEND BREAK CHARACTER SEQUENCE

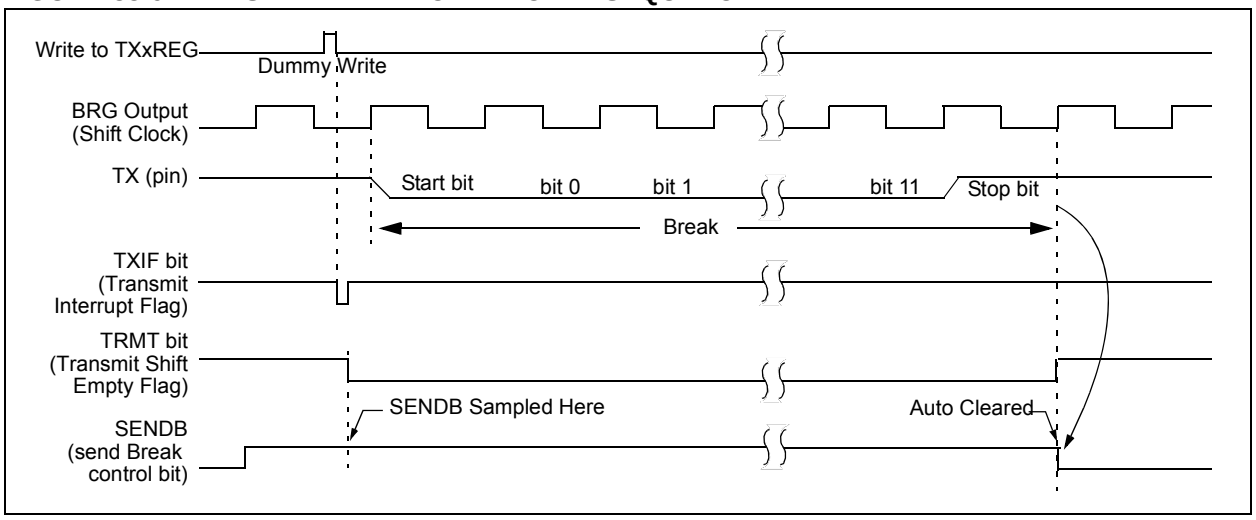
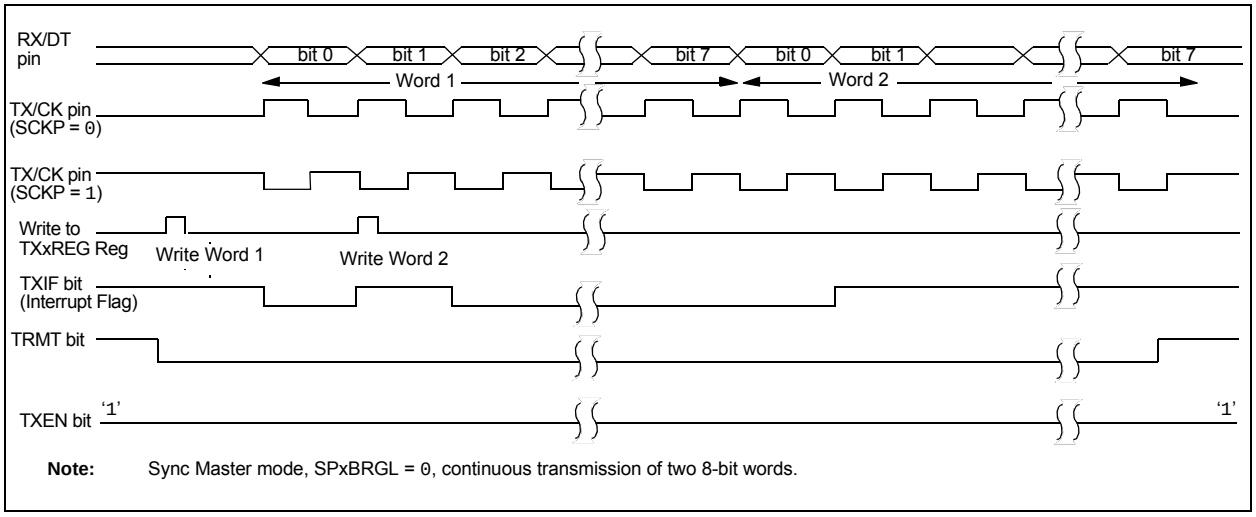


FIGURE 33-10: SYNCHRONOUS TRANSMISSION



Note: Sync Master mode, SPxBRGL = 0, continuous transmission of two 8-bit words.

FIGURE 33-11: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)

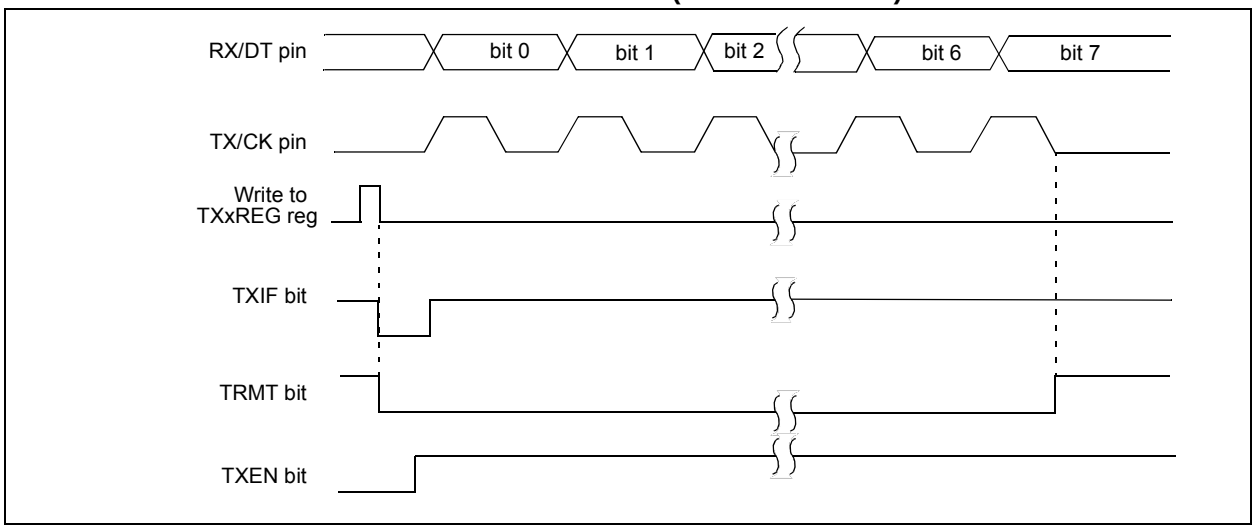


TABLE 36-3: POWER-DOWN CURRENTS (I_{PD})(1,2)

PIC16LF1777/8/9		Operating Conditions: (unless otherwise stated) Low-Power Sleep Mode						
PIC16F1777/8/9		Low-Power Sleep Mode, VREGPM = 1						
Param No.	Device Characteristics	Min.	Typ†	Max. +85°C	Max. +125°C	Units	Conditions	
							V_{DD}	Note
D023	Base I_{PD}	—	0.05	1.0	8.0	µA	1.8	WDT, BOR, FVR, and SOSC disabled, all Peripherals Inactive
		—	0.08	2.0	9.0	µA	3.0	
D023	Base I_{PD}	—	0.3	2.4	10	µA	2.3	WDT, BOR, FVR, and SOSC disabled, all Peripherals Inactive, Low-Power Sleep mode
		—	0.4	4	12	µA	3.0	
		—	0.5	6	15	µA	5.0	
D023A	Base I_{PD}	—	9.8	17	28	µA	2.3	WDT, BOR, FVR and SOSC disabled, all Peripherals inactive, Normal Power Sleep mode VREGPM = 0
		—	10.3	20	40	µA	3.0	
		—	11.5	22	44	µA	5.0	
D024		—	0.5	6	14	µA	1.8	WDT Current
		—	0.8	7	17	µA	3.0	
D024		—	0.8	6	15	µA	2.3	WDT Current
		—	0.9	7	20	µA	3.0	
		—	1.0	8	22	µA	5.0	
D025		—	15	28	30	µA	1.8	FVR Current (ADC)
		—	24	35	38	µA	3.0	
D025		—	18	33	35	µA	2.3	FVR Current (ADC)
		—	24	35	40	µA	3.0	
		—	26	37	44	µA	5.0	
D025A		—	25	50	55	µA	1.8	FVR Current (DAC)
		—	30	65	70	µA	3.0	
D025A		—	30	55	66	µA	2.3	FVR Current (DAC)
		—	32	68	82	µA	3.0	
		—	35	77	90	µA	5.0	
D026		—	7.5	25	28	µA	3.0	BOR Current
D026		—	10	25	28	µA	3.0	BOR Current
		—	12	28	31	µA	5.0	
D027		—	0.5	4	10	µA	3.0	LPBOR Current
D027		—	0.8	6	15	µA	3.0	LPBOR Current
		—	1	8	17	µA	5.0	
D028		—	0.5	5	9	µA	1.8	SOSC Current
		—	0.8	8.5	12	µA	3.0	
D028		—	1.1	6	10	µA	2.3	SOSC Current
		—	1.3	8.5	20	µA	3.0	
		—	1.4	10	25	µA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base I_{PD} and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base I_{DD} or I_{PD} current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{SS}.

3: ADC clock source is FRC.

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

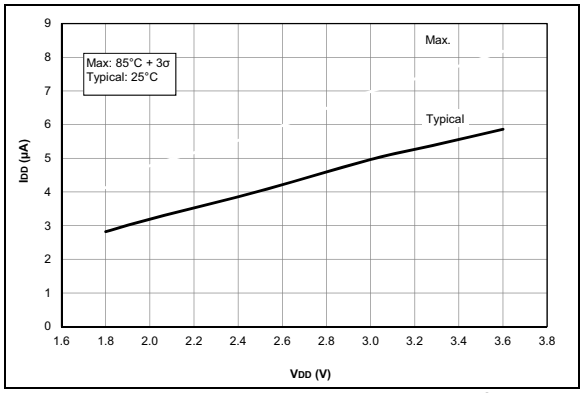


FIGURE 37-19: *IDD, LFINTOSC Mode, Fosc = 31 kHz, PIC16LF1777/8/9 Only.*

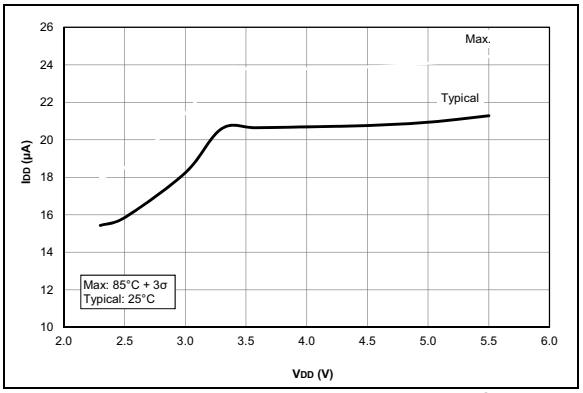


FIGURE 37-20: *IDD, LFINTOSC Mode, Fosc = 31 kHz, PIC16F1777/8/9 Only.*

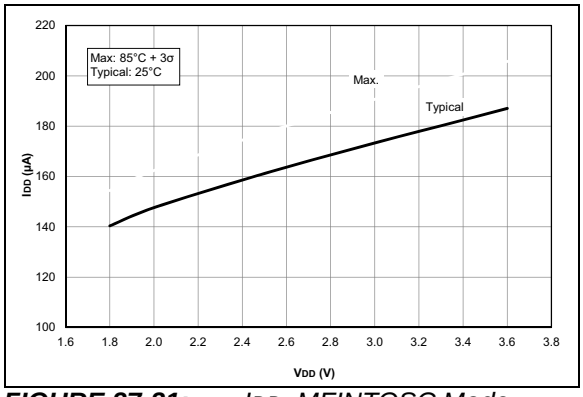


FIGURE 37-21: *IDD, MFINTOSC Mode, Fosc = 500 kHz, PIC16LF1777/8/9 Only.*

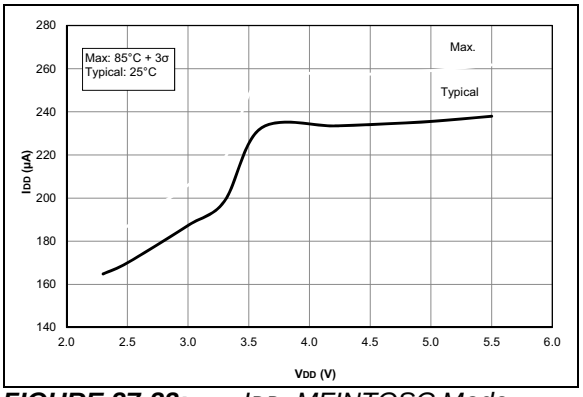


FIGURE 37-22: *IDD, MFINTOSC Mode, Fosc = 500 kHz, PIC16F1777/8/9 Only.*

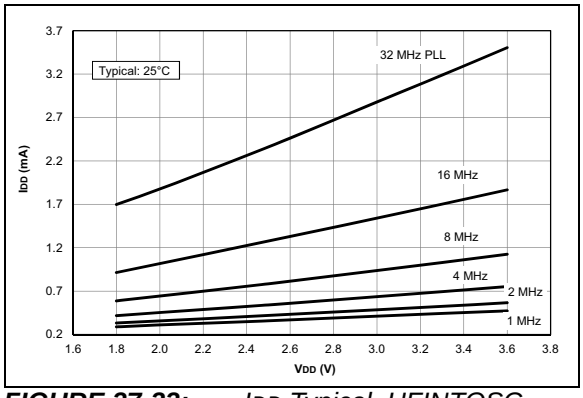


FIGURE 37-23: *IDD Typical, HFINTOSC Mode, PIC16LF1777/8/9 Only.*

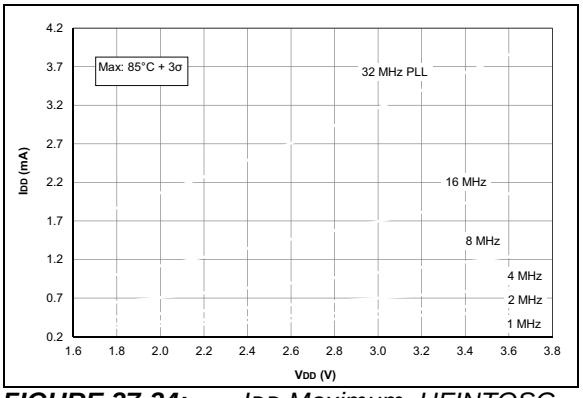


FIGURE 37-24: *IDD Maximum, HFINTOSC Mode, PIC16LF1777/8/9 Only.*

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

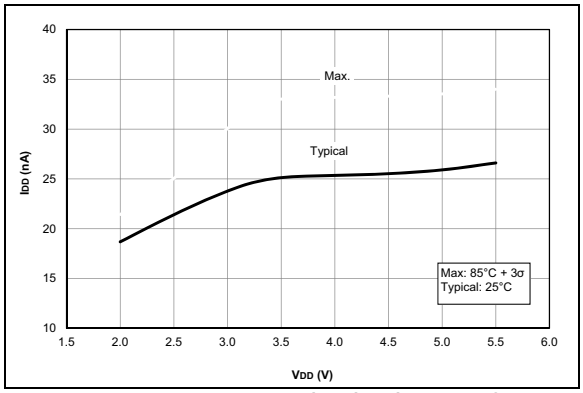


FIGURE 37-37: *IPD, Fixed Voltage Reference (FVR), ADC, PIC16F1777/8/9 Only.*

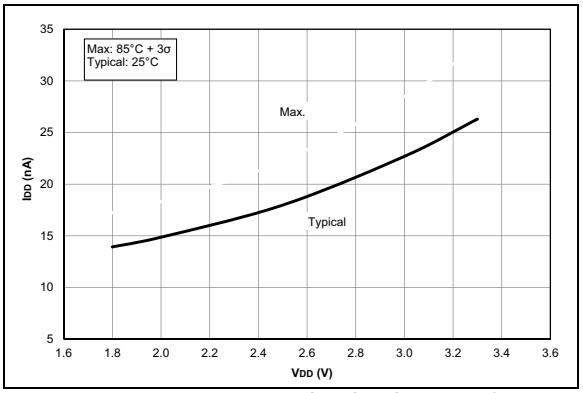


FIGURE 37-38: *IPD, Fixed Voltage Reference (FVR), DAC/Comparator, PIC16LF1777/8/9 Only.*

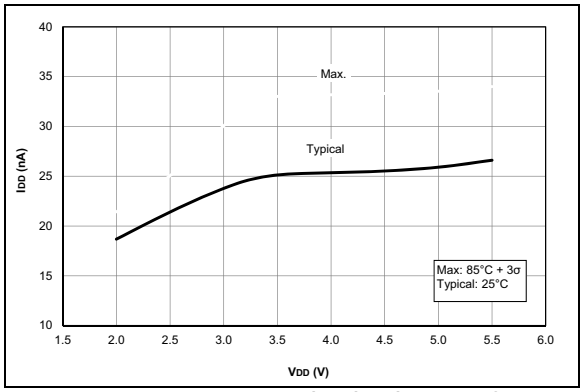


FIGURE 37-39: *IPD, Fixed Voltage Reference (FVR), DAC/Comparator, PIC16F1777/8/9 Only.*

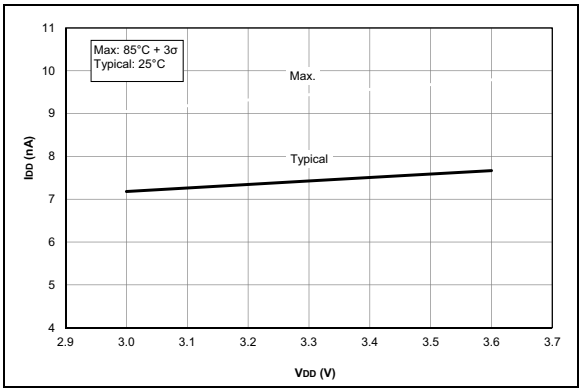


FIGURE 37-40: *IPD, Brown-Out Reset (BOR), BORV = 1, PIC16LF1777/8/9 Only.*

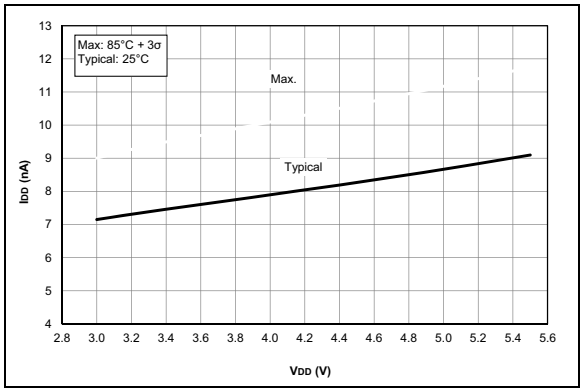


FIGURE 37-41: *IPD, Brown-Out Reset (BOR), BORV = 1, PIC16F1777/8/9 Only.*

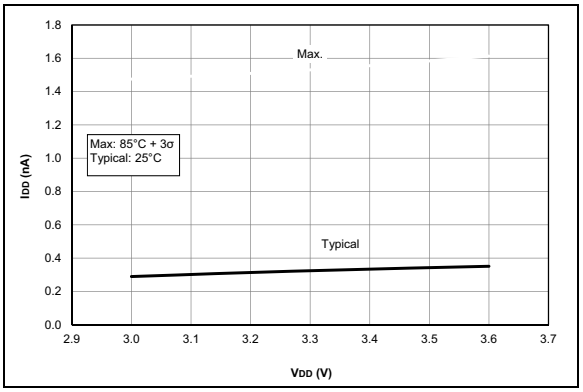
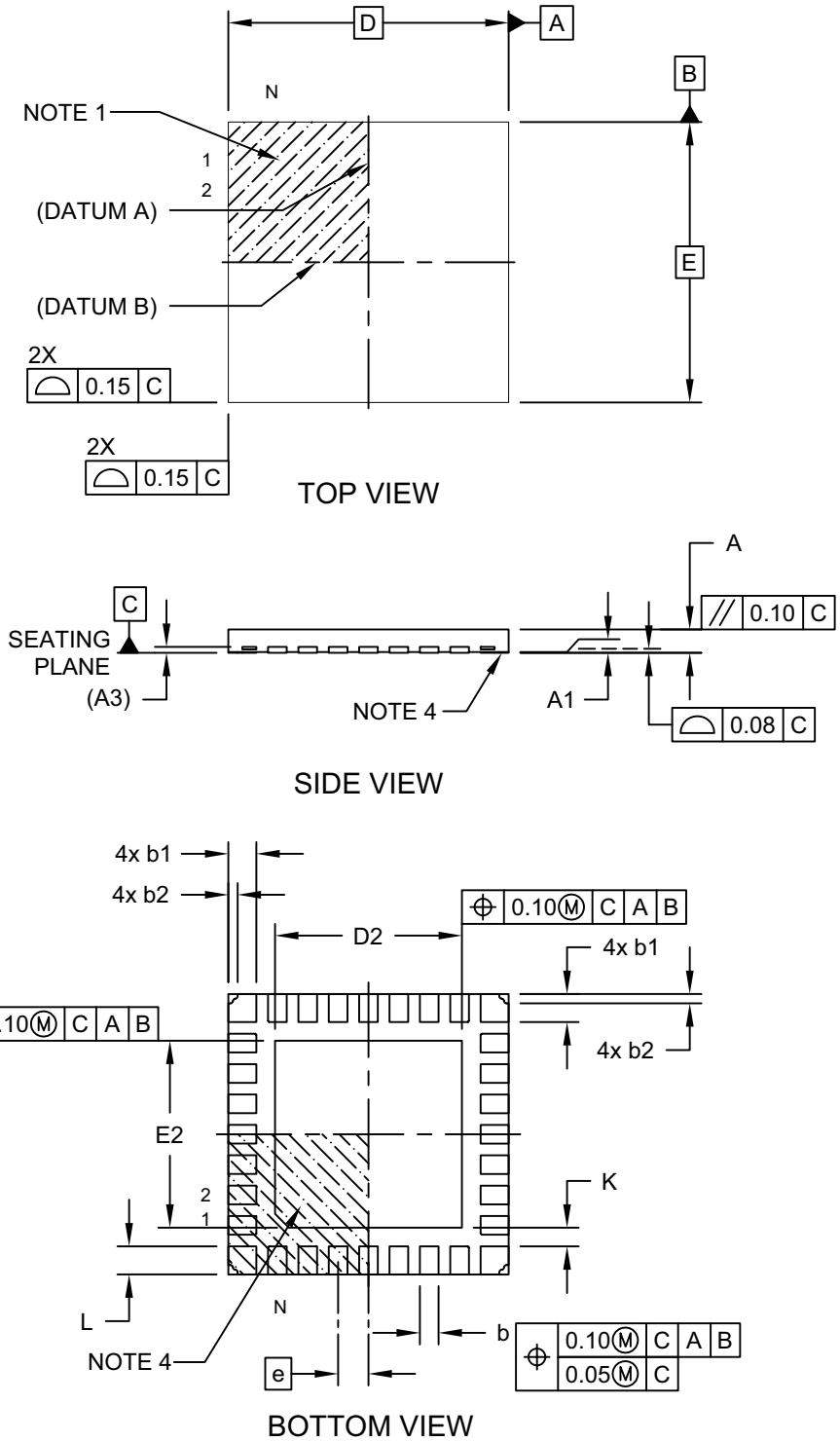


FIGURE 37-42: *IPD, LP Brown-Out Reset (LPBOR = 0), PIC16LF1777/8/9 Only.*

28-Lead Plastic Quad Flat, No Lead Package (MX) - 6x6x0.5mm Body [UQFN]
Ultra-Thin with 0.40 x 0.60 mm Terminal Width/Length and Corner Anchors

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-0209 Rev C Sheet 1 of 2