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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x10b; D/A 3x5b, 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1778-e-ss

TABLE 3: 28-PIN ALLOCATION TABLE (PIC16(L)F1778) (CONTINUED)

I/O	28-Pin SPDIP/SOIC/SSOP	28-Pin UQFN	ADC	VREF	DAC	Op Amp	Comparator	ZCD	PRG	Timers	PWM	CCP	COG	CLC	Modulator	EUSART	MSSP	Interrupt	Pull-ups	High Current	Basic
OUT(2)	—	—	—	—	—	—	C1OUT C2OUT C3OUT C4OUT C5OUT C6OUT	—	—	—	PWM3 PWM4 PWM5 PWM6 PWM9 PWM11	CCP1 CCP2 CCP7	COG1A COG1B COG1C COG1D COG2A COG2B COG2C COG2D COG3A COG3B COG3C COG3D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	MD1OUT MD2OUT MD3OUT	DT(3) TX CK	SDO SDA(3) SCK SCL(3)	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection register.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

1.0 DEVICE OVERVIEW

The PIC16(L)F1777/8/9 are described within this data sheet. See Table 2 for available package configurations.

Figure 1-1 shows a block diagram of the PIC16(L)F1777/8/9 devices. Table 1-2 shows the pinout descriptions.

Refer to Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F1778	PIC16(L)F1777/9
Analog-to-Digital Converter (ADC)		●	●
Fixed Voltage Reference (FVR)		●	●
Zero-Cross Detection (ZCD)		●	●
Temperature Indicator		●	●
Complementary Output Generator (COG)			
	COG1	●	●
	COG2	●	●
	COG3	●	●
	COG4		●
Programmable Ramp Generator (PRG)			
	PRG1	●	●
	PRG2	●	●
	PRG3	●	●
	PRG4		●
10-bit Digital-to-Analog Converter (DAC)			
	DAC1	●	●
	DAC2	●	●
	DAC5	●	●
	DAC6		●
5-bit Digital-to-Analog Converter (DAC)			
	DAC3	●	●
	DAC4	●	●
	DAC7	●	●
	DAC8		●
Capture/Compare/PWM (CCP/ECCP) Modules			
	CCP1	●	●
	CCP2	●	●
	CCP7	●	●
	CCP8		●
Comparators			
	C1	●	●
	C2	●	●
	C3	●	●
	C4	●	●
	C5	●	●
	C6	●	●
	C7		●
	C8		●

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F1778	PIC16(L)F1777/9
Configurable Logic Cell (CLC)			
	CLC1	●	●
	CLC2	●	●
	CLC3	●	●
	CLC4	●	●
Data Signal Modulator (DSM)			
	DSM1	●	●
	DSM2	●	●
	DSM3	●	●
	DSM4		●
Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)			
	EUSART	●	●
Master Synchronous Serial Ports			
	MSSP	●	●
Op Amps			
	OPA1	●	●
	OPA2	●	●
	OPA3	●	●
	OPA4		●
10-bit Pulse-Width Modulator (PWM)			
	PWM3	●	●
	PWM4	●	●
	PWM9	●	●
	PWM10		●
16-bit Pulse-Width Modulator (PWM)			
	PWM5	●	●
	PWM6	●	●
	PWM11	●	●
	PWM12		●
8-bit Timers			
	Timer0	●	●
	Timer2	●	●
	Timer4	●	●
	Timer6	●	●
	Timer8	●	●
16-bit Timers			
	Timer1	●	●
	Timer3	●	●
	Timer5	●	●

3.4 Register Definitions: Status

REGISTER 3-1: STATUS: STATUS REGISTER

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC(1)	C(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **$\overline{TO}$:** Time-Out bit
1 = After power-up, CLRWDT instruction or SLEEP instruction
0 = A WDT Time-out occurred

bit 3 **$\overline{PD}$:** Power-Down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{\text{Digit Borrow}}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{\text{Borrow}}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

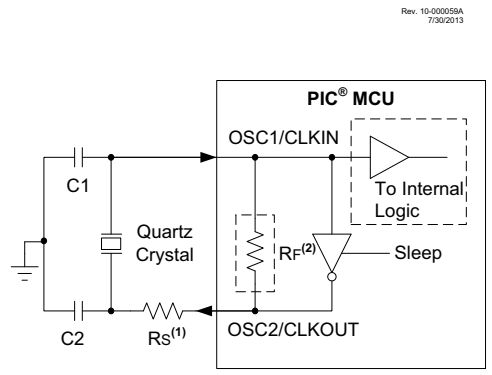
Note 1: For $\overline{\text{Borrow}}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand.

TABLE 3-15: PIC16(L)F1777/9 MEMORY MAP, BANK 27-30

	Bank 27		Bank 28		Bank 29		Bank 30
D8Ch	—	E0Ch	PPSLOCK	E8Ch	—	F0Ch	—
D8Dh	—	E0Dh	INTPPS	E8Dh	—	F0Dh	—
D8Eh	PWMEN	E0Eh	T0CKIPPS	E8Eh	—	F0Eh	—
D8Fh	PWMLD	E0Fh	T1CKIPPS	E8Fh	—	F0Fh	CLCDATA
D90h	PWMOUT	E10h	T1GPPS	E90h	RA0PPS	F10h	CLC1CON
D91h	PWM5PHL	E11h	T3CKIPPS	E91h	RA1PPS	F11h	CLC1POL
D92h	PWM5PHH	E12h	T3GPPS	E92h	RA2PPS	F12h	CLC1SEL0
D93h	PWM5DCL	E13h	T5CKIPPS	E93h	RA3PPS	F13h	CLC1SEL1
D94h	PWM5DCH	E14h	T5GPPS	E94h	RA4PPS	F14h	CLC1SEL2
D95h	PWM5PRL	E15h	T2INPPS	E95h	RA5PPS	F15h	CLC1SEL3
D96h	PWM5PRH	E16h	T4INPPS	E96h	RA6PPS	F16h	CLC1GLS0
D97h	PWM5OFL	E17h	T6INPPS	E97h	RA7PPS	F17h	CLC1GLS1
D98h	PWM5OFH	E18h	T8INPPS	E98h	RB0PPS	F18h	CLC1GLS2
D99h	PWM5TMRL	E19h	CCP1PPS	E99h	RB1PPS	F19h	CLC1GLS3
D9Ah	PWM5TMRH	E1Ah	CCP2PPS	E9Ah	RB2PPS	F1Ah	CLC2CON
D9Bh	PWM5CON	E1Bh	CCP7PPS	E9Bh	RB3PPS	F1Bh	CLC2POL
D9Ch	PWM5INTE	E1Ch	CCP8PPS	E9Ch	RB4PPS	F1Ch	CLC2SEL0
D9Dh	PWM5INTF	E1Dh	COG1INPPS	E9Dh	RB5PPS	F1Dh	CLC2SEL1
D9Eh	PWM5CLKCON	E1Eh	COG2INPPS	E9Eh	RB6PPS	F1Eh	CLC2SEL2
D9Fh	PWM5LDCON	E1Fh	COG3INPPS	E9Fh	RB7PPS	F1Fh	CLC2SEL3
DA0h	PWM5OFCON	E20h	COG4INPPS	EA0h	RC0PPS	F20h	CLC2GLS0
DA1h	PWM6PHL	E21h	MD1CLPPS	EA1h	RC1PPS	F21h	CLC2GLS1
DA2h	PWM6PHH	E22h	MD1CHPPS	EA2h	RC2PPS	F22h	CLC2GLS2
DA3h	PWM6DCL	E23h	MD1MODPPS	EA3h	RC3PPS	F23h	CLC2GLS3
DA4h	PWM6DCH	E24h	MD2CLPPS	EA4h	RC4PPS	F24h	CLC3CON
DA5h	PWM6PRL	E25h	MD2CHPPS	EA5h	RC5PPS	F25h	CLC3POL
DA6h	PWM6PRH	E26h	MD2MODPPS	EA6h	RC6PPS	F26h	CLC3SEL0
DA7h	PWM6OFL	E27h	MD3CLPPS	EA7h	RC7PPS	F27h	CLC3SEL1
DA8h	PWM6OFH	E28h	MD3CHPPS	EA8h	RD0PPS	F28h	CLC3SEL2
DA9h	PWM6TMRL	E29h	MD3MODPPS	EA9h	RD1PPS	F29h	CLC3SEL3
DAAh	PWM6TMRH	E2Ah	MD4CLPPS	EAAh	RD2PPS	F2Ah	CLC3GLS0
DABh	PWM6CON	E2Bh	MD4CHPPS	EABh	RD3PPS	F2Bh	CLC3GLS1
DACh	PWM6INTE	E2Ch	MD4MODPPS	EACh	RD4PPS	F2Ch	CLC3GLS2
DADh	PWM6INTF	E2Dh	PRG1RPPS	EADh	RD5PPS	F2Dh	CLC3GLS3
DAEh	PWM6CLKCON	E2Eh	PRG1FPPS	EAEh	RD6PPS	F2Eh	CLC4CON
DAFh	PWM6LDCON	E2Fh	PRG2RPPS	EAFh	RD7PPS	F2Fh	CLC4POL
DB0h	PWM6OFCON	E30h	PRG2FPPS	EB0h	RE0PPS	F30h	CLC4SEL0
DB1h	PWM11PHL	E31h	PRG3FPPS	EB1h	RE1PPS	F31h	CLC4SEL1
DB2h	PWM11PHH	E32h	PRG3RPPS	EB2h	RE2PPS	F32h	CLC4SEL2
DB3h	PWM11DCL	E33h	PRG4FPPS	EB3h		F33h	CLC4SEL3
DB4h	PWM11DCH	E34h	PRG4RPPS	EB4h		F34h	CLC4GLS0
DB5h	PWM11PRL	E35h	CLCIN0PPS	EB5h		F35h	CLC4GLS1
DB6h	PWM11PRH	E36h	CLCIN1PPS	EB6h		F36h	CLC4GLS2
DB7h	PWM11OFL	E37h	CLCIN2PPS	EB7h		F37h	CLC4GLS3
DB8h	PWM11OFH	E38h	CLCIN3PPS	EB8h		F38h	
DB9h	PWM11TMRL	E39h	ADCACTPPS	EB9h		F39h	
DBAh	PWM11TMRH	E3Ah	SSPCLKPPS	EBAh		F3Ah	
DBBh	PWM11CON	E3Bh	SSPDATPPS	EBBh		F3Bh	
DBCh	PWM11INTE	E3Ch	SSPSSPPS	EBCh		F3Ch	
DBDh	PWM11INTF	E3Dh	RXPPS	EBDh		F3Dh	
DBEh	PWM11CLKCON	E3Eh	CKPPS	EBEh		F3Eh	
DBFh	PWM11LDCON	E3Fh		EBFh		F3Fh	
DC0h	PWM11OFCON	E40h		EC0h		F40h	
DC1h	PWM12PHL	E31h		EB1h		F31h	
DC2h	PWM12PHH	E32h		EB2h		F32h	
DC3h	PWM12DCL	E33h		EB3h	—	F33h	
DC4h	PWM12DCH	E34h		EB4h		F34h	
DC5h	PWM12PRL	E35h		EB5h		F35h	
DC6h	PWM12PRH	E36h		EB6h		F36h	—
DC7h	PWM12OFL	E37h		EB7h		F37h	
DC8h	PWM12OFH	E38h		EB8h		F38h	
DC9h	PWM12TMRL	E39h	—	EB9h		F39h	
DCAh	PWM12TMRH	E3Ah		EBAh		F3Ah	
DCBh	PWM12CON	E3Bh		EBBh		F3Bh	
DCCh	PWM12INTE	E3Ch		EBCh		F3Ch	
DCDh	PWM12INTF	E3Dh		EBDh		F3Dh	
DCEh	PWM12CLKCON	E3Eh		EBEh		F3Eh	
DCFh	PWM12LDCON	E3Fh		EBFh		F3Fh	
DCFh	PWM12LDCON	E3Fh		EBFh		F3Fh	
DD0h	PWM12OFCON	E6Fh		EEFh		F6Fh	
DD1h - DEFh	—	E6Fh		EEFh		F6Fh	
		E6Fh		EEFh		F6Fh	

Legend: = Unimplemented data memory locations, read as '0',

FIGURE 5-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



Note 1: A series resistor (Rs) may be required for quartz crystals with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ and 10 MΩ).

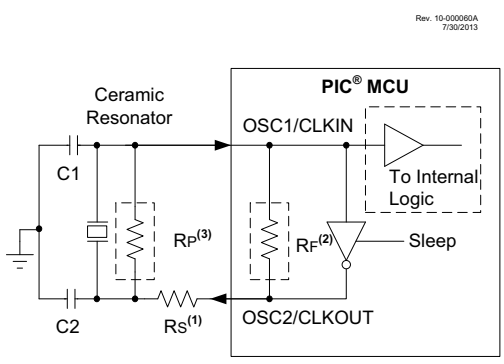
Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

2: Always verify oscillator performance over the VDD and temperature range that is expected for the application.

3: For oscillator design assistance, reference the following Microchip Application Notes:

- AN826, "*Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices*" (DS00826)
- AN849, "*Basic PIC® Oscillator Design*" (DS00849)
- AN943, "*Practical PIC® Oscillator Analysis and Design*" (DS00943)
- AN949, "*Making Your Oscillator Work*" (DS00949)

FIGURE 5-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)



Note 1: A series resistor (Rs) may be required for ceramic resonators with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ and 10 MΩ).

3. An additional parallel feedback resistor (RP) may be required for proper ceramic resonator operation.

5.2.1.3 Oscillator Start-up Timer (OST)

If the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended, unless either FSCM or Two-Speed Start-Up are enabled. In this case, code will continue to execute at the selected INTOSC frequency while the OST is counting. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the oscillator module.

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Clock Start-up mode can be selected (see **Section 5.4 "Two-Speed Clock Start-up Mode"**).

5.2.2.1 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a factory calibrated 16 MHz internal clock source. The frequency of the HFINTOSC can be altered via software using the OSCTUNE register (Register 5-3).

The output of the HFINTOSC connects to a postscaler and multiplexer (see Figure 5-1). One of multiple frequencies derived from the HFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See **Section 5.2.2.7 "Internal Oscillator Clock Switch Timing"** for more information.

The HFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'.

A fast start-up oscillator allows internal circuits to power up and stabilize before switching to HFINTOSC.

The High-Frequency Internal Oscillator Ready bit (HFIOFR) of the OSCSTAT register indicates when the HFINTOSC is running.

The High-Frequency Internal Oscillator Status Locked bit (HFIOFL) of the OSCSTAT register indicates when the HFINTOSC is running within 2% of its final value.

The High-Frequency Internal Oscillator Stable bit (HFIOFS) of the OSCSTAT register indicates when the HFINTOSC is running within 0.5% of its final value.

5.2.2.2 MFINTOSC

The Medium-Frequency Internal Oscillator (MFINTOSC) is a factory calibrated 500 kHz internal clock source. The frequency of the MFINTOSC can be altered via software using the OSCTUNE register (Register 5-3).

The output of the MFINTOSC connects to a postscaler and multiplexer (see Figure 5-1). One of nine frequencies derived from the MFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See **Section 5.2.2.7 "Internal Oscillator Clock Switch Timing"** for more information.

The MFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'.

The Medium-Frequency Internal Oscillator Ready bit (MFIOFR) of the OSCSTAT register indicates when the MFINTOSC is running.

5.2.2.3 Internal Oscillator Frequency Adjustment

The 500 kHz internal oscillator is factory calibrated. This internal oscillator can be adjusted in software by writing to the OSCTUNE register (Register 5-3). Since the HFINTOSC and MFINTOSC clock sources are derived from the 500 kHz internal oscillator, a change in the OSCTUNE register value will apply to both.

The default value of the OSCTUNE register is '0'. The value is a 6-bit two's complement number. A value of 1Fh will provide an adjustment to the maximum frequency. A value of 20h will provide an adjustment to the minimum frequency.

When the OSCTUNE register is modified, the oscillator frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

5.2.2.4 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is an uncalibrated 31 kHz internal clock source.

The output of the LFINTOSC connects to a multiplexer (see Figure 5-1). Select 31 kHz, via software, using the IRCF<3:0> bits of the OSCCON register. See **Section 5.2.2.7 "Internal Oscillator Clock Switch Timing"** for more information. The LFINTOSC is also the frequency for the Power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled by selecting 31 kHz (IRCF<3:0> bits of the OSCCON register = 000) as the system clock source (SCS bits of the OSCCON register = 1x), or when any of the following are enabled:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired LF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'.

Peripherals that use the LFINTOSC are:

- Power-up Timer (PWRT)
- Watchdog Timer (WDT)
- Fail-Safe Clock Monitor (FSCM)

The Low-Frequency Internal Oscillator Ready bit (LFIOFR) of the OSCSTAT register indicates when the LFINTOSC is running.

TABLE 6-5: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BORCON	SBOREN	BORFS	—	—	—	—	—	BORRDY	121
PCON	STKOVF	STKUNF	—	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	125
STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	40
WDTCON	—	—	WDTPS<4:0>					SWDTEN	154

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Resets.

7.6 Register Definitions: Interrupt Control

REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-0/0
GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all active interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all active peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **TMR0IE:** Timer0 Overflow Interrupt Enable bit
1 = Enables the Timer0 interrupt
0 = Disables the Timer0 interrupt

bit 4 **INTE:** INT External Interrupt Enable bit
1 = Enables the INT external interrupt
0 = Disables the INT external interrupt

bit 3 **IOCIE:** Interrupt-on-Change Enable bit
1 = Enables the interrupt-on-change
0 = Disables the interrupt-on-change

bit 2 **TMR0IF:** Timer0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed
0 = TMR0 register did not overflow

bit 1 **INTF:** INT External Interrupt Flag bit
1 = The INT external interrupt occurred
0 = The INT external interrupt did not occur

bit 0 **IOCIF:** Interrupt-on-Change Interrupt Flag bit(1)
1 = When at least one of the interrupt-on-change pins changed state
0 = None of the interrupt-on-change pins have changed state

Note 1: The IOCIF Flag bit is read-only and cleared when all the interrupt-on-change flags in the IOCxF registers have been cleared by software.

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 7-2: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **TMR1GIE:** Timer1 Gate Interrupt Enable bit
1 = Enables the Timer1 gate acquisition interrupt
0 = Disables the Timer1 gate acquisition interrupt

bit 6 **ADIE:** Analog-to-Digital Converter (ADC) Interrupt Enable bit
1 = Enables the ADC interrupt
0 = Disables the ADC interrupt

bit 5 **RCIE:** EUSART Receive Interrupt Enable bit
1 = Enables the EUSART receive interrupt
0 = Disables the EUSART receive interrupt

bit 4 **TXIE:** EUSART Transmit Interrupt Enable bit
1 = Enables the EUSART transmit interrupt
0 = Disables the EUSART transmit interrupt

bit 3 **SSP1IE:** Synchronous Serial Port (MSSP) Interrupt Enable bit
1 = Enables the MSSP interrupt
0 = Disables the MSSP interrupt

bit 2 **CCP1IE:** CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 1 **TMR2IE:** TMR2 to T2PR Match Interrupt Enable bit
1 = Enables the Timer2 to T2PR match interrupt
0 = Disables the Timer2 to T2PR match interrupt

bit 0 **TMR1IE:** Timer1 Overflow Interrupt Enable bit
1 = Enables the Timer1 overflow interrupt
0 = Disables the Timer1 overflow interrupt

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

9.1 Independent Clock Source

The WDT derives its time base from the 31 kHz LFINTOSC internal oscillator. Time intervals in this chapter are based on a nominal interval of 1 ms. See Table 36-8: Oscillator Parameters for the LFINTOSC specification.

9.2 WDT Operating Modes

The Watchdog Timer module has four operating modes controlled by the WDTE<1:0> bits in Configuration Words. See Table 9-1.

9.2.1 WDT IS ALWAYS ON

When the WDTE bits of Configuration Words are set to '11', the WDT is always on.

WDT protection is active during Sleep.

9.2.2 WDT IS OFF IN SLEEP

When the WDTE bits of Configuration Words are set to '10', the WDT is on, except in Sleep.

WDT protection is not active during Sleep.

9.2.3 WDT CONTROLLED BY SOFTWARE

When the WDTE bits of Configuration Words are set to '01', the WDT is controlled by the SWDTEN bit of the WDTCON register.

WDT protection is unchanged by Sleep. See Table 9-1 for more details.

TABLE 9-1: WDT OPERATING MODES

WDTE<1:0>	SWDTEN	Device Mode	WDT Mode
11	X	X	Active
10	X	Awake	Active
		Sleep	Disabled
01	1	X	Active
	0		Disabled
00	X	X	Disabled

9.3 Time-Out Period

The WDTPS bits of the WDTCON register set the time-out period from 1 ms to 256 seconds (nominal). After a Reset, the default time-out period is two seconds.

9.4 Clearing the WDT

The WDT is cleared when any of the following conditions occur:

- Any Reset
- CLRWDT instruction is executed
- Device enters Sleep
- Device wakes up from Sleep
- Oscillator fail
- WDT is disabled
- Oscillator Start-up Timer (OST) is running

See Table 9-2 for more information.

9.5 Operation During Sleep

When the device enters Sleep, the WDT is cleared. If the WDT is enabled during Sleep, the WDT resumes counting.

When the device exits Sleep, the WDT is cleared again. The WDT remains clear until the OST, if enabled, completes. See **Section 5.0 "Oscillator Module (with Fail-Safe Clock Monitor)"** for more information on the OST.

When a WDT time-out occurs while the device is in Sleep, no Reset is generated. Instead, the device wakes up and resumes operation. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register are changed to indicate the event. See STATUS Register (Register 3-1) for more information.

10.4 User ID, Device ID and Configuration Word Access

Instead of accessing program memory, the User ID's, Device ID/Revision ID and Configuration Words can be accessed when CFGS = 1 in the PMCON1 register. This is the region that would be pointed to by PC<15> = 1, but not all addresses are accessible. Different access may exist for reads and writes. Refer to Table 10-2.

When read access is initiated on an address outside the parameters listed in Table 10-2, the PMDATH:PMDATL register pair is cleared, reading back '0's.

TABLE 10-2: USER ID, DEVICE ID AND CONFIGURATION WORD ACCESS (CFGS = 1)

Address	Function	Read Access	Write Access
8000h-8003h	User IDs	Yes	Yes
8005h-8006h	Device ID/Revision ID	Yes	No
8007h-8008h	Configuration Words 1 and 2	Yes	No

EXAMPLE 10-4: CONFIGURATION WORD AND DEVICE ID ACCESS

```
* This code block will read 1 word of program memory at the memory address:
*   PROG_ADDR_LO (must be 00h-08h) data will be returned in the variables;
*   PROG_DATA_HI, PROG_DATA_LO

    BANKSEL  PMADRL           ; Select correct Bank
    MOVLW    PROG_ADDR_LO     ;
    MOVWF    PMADRL           ; Store LSB of address
    CLRF     PMADRH           ; Clear MSB of address

    BSF      PMCON1,CFGS      ; Select Configuration Space
    BCF      INTCON,GIE       ; Disable interrupts
    BSF      PMCON1,RD        ; Initiate read
    NOP                       ; Executed (See Figure 10-2)
    NOP                       ; Ignored (See Figure 10-2)
    BSF      INTCON,GIE       ; Restore interrupts

    MOVF     PMDATL,W         ; Get LSB of word
    MOVWF    PROG_DATA_LO     ; Store in user location
    MOVF     PMDATH,W         ; Get MSB of word
    MOVWF    PROG_DATA_HI     ; Store in user location
```

11.10 Register Definitions: PORTE

REGISTER 11-34: PORTE: PORTE REGISTER

U-0	U-0	U-0	U-0	R-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	—	RE3	RE2(1)	RE1(1)	RE0(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **Unimplemented**: Read as '0'

bit 3-0 **RE<3:0>**: PORTE I/O Pin bits(1)
1 = Port pin is > VIH
0 = Port pin is < VIL

Note 1: RE<2:0> are not implemented on the PIC16(L)F1778. Read as '0'. Writes to RE<2:0> are actually written to corresponding LATE register. Reads from PORTE register is the return of actual I/O pin values.

REGISTER 11-35: TRISE: PORTE TRI-STATE REGISTER

U-0	U-0	U-0	U-0	U-1(2)	R/W-1	R/W-1	R/W-1
—	—	—	—	—	TRISE2(1)	TRISE1(1)	TRISE0(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **Unimplemented**: Read as '0'

bit 3 **Unimplemented**: Read as '1'

bit 2-0 **TRISE<2:0>:** RE<2:0> Tri-State Control bits(1)
1 = PORTE pin configured as an input (tri-stated)
0 = PORTE pin configured as an output

Note 1: TRISE<2:0> are not implemented on the PIC16(L)F1778.
2: Unimplemented, read as '1'.

TABLE 19-6: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	177
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	182
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—	187
CM1CON0	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	258
CM2CON0	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	258
CM3CON0	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	258
CM4CON0	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	258
CM5CON0	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	258
CM6CON0	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	258
CM1CON1	—	—	—	—	—	—	INTP	INTN	259
CM2CON1	—	—	—	—	—	—	INTP	INTN	259
CM3CON1	—	—	—	—	—	—	INTP	INTN	259
CM4CON1	—	—	—	—	—	—	INTP	INTN	259
CM5CON1	—	—	—	—	—	—	INTP	INTN	259
CM6CON1	—	—	—	—	—	—	INTP	INTN	259
CM7CON1(1)	—	—	—	—	—	—	INTP	INTN	259
CM8CON1(1)	—	—	—	—	—	—	INTP	INTN	259
CM1NSEL	—	—	—	—	NCH<3:0>				260
CM2NSEL	—	—	—	—	NCH<3:0>				260
CM3NSEL	—	—	—	—	NCH<3:0>				260
CM4NSEL	—	—	—	—	NCH<3:0>				260
CM5NSEL	—	—	—	—	NCH<3:0>				260
CM6NSEL	—	—	—	—	NCH<3:0>				260
CM7NSEL(1)	—	—	—	—	NCH<3:0>				260
CM8NSEL(1)	—	—	—	—	NCH<3:0>				260
CM1PSEL	—	—	—	—	PCH<3:0>				261
CM2PSEL	—	—	—	—	PCH<3:0>				261
CM3PSEL	—	—	—	—	PCH<3:0>				261
CM4PSEL	—	—	—	—	PCH<3:0>				261
CM5PSEL	—	—	—	—	PCH<3:0>				261
CM6PSEL	—	—	—	—	PCH<3:0>				261
CM7PSEL(1)	—	—	—	—	PCH<3:0>				261
CM8PSEL(1)	—	—	—	—	PCH<3:0>				261
CMOUT	MC8OUT(1)	MC7OUT(1)	MC6OUT	MC5OUT	MC4OUT	MC3OUT	MC2OUT	MC1OUT	262
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		223
DAC1CON0	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC2CON0	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC5CON0	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC6CON0(1)	EN	FM	OE1	OE2	PSS<1:0>		NSS<1:0>		249
DAC3CON0	EN	—	OE1	OE2	PSS<1:0>		NSS<1:0>		244
DAC4CON0	EN	—	OE1	OE2	PSS<1:0>		NSS<1:0>		244
DAC7CON0	EN	—	OE1	OE2	PSS<1:0>		NSS<1:0>		244
DAC8CON0(1)	EN	—	OE1	OE2	PSS<1:0>		NSS<1:0>		244
DAC3REF	---	---	---	REF<4:0>					245
DAC4REF	---	---	---	REF<4:0>					245
DAC7REF	---	---	---	REF<4:0>					245
DAC8REF(1)	---	---	---	REF<4:0>					245
DAC1REFH	REF<9:x> (x Depends on FM bit)								250

Legend: — = unimplemented location, read as '0'. Shaded cells are unused by the comparator module.
Note 1: PIC16LF1777/9 only.

NOTES:

27.3 Modes of Operation

27.3.1 STEERED PWM MODES

In Steered PWM mode, the PWM signal derived from the input event sources is output as a single phase PWM which can be steered to any combination of the four COG outputs. Output steering takes effect on the instruction cycle following the write to the COGxSTR register.

Synchronous Steered PWM mode is identical to the Steered PWM mode except that changes to the output steering take effect on the first rising event after the COGxSTR register write. Static output data is not synchronized.

Steering mode configurations are shown in Figure 27-2 and Figure 27-3.

Steered PWM and Synchronous Steered PWM modes are selected by setting the MD<2:0> bits of the COGxCON0 register (Register 27-1) to '000' and '001', respectively.

27.3.2 FULL-BRIDGE MODES

In both Forward and Reverse Full-Bridge modes, two of the four COG outputs are active and the other two are inactive. Of the two active outputs, one is modulated by the PWM input signal and the other is on at 100% duty cycle. When the direction is changed, the dead-band time is inserted to delay the modulated output. This gives the unmodulated driver time to shut down, thereby, preventing shoot-through current in the series connected power devices.

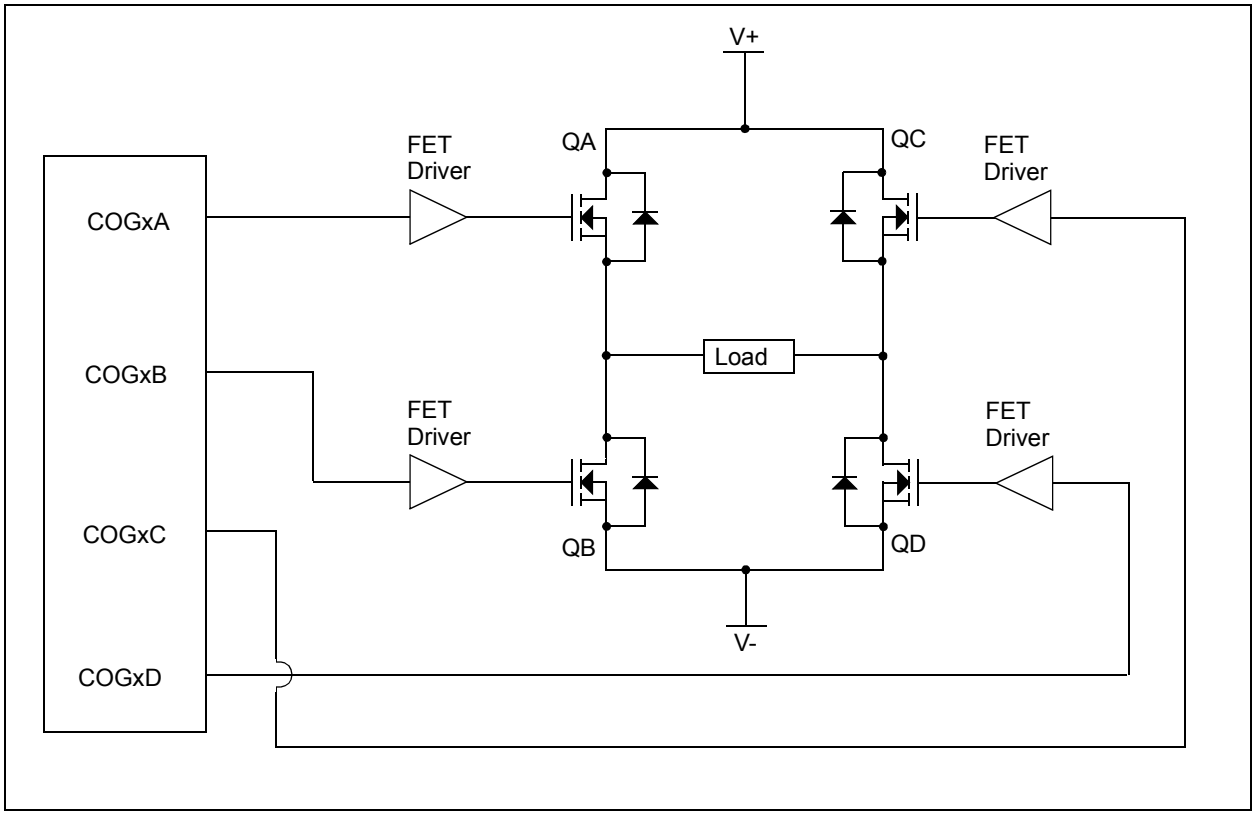
In Forward Full-Bridge mode, the PWM input modulates the COGxD output and drives the COGA output at 100%.

In Reverse Full-Bridge mode, the PWM input modulates the COGxB output and drives the COGxC output at 100%.

The full-bridge configuration is shown in Figure 27-4. Typical full-bridge waveforms are shown in Figure 27-12 and Figure 27-13.

Full-Bridge Forward and Full-Bridge Reverse modes are selected by setting the MD<2:0> bits of the COGxCON0 register to '010' and '011', respectively.

FIGURE 27-1: EXAMPLE OF FULL-BRIDGE APPLICATION



REGISTER 30-2: PRGxCON1: PROGRAMMABLE RAMP GENERATOR CONTROL 1 REGISTER

U-0	U-0	U-0	U-0	U-0	R-0	R/W-0/0	R/W-0/0
—	—	—	—	—	RDY	FPOL	RPOL
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = value depends on configuration bits

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **RDY:** Slope Generator Ready Status bit
1 = PRG is ready
0 = PRG is not ready

bit 1 **FPOL:** Fall Event Polarity Select bit
1 = Set_falling timing input is active-low
0 = Set_falling timing input is active-high

bit 0 **RPOL:** Rise Event Polarity Select bit
1 = Set_rising timing input is active-low
0 = Set_rising timing input is active-high

REGISTER 30-3: PRGxINS: VOLTAGE INPUT SELECT REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	INS<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = value depends on configuration bits

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **INS<3:0>:** Voltage Input Select bits
Selects source of voltage level at which the ramp starts. See Table 30-3.

TABLE 30-3: VOLTAGE INPUT SOURCES

INS<2:0>	PRG1 Voltage Source	PRG2 Voltage Source	PRG3 Voltage Source	PRG4 Voltage Source(2)
1010-1111	Reserved	Reserved	Reserved	Reserved
1001(1)	Switched PRG1IN1/OPA2OUT	Switched PRG1IN1/OPA2OUT	Switched PRG3IN1/OPA4OUT(2)	Switched PRG4IN1/OPA3OUT
1000(1)	Switched PRG1IN0/OPA1OUT	Switched PRG1IN0/OPA1OUT	Switched PRG3IN0/OPA3OUT	Switched PRG4IN0/OPA4OUT
0111	Reserved	Reserved	Reserved	Reserved
0110	DAC4_output	DAC4_output	DAC8_output(2)	DAC8_output
0101	DAC3_output	DAC3_output	DAC7_output	DAC7_output
0100	DAC2_output	DAC2_output	DAC6_output(2)	DAC6_output
0011	DAC1_output	DAC1_output	DAC5_output	DAC5_output
0010	FVR_buffer1	FVR_buffer1	FVR_buffer2	FVR_buffer2
0001	PRG1IN1/OPA2OUT	PRG2IN1/OPA1OUT	PRG3IN1/OPA4OUT(2)	PRG4IN1/OPA3OUT
0000	PRG1IN0/OPA1OUT	PRG2IN0/OPA2OUT	PRG3IN0/OPA3OUT	PRG4IN0/OPA4OUT

Note 1: Input source is switched off when op amp override is forcing tri-state. See **Section 29.3 "Override Control"**.
2: PIC16(L)F1777/9 only.

TABLE 36-25: SPI MODE REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
SP70*	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK↓ or SCK↑ input	2.25 Tcy	—	—	ns	
SP71*	TscH	SCK input high time (Slave mode)	Tcy + 20	—	—	ns	
SP72*	TscL	SCK input low time (Slave mode)	Tcy + 20	—	—	ns	
SP73*	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	100	—	—	ns	
SP74*	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	100	—	—	ns	
SP75*	TdoR	SDO data output rise time	—	10	25	ns	3.0V ≤ VDD ≤ 5.5V
			—	25	50	ns	1.8V ≤ VDD ≤ 5.5V
SP76*	TdoF	SDO data output fall time	—	10	25	ns	
SP77*	TssH2doZ	$\overline{SS}\uparrow$ to SDO output high-impedance	10	—	50	ns	
SP78*	TscR	SCK output rise time (Master mode)	—	10	25	ns	3.0V ≤ VDD ≤ 5.5V
			—	25	50	ns	1.8V ≤ VDD ≤ 5.5V
SP79*	TscF	SCK output fall time (Master mode)	—	10	25	ns	
SP80*	TscH2doV, TscL2doV	SDO data output valid after SCK edge	—	—	50	ns	3.0V ≤ VDD ≤ 5.5V
			—	—	145	ns	1.8V ≤ VDD ≤ 5.5V
SP81*	TdoV2scH, TdoV2scL	SDO data output setup to SCK edge	1 Tcy	—	—	ns	
SP82*	TssL2doV	SDO data output valid after $\overline{SS}\downarrow$ edge	—	—	50	ns	
SP83*	TscH2ssH, TscL2ssH	$\overline{SS}\uparrow$ after SCK edge	1.5 Tcy + 40	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

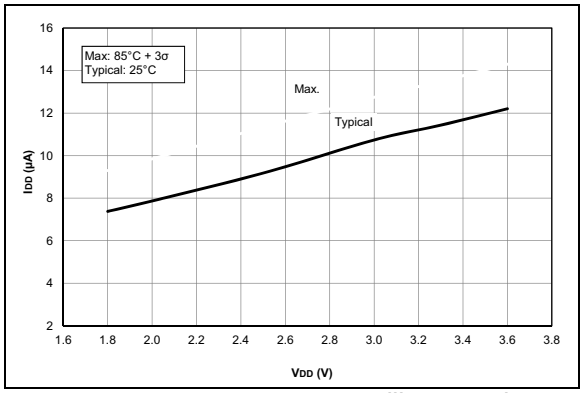


FIGURE 37-1: *IDD, LP Oscillator Mode, Fosc = 32 kHz, PIC16LF1777/8/9 Only.*

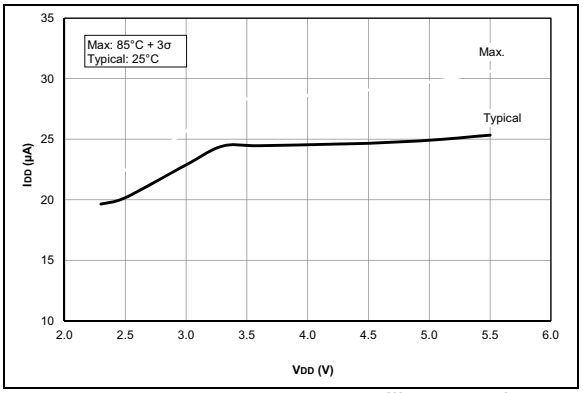


FIGURE 37-2: *IDD, LP Oscillator Mode, Fosc = 32 kHz, PIC16F1777/8/9 Only.*

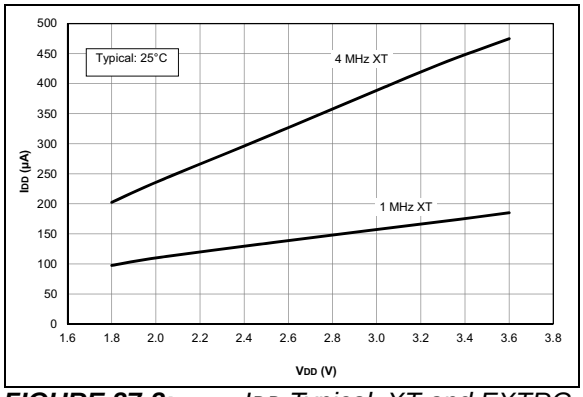


FIGURE 37-3: *IDD Typical, XT and EXTRC Oscillator, PIC16LF1777/8/9 Only.*

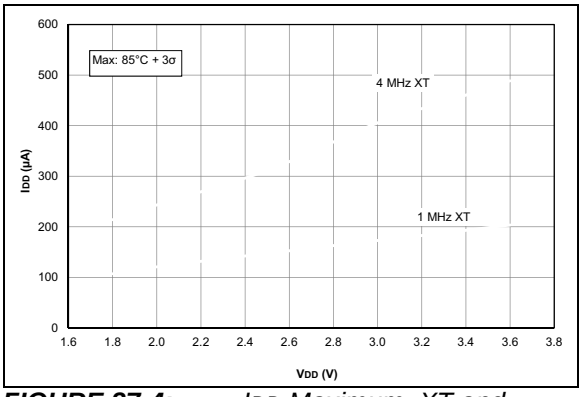


FIGURE 37-4: *IDD Maximum, XT and EXTRC Oscillator, PIC16LF1777/8/9 Only.*

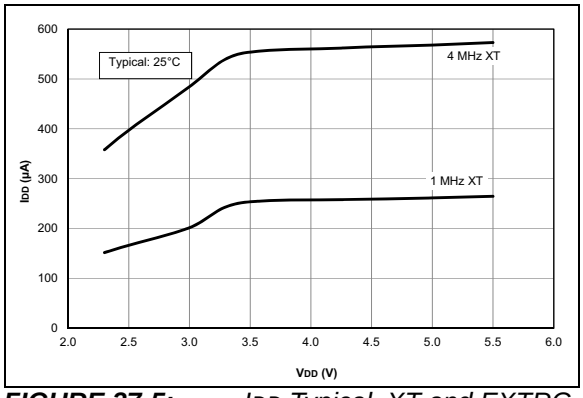


FIGURE 37-5: *IDD Typical, XT and EXTRC Oscillator, PIC16F1777/8/9 Only.*

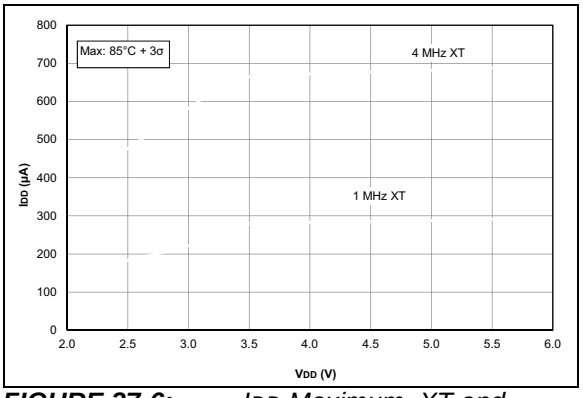
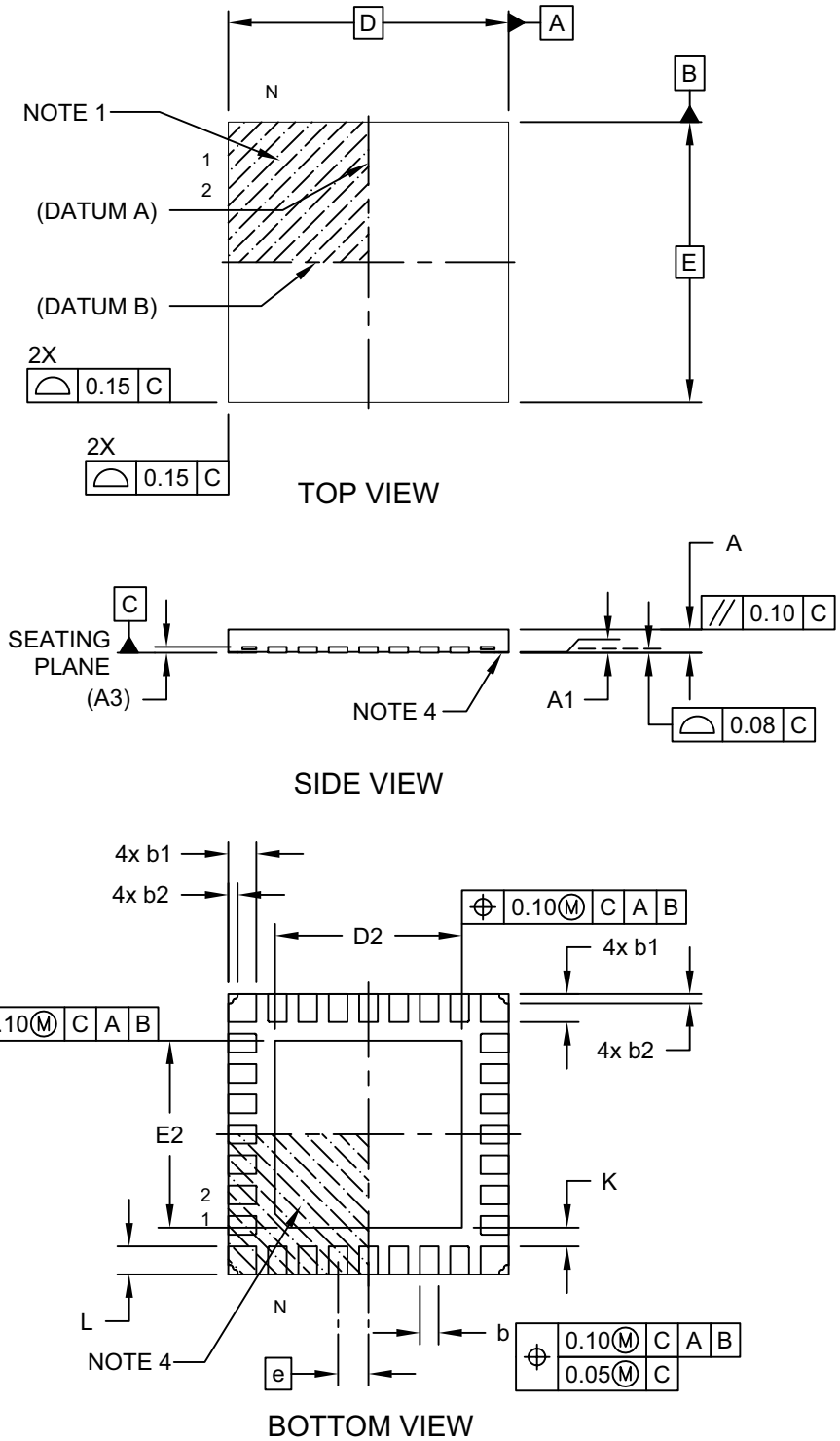


FIGURE 37-6: *IDD Maximum, XT and EXTRC Oscillator, PIC16F1777/8/9 Only.*

28-Lead Plastic Quad Flat, No Lead Package (MX) - 6x6x0.5mm Body [UQFN]
Ultra-Thin with 0.40 x 0.60 mm Terminal Width/Length and Corner Anchors

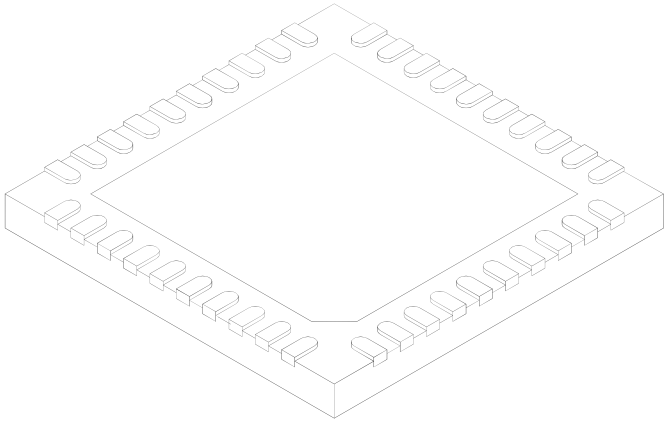
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-0209 Rev C Sheet 1 of 2

40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		40	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-156A Sheet 2 of 2