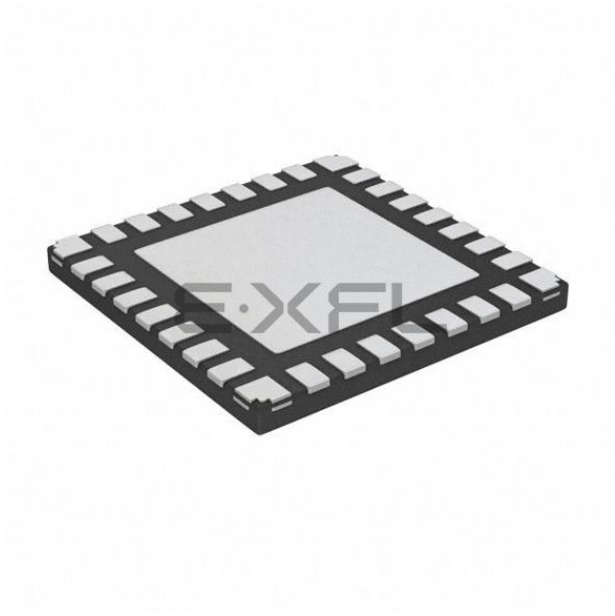

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 28KB (16K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | 128 x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 17x10b; D/A 3x5b, 3x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-UQFN Exposed Pad |
| Supplier Device Package | 28-UQFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1778t-i-mx |

## 1.0 DEVICE OVERVIEW

The PIC16(L)F1777/8/9 are described within this data sheet. See Table 2 for available package configurations.

Figure 1-1 shows a block diagram of the PIC16(L)F1777/8/9 devices. Table 1-2 shows the pinout descriptions.

Refer to Table 1-1 for peripherals available per device.

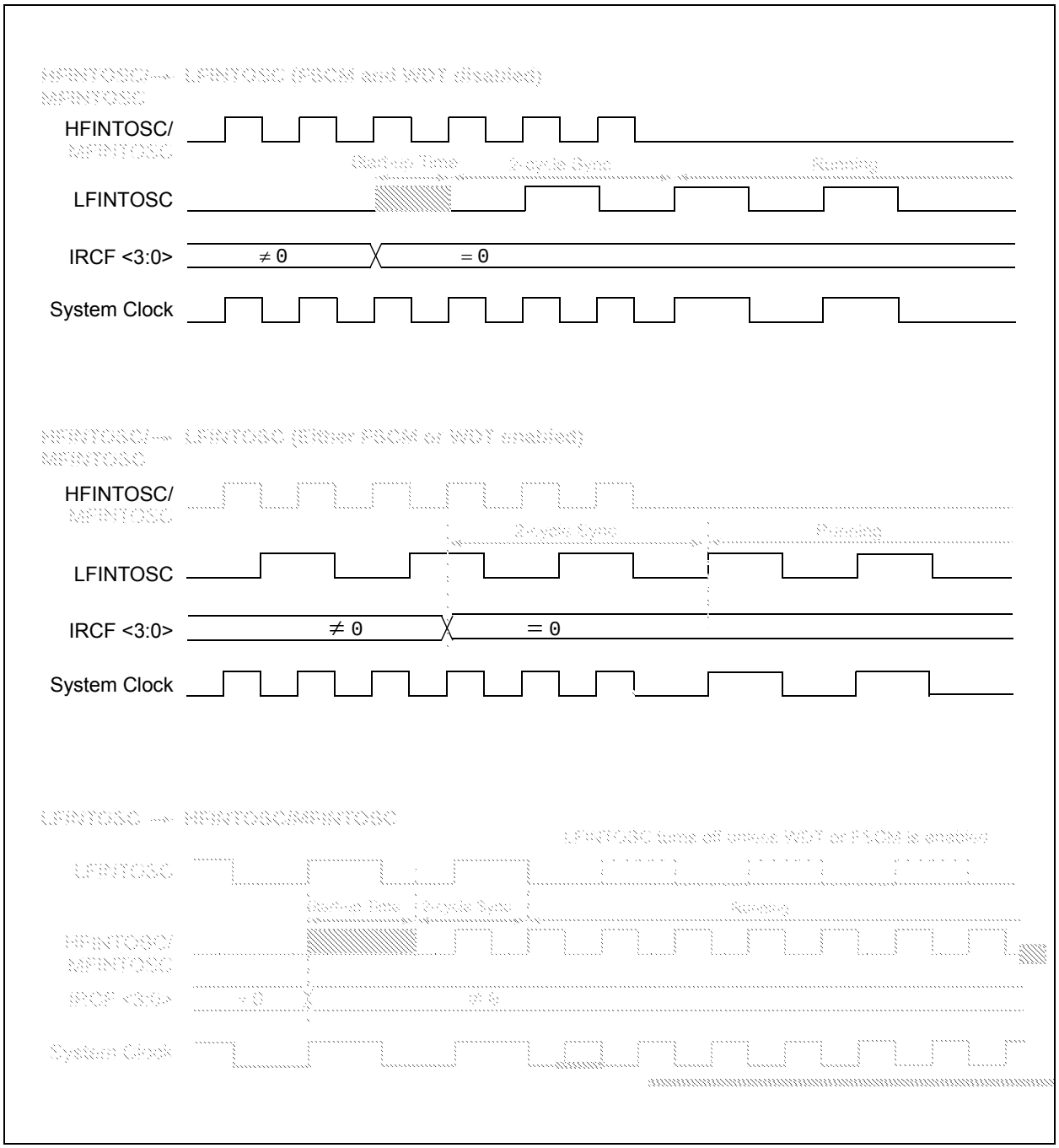
**TABLE 1-1: DEVICE PERIPHERAL SUMMARY**

| Peripheral | | PIC16(L)F1778 | PIC16(L)F1777/9 |
|---|---|---|---|
| Analog-to-Digital Converter (ADC) | | ● | ● |
| Fixed Voltage Reference (FVR) | | ● | ● |
| Zero-Cross Detection (ZCD) | | ● | ● |
| Temperature Indicator | | ● | ● |
| Complementary Output Generator (COG) | | | |
| | COG1 | ● | ● |
| | COG2 | ● | ● |
| | COG3 | ● | ● |
| | COG4 | | ● |
| Programmable Ramp Generator (PRG) | | | |
| | PRG1 | ● | ● |
| | PRG2 | ● | ● |
| | PRG3 | ● | ● |
| | PRG4 | | ● |
| 10-bit Digital-to-Analog Converter (DAC) | | | |
| | DAC1 | ● | ● |
| | DAC2 | ● | ● |
| | DAC5 | ● | ● |
| | DAC6 | | ● |
| 5-bit Digital-to-Analog Converter (DAC) | | | |
| | DAC3 | ● | ● |
| | DAC4 | ● | ● |
| | DAC7 | ● | ● |
| | DAC8 | | ● |
| Capture/Compare/PWM (CCP/ECCP) Modules | | | |
| | CCP1 | ● | ● |
| | CCP2 | ● | ● |
| | CCP7 | ● | ● |
| | CCP8 | | ● |
| Comparators | | | |
| | C1 | ● | ● |
| | C2 | ● | ● |
| | C3 | ● | ● |
| | C4 | ● | ● |
| | C5 | ● | ● |
| | C6 | ● | ● |
| | C7 | | ● |
| | C8 | | ● |

**TABLE 1-1: DEVICE PERIPHERAL SUMMARY**

| Peripheral | | PIC16(L)F1778 | PIC16(L)F1777/9 |
|---|---|---|---|
| Configurable Logic Cell (CLC) | | | |
| | CLC1 | ● | ● |
| | CLC2 | ● | ● |
| | CLC3 | ● | ● |
| | CLC4 | ● | ● |
| Data Signal Modulator (DSM) | | | |
| | DSM1 | ● | ● |
| | DSM2 | ● | ● |
| | DSM3 | ● | ● |
| | DSM4 | | ● |
| Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART) | | | |
| | EUSART | ● | ● |
| Master Synchronous Serial Ports | | | |
| | MSSP | ● | ● |
| Op Amps | | | |
| | OPA1 | ● | ● |
| | OPA2 | ● | ● |
| | OPA3 | ● | ● |
| | OPA4 | | ● |
| 10-bit Pulse-Width Modulator (PWM) | | | |
| | PWM3 | ● | ● |
| | PWM4 | ● | ● |
| | PWM9 | ● | ● |
| | PWM10 | | ● |
| 16-bit Pulse-Width Modulator (PWM) | | | |
| | PWM5 | ● | ● |
| | PWM6 | ● | ● |
| | PWM11 | ● | ● |
| | PWM12 | | ● |
| 8-bit Timers | | | |
| | Timer0 | ● | ● |
| | Timer2 | ● | ● |
| | Timer4 | ● | ● |
| | Timer6 | ● | ● |
| | Timer8 | ● | ● |
| 16-bit Timers | | | |
| | Timer1 | ● | ● |
| | Timer3 | ● | ● |
| | Timer5 | ● | ● |

**FIGURE 5-7: INTERNAL OSCILLATOR SWITCH TIMING**



## 8.3 Register Definitions: Voltage Regulator Control

**REGISTER 8-1: VREGCON: VOLTAGE REGULATOR CONTROL REGISTER(1)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0/0 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | VREGPM | Reserved |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

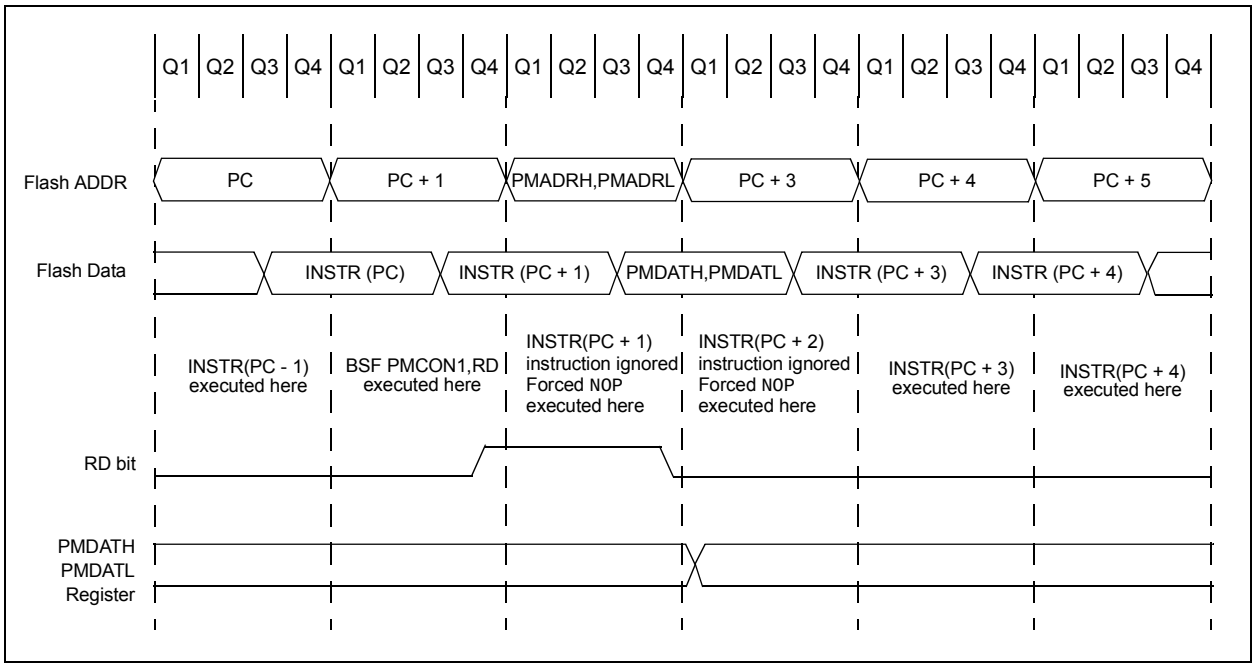
bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **VREGPM:** Voltage Regulator Power Mode Selection bit
- 1 = Low-Power Sleep mode enabled in Sleep(2)
  Draws lowest current in Sleep, slower wake-up
- 0 = Normal Power mode enabled in Sleep(2)
  Draws higher current in Sleep, faster wake-up

bit 0 **Reserved:** Read as ‘1’. Maintain this bit set.

**Note 1:** PIC16F1777/8/9 only.
**2:** See **Section 36.0 “Electrical Specifications”**.

**FIGURE 10-2: FLASH PROGRAM MEMORY READ CYCLE EXECUTION**




**EXAMPLE 10-1: FLASH PROGRAM MEMORY READ**

```
* This code block will read 1 word of program
* memory at the memory address:
    PROG_ADDR_HI : PROG_ADDR_LO
*   data will be returned in the variables;
*   PROG_DATA_HI, PROG_DATA_LO

    BANKSEL  PMADRL           ; Select Bank for PMCON registers
    MOVLW    PROG_ADDR_LO     ;
    MOVWF    PMADRL           ; Store LSB of address
    MOVLW    PROG_ADDR_HI     ;
    MOVWF    PMADRH           ; Store MSB of address

    BCF      PMCON1,CFGS      ; Do not select Configuration Space
    BSF      PMCON1,RD        ; Initiate read
    NOP                       ; Ignored (Figure 10-1)
    NOP                       ; Ignored (Figure 10-1)

    MOVF     PMDATL,W         ; Get LSB of word
    MOVWF    PROG_DATA_LO     ; Store in user location
    MOVF     PMDATH,W         ; Get MSB of word
    MOVWF    PROG_DATA_HI     ; Store in user location
```

**REGISTER 11-28: LATD: PORTD DATA LATCH REGISTER**

| R/W-x/u | R/W-x/u | R/W-x/u | R/W-x/u | R/W-x/u | R/W-x/u | R/W-x/u | R/W-x/u |
|---|---|---|---|---|---|---|---|
| LATD7 | LATD6 | LATD5 | LATD4 | LATD3 | LATD2 | LATD1 | LATD0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-0 **LATD<7:0>**: PORTD Output Latch Value bits

**REGISTER 11-29: ANSELD: PORTD ANALOG SELECT REGISTER**

| R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| ANSD7 | ANSD6 | ANSD5 | ANSD4 | ANSD3 | ANSD2 | ANSD1 | ANSD0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-0 **ANSD<7:0>**: Analog Select between Analog or Digital Function on pins RD<7:0>**(1)**
1 = Analog input. Pin is assigned as analog input**(1)**. Digital input buffer disabled.
0 = Digital I/O. Pin is assigned to port or digital special function.

**Note 1:** When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

**REGISTER 11-32: SLRCOND: PORTD SLEW RATE CONTROL REGISTER**

| R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| SLRD7 | SLRD6 | SLRD5 | SLRD4 | SLRD3 | SLRD2 | SLRD1 | SLRD0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-0 **SLRD<7:0>:** PORTD Slew Rate Enable bits
For RD<7:0> pins
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

**REGISTER 11-33: INLVLD: PORTD INPUT LEVEL CONTROL REGISTER**

| R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| INLVLD7 | INLVLD6 | INLVLD5 | INLVLD4 | INLVLD3 | INLVLD2 | INLVLD1 | INLVLD0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-0 **INLVLD<7:0>:** PORTD Input Level Select bits
For RD<7:0> pins
1 = Port pin digital input operates with ST thresholds
0 = Port pin digital input operates with TTL thresholds

## 11.10 Register Definitions: PORTE

**REGISTER 11-34: PORTE: PORTE REGISTER**

| U-0 | U-0 | U-0 | U-0 | R-x/u | R/W-x/u | R/W-x/u | R/W-x/u |
|---|---|---|---|---|---|---|---|
| — | — | — | — | RE3 | RE2(1) | RE1(1) | RE0(1) |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-4 **Unimplemented**: Read as '0'

bit 3-0 **RE<3:0>**: PORTE I/O Pin bits(1)
1 = Port pin is > VIH
0 = Port pin is < VIL

**Note 1:** RE<2:0> are not implemented on the PIC16(L)F1778. Read as '0'. Writes to RE<2:0> are actually written to corresponding LATE register. Reads from PORTE register is the return of actual I/O pin values.

**REGISTER 11-35: TRISE: PORTE TRI-STATE REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-1(2) | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | TRISE2(1) | TRISE1(1) | TRISE0(1) |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-4 **Unimplemented**: Read as '0'

bit 3 **Unimplemented**: Read as '1'

bit 2-0 **TRISE<2:0>:** RE<2:0> Tri-State Control bits(1)
1 = PORTE pin configured as an input (tri-stated)
0 = PORTE pin configured as an output

**Note 1:** TRISE<2:0> are not implemented on the PIC16(L)F1778.
**2:** Unimplemented, read as '1'.

**TABLE 12-3: SUMMARY OF REGISTERS ASSOCIATED WITH THE PPS MODULE**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on page |
|---|---|---|---|---|---|---|---|---|---|
| PPSLOCK | — | — | — | — | — | — | — | PPSLOCKED | 206 |
| INTPPS | — | — | INTPPS<5:0> | | | | | | 205 |
| T0CKIPPS | — | — | T0CKIPPS<5:0> | | | | | | 205 |
| T1CKIPPS | — | — | T1CKIPPS<5:0> | | | | | | 205 |
| T1GPPS | — | — | T1GPPS<5:0> | | | | | | 205 |
| T3CKIPPS | — | — | T3CKIPPS<5:0> | | | | | | 205 |
| T3GPPS | — | — | T3GPPS<5:0> | | | | | | 205 |
| T5CKIPPS | — | — | T5CKIPPS<5:0> | | | | | | 205 |
| T5GPPS | — | — | T5GPPS<5:0> | | | | | | 205 |
| T2INPPS | — | — | T2INPPS<5:0> | | | | | | 205 |
| T4INPPS | — | — | T4INPPS<5:0> | | | | | | 205 |
| T6INPPS | — | — | T6INPPS<5:0> | | | | | | 205 |
| T8INPPS | — | — | T8INPPS<5:0> | | | | | | 205 |
| CCP1PPS | — | — | CCP1PPS<5:0> | | | | | | 205 |
| CCP2PPS | — | — | CCP2PPS<5:0> | | | | | | 205 |
| CCP7PPS | — | — | CCP7PPS<5:0> | | | | | | 205 |
| CCP8PPS(1) | — | — | CCP8PPS<5:0> | | | | | | 205 |
| COGIN1PPS | — | — | COG1PPS<5:0> | | | | | | 205 |
| COG2INPPS | — | — | COG2PPS<5:0> | | | | | | 205 |
| COG3INPPS | — | — | COG3PPS<5:0> | | | | | | 205 |
| COG4INPPS(1) | — | — | COG4PPS<5:0> | | | | | | 205 |
| MD1CLPPS | — | — | MD1CLPPS<5:0> | | | | | | 205 |
| MD1CHPPS | — | — | MD1CHPPS<5:0> | | | | | | 205 |
| MD1MODPPS | — | — | MD1MODPPS<5:0> | | | | | | 205 |
| MD2CLPPS | — | — | MD2CLPPS<5:0> | | | | | | 205 |
| MD2CHPPS | — | — | MD2CHPPS<5:0> | | | | | | 205 |
| MD2MODPPS | — | — | MD2MODPPS<5:0> | | | | | | 205 |
| MD3CLPPS | — | — | MD3CLPPS<5:0> | | | | | | 205 |
| MD3CHPPS | — | — | MD3CHPPS<5:0> | | | | | | 205 |
| MD3MODPPS | — | — | MD3MODPPS<5:0> | | | | | | 205 |
| MD4CLPPS(1) | — | — | MD4CLPPS<5:0> | | | | | | 205 |
| MD4CHPPS(1) | — | — | MD4CHPPS<5:0> | | | | | | 205 |
| MD4MODPPS(1) | — | — | MD4MODPPS<5:0> | | | | | | 205 |
| PRG1RPPS | — | — | PRG1RPPS<5:0> | | | | | | 205 |
| PRG1FPPS | — | — | PRG1FPPS<5:0> | | | | | | 205 |
| PRG2RPPS | — | — | PRG2RPPS<5:0> | | | | | | 205 |
| PRG2FPPS | — | — | PRG2FPPS<5:0> | | | | | | 205 |
| PRG3RPPS | — | — | PRG3RPPS<5:0> | | | | | | 205 |
| PRG3FPPS | — | — | PRG3FPPS<5:0> | | | | | | 205 |
| PRG4RPPS | — | — | PRG4RPPS<5:0> | | | | | | 205 |
| PRG4FPPS | — | — | PRG4FPPS<5:0> | | | | | | 205 |
| CLC1IN0PPS | — | — | CLCIN0PPS<5:0> | | | | | | 205 |

## 15.4 ADC Acquisition Time

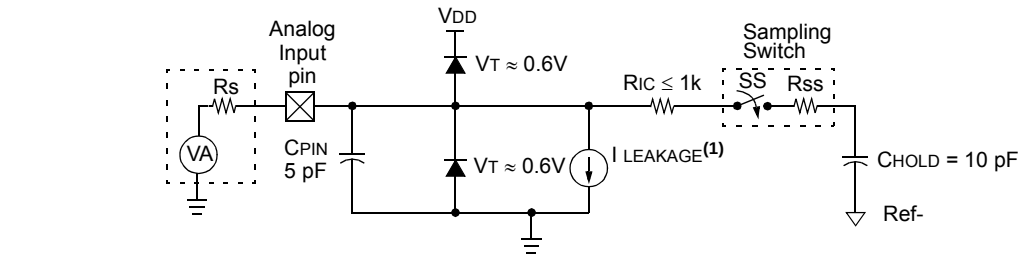
To ensure accurate temperature measurements, the user must wait at least 200 μs after the ADC input multiplexer is connected to the temperature indicator output before the conversion is performed. In addition, the user must wait 200 μs between sequential conversions of the temperature indicator output.

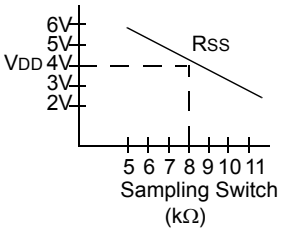
**TABLE 15-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE TEMPERATURE INDICATOR**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on page |
|---|---|---|---|---|---|---|---|---|---|
| FVRCON | FVREN | FVRRDY | TSEN | TSRNG | CDFVR<1:0> | | ADFVR<1:0> | | 223 |

**Legend:** Shaded cells are unused by the temperature indicator module.

**FIGURE 16-4: ANALOG INPUT MODEL**



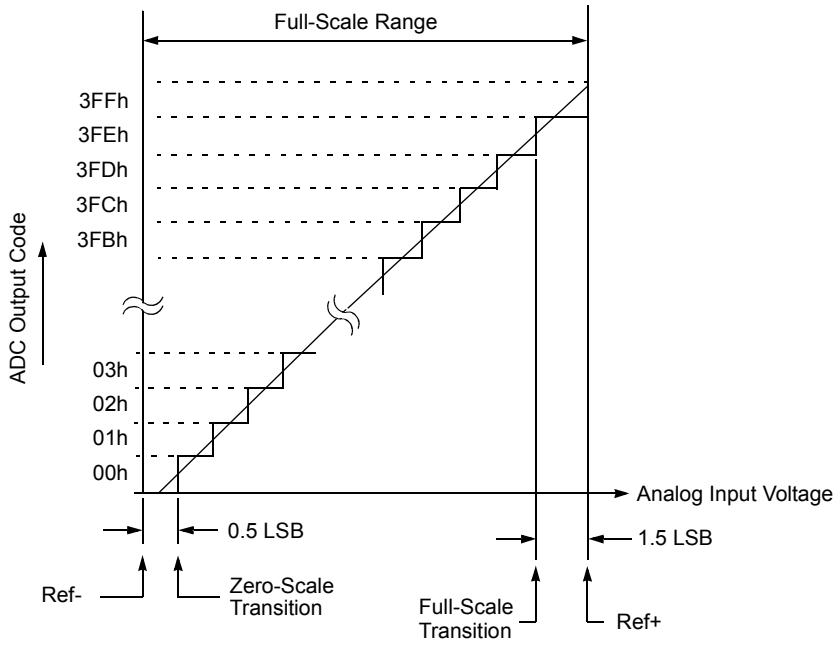




**Legend:**

| | |
|---|---|
| CHOLD | = Sample/Hold Capacitance |
| CPIN | = Input Capacitance |
| I LEAKAGE | = Leakage current at the pin due to various junctions |
| RIC | = Interconnect Resistance |
| RSS | = Resistance of Sampling Switch |
| SS | = Sampling Switch |
| VT | = Threshold Voltage |

**Note 1:** Refer to Table 36-4: I/O Ports (parameter D060).

**FIGURE 16-5: ADC TRANSFER FUNCTION**



## 19.11 Register Definitions: Comparator Control

Long bit name prefixes for the Comparator peripherals are shown in Table 19-3. Refer to **Section 1.1.2.2 "Long Bit Names"** for more information

**TABLE 19-3:**

| Peripheral | Bit Name Prefix |
|---|---|
| Comparator 1 | C1 |
| Comparator 2 | C2 |
| Comparator 3 | C3 |
| Comparator 4 | C4 |
| Comparator 5 | C5 |
| Comparator 6 | C6 |
| Comparator 7(1) | C7 |
| Comparator 8(1) | C8 |

**Note 1:** PIC16(L)F1777/9 only.

### REGISTER 19-1: CMxCON0: COMPARATOR Cx CONTROL REGISTER 0

| R/W-0/0 | R-0/0 | U-0 | R/W-0/0 | R/W-0/0 | R/W-1/1 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| ON | OUT | — | POL | ZLF | — | HYS | SYNC |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7 **ON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled and consumes no active power

bit 6 **OUT:** Comparator Output bit
If POL = 1 (inverted polarity):
1 = CxVP < CxVN
0 = CxVP > CxVN
If POL = 0 (non-inverted polarity):
1 = CxVP > CxVN
0 = CxVP < CxVN

bit 5 **Reserved:** Read as '1'. Maintain this bit set.

bit 4 **POL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 3 **ZLF:** Comparator Zero Latency Filter Enable bit
1 = Comparator output is filtered
0 = Comparator output is unfiltered

bit 2 **Reserved:** Read as '1'. Maintain this bit set.

bit 1 **HYS:** Comparator Hysteresis Enable bit
1 = Comparator hysteresis enabled
0 = Comparator hysteresis disabled

bit 0 **SYNC:** Comparator Output Synchronous Mode bit
1 = Comparator output to Timer1 and I/O pin is synchronous to changes on Timer1 clock source. Output updated on the falling edge of Timer1 clock source.
0 = Comparator output to Timer1 and I/O pin is asynchronous

**REGISTER 27-7: COGxFIS0: COG FALLING EVENT INPUT SELECTION REGISTER**

| R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| FIS7 | FIS6 | FIS5 | FIS4 | FIS3 | FIS2 | FIS1 | FIS0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | q = Value depends on condition |

bit 7-0 **FIS<7:0>:** Falling Event Input Source <n> Enable bits(1). See Table 27-5.
1 = Source <n> output is enabled as a falling event input
0 = Source <n> output has no effect on the falling event

**Note 1:** Any combination of <n> bits can be selected.

**REGISTER 27-8: COGxFIS1: COG FALLING EVENT INPUT SELECTION REGISTER**

| R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| FIS15 | FIS14 | FIS13 | FIS12 | FIS11 | FIS10 | FIS9 | FIS8 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | q = Value depends on condition |

bit 15-8 **FIS<15:8>:** Falling Event Input Source <n> Enable bits(1). See Table 27-5.
1 = Source <n> output is enabled as a falling event input
0 = Source <n> output has no effect on the falling event

**Note 1:** Any combination of <n> bits can be selected.

**FIGURE 30-2: SLOPE COMPENSATION (FALLING RAMP) TIMING DIAGRAM (MODE = 00)**

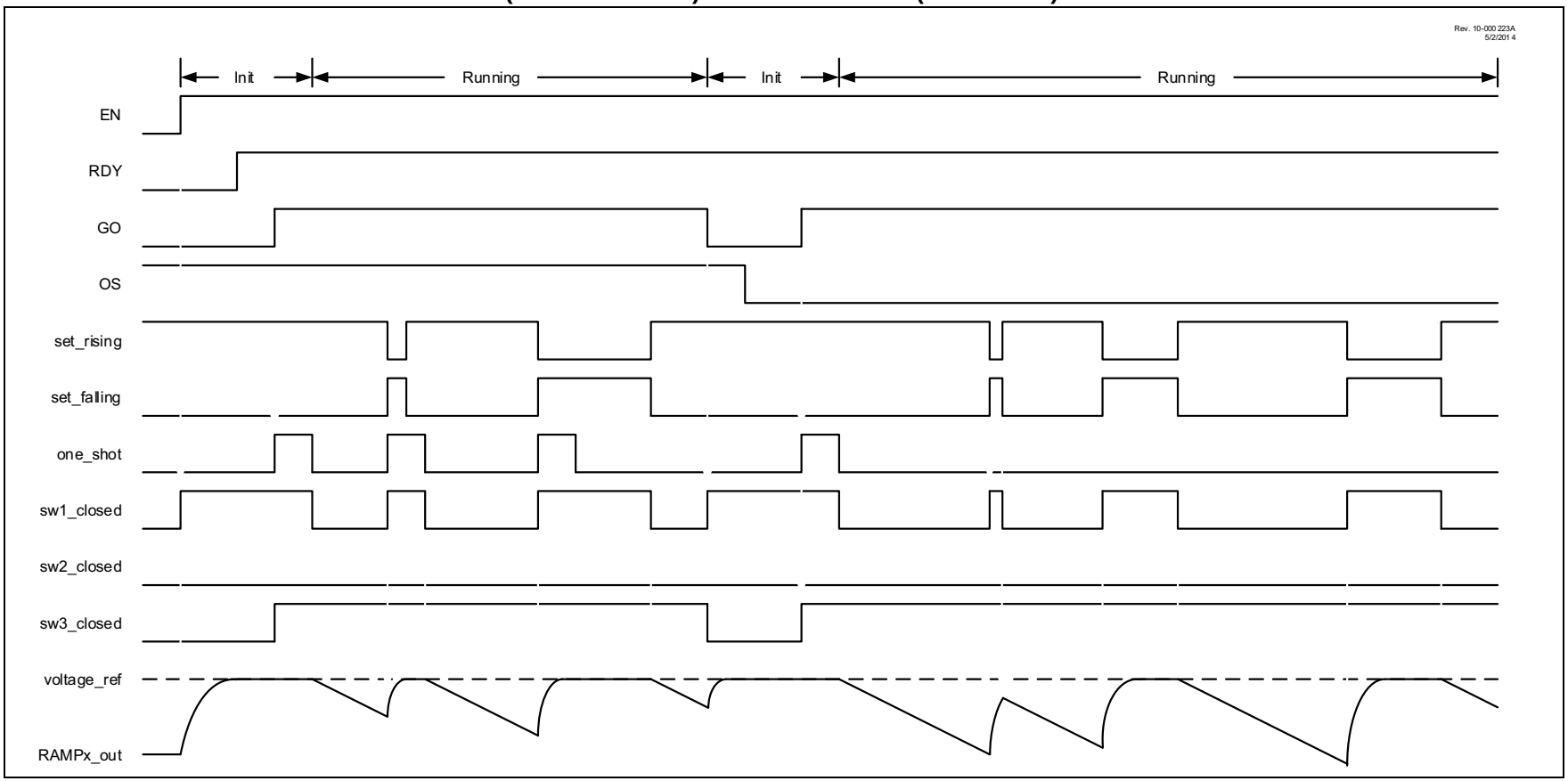


**TABLE 32-3: SUMMARY OF REGISTERS ASSOCIATED WITH $I^2C$ OPERATION**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset Values on Page: |
|---|---|---|---|---|---|---|---|---|---|
| ANSELA | — | — | ANSA5 | ANSA4 | ANSA3 | ANSA2 | ANSA1 | ANSA0 | 177 |
| ANSELB | — | — | ANSB5 | ANSB4 | ANSB3 | ANSB2 | ANSB1 | ANSB0 | 182 |
| ANSELC | ANSC7 | ANSC6 | ANSC5 | ANSC4 | ANSC3 | ANSC2 | — | — | 187 |
| INTCON | GIE | PEIE | TMR0IE | INTE | IOCIE | TMR0IF | INTF | IOCIF | 132 |
| PIE1 | TMR1GIE | ADIE | RCIE | TXIE | SSP1IE | CCP1IE | TMR2IE | TMR1IE | 133 |
| PIE2 | OSFIE | C2IE | C1IE | COG1IE | BCL1IE | C4IE | C3IE | CCP2IE | 134 |
| PIR1 | TMR1GIF | ADIF | RCIF | TXIF | SSP1IF | CCP1IF | TMR2IF | TMR1IF | 139 |
| PIR2 | OSFIF | C2IF | C1IF | COG1IF | BCL1IF | C4IF | C3IF | CCP2IF | 140 |
| RxyPPS | — | — | RxyPPS<5:0> | | | | | | 205 |
| SSPCLKPPS | — | — | SSPCLKPPS<5:0> | | | | | | 205, 207 |
| SSPDATPPS | — | — | SSPDATPPS<5:0> | | | | | | 205, 207 |
| SSPSSPPS | — | — | SSPSSPPS<5:0> | | | | | | 205, 207 |
| SSP1ADD | ADD<7:0> | | | | | | | | 492 |
| SSP1BUF | Synchronous Serial Port Receive Buffer/Transmit Register | | | | | | | | 444* |
| SSP1CON1 | WCOL | SSPOV | SSPEN | CKP | SSPM<3:0> | | | | 489 |
| SSP1CON2 | GCEN | ACKSTAT | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 490 |
| SSP1CON3 | ACKTIM | PCIE | SCIE | BOEN | SDAHT | SBCDE | AHEN | DHEN | 491 |
| SSP1MSK | MSK<7:0> | | | | | | | | 492 |
| SSP1STAT | SMP | CKE | D/$\overline{A}$ | P | S | R/$\overline{W}$ | UA | BF | 488 |
| TRISA | TRISA7 | TRISA6 | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | 176 |
| TRISB | TRISB7 | TRISB6 | TRISB5 | TRISB4 | TRISB3 | TRISB2 | TRISB1 | TRISB0 | 181 |
| TRISC | TRISC7 | TRISC6 | TRISC5 | TRISC4 | TRISC3 | TRISC2 | TRISC1 | TRISC0 | 186 |

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by the MSSP module in $I^2C$ mode.

* Page provides register information.

## 33.5 EUSART Synchronous Mode

Synchronous serial communications are typically used in systems with a single master and one or more slaves. The master device contains the necessary circuitry for baud rate generation and supplies the clock for all devices in the system. Slave devices can take advantage of the master clock by eliminating the internal clock generation circuitry.

There are two signal lines in Synchronous mode: a bidirectional data line and a clock line. Slaves use the external clock supplied by the master to shift the serial data into and out of their respective receive and transmit shift registers. Since the data line is bidirectional, synchronous operation is half-duplex only. Half-duplex refers to the fact that master and slave devices can receive and transmit data but not both simultaneously. The EUSART can operate as either a master or slave device.

Start and Stop bits are not used in synchronous transmissions.

### 33.5.1 SYNCHRONOUS MASTER MODE

The following bits are used to configure the EUSART for synchronous master operation:

- SYNC = 1
- CSRC = 1
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXxSTA register configures the device for synchronous operation. Setting the CSRC bit of the TXxSTA register configures the device as a master. Clearing the SREN and CREN bits of the RCxSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCxSTA register enables the EUSART.

#### 33.5.1.1 Master Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a master transmits the clock on the TX/CK line. The TX/CK pin output driver is automatically enabled when the EUSART is configured for synchronous transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One clock cycle is generated for each data bit. Only as many clock cycles are generated as there are data bits.

#### 33.5.1.2 Clock Polarity

A clock polarity option is provided for Microwire compatibility. Clock polarity is selected with the SCKP bit of the BAUDxCON register. Setting the SCKP bit sets the clock Idle state as high. When the SCKP bit is set, the data changes on the falling edge of each clock. Clearing the SCKP bit sets the Idle state as low. When the SCKP bit is cleared, the data changes on the rising edge of each clock.

#### 33.5.1.3 Synchronous Master Transmission

Data is transferred out of the device on the RX/DT pin. The RX/DT and TX/CK pin output drivers are automatically enabled when the EUSART is configured for synchronous master transmit operation.

A transmission is initiated by writing a character to the TXxREG register. If the TSR still contains all or part of a previous character the new character data is held in the TXxREG until the last bit of the previous character has been transmitted. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXxREG is immediately transferred to the TSR. The transmission of the character commences immediately following the transfer of the data to the TSR from the TXxREG.

Each data bit changes on the leading edge of the master clock and remains valid until the subsequent leading clock edge.

| **Note:** | The TSR register is not mapped in data memory, so it is not available to the user. |
|---|---|

#### 33.5.1.4 Synchronous Master Transmission Set-up:

1. Initialize the SPxBRGH:SPxBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 33.4 “EUSART Baud Rate Generator (BRG)”**).
2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
3. Disable Receive mode by clearing bits SREN and CREN.
4. Enable Transmit mode by setting the TXEN bit.
5. If 9-bit transmission is desired, set the TX9 bit.
6. If interrupts are desired, set the TXIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
7. If 9-bit transmission is selected, the ninth bit should be loaded in the TX9D bit.
8. Start transmission by loading data to the TXxREG register.

**TABLE 35-3: INSTRUCTION SET (CONTINUED)**

| Mnemonic, Operands | | Description | Cycles | 14-Bit Opcode MSb LSb | Status Affected | Notes |
|---|---|---|---|---|---|---|
| **CONTROL OPERATIONS** | | | | | | |
| BRA | k | Relative Branch | 2 | 11 001k kkkk kkkk | | |
| BRW | – | Relative Branch with W | 2 | 00 0000 0000 1011 | | |
| CALL | k | Call Subroutine | 2 | 10 0kkk kkkk kkkk | | |
| CALLW | – | Call Subroutine with W | 2 | 00 0000 0000 1010 | | |
| GOTO | k | Go to address | 2 | 10 1kkk kkkk kkkk | | |
| RETFIE | k | Return from interrupt | 2 | 00 0000 0000 1001 | | |
| RETLW | k | Return with literal in W | 2 | 11 0100 kkkk kkkk | | |
| RETURN | – | Return from Subroutine | 2 | 00 0000 0000 1000 | | |
| **INHERENT OPERATIONS** | | | | | | |
| CLRWDT | – | Clear Watchdog Timer | 1 | 00 0000 0110 0100 | $\overline{TO}$, $\overline{PD}$ | |
| NOP | – | No Operation | 1 | 00 0000 0000 0000 | | |
| OPTION | – | Load OPTION_REG register with W | 1 | 00 0000 0110 0010 | | |
| RESET | – | Software device Reset | 1 | 00 0000 0000 0001 | | |
| SLEEP | – | Go into Standby mode | 1 | 00 0000 0110 0011 | $\overline{TO}$, $\overline{PD}$ | |
| TRIS | f | Load TRIS register with W | 1 | 00 0000 0110 0fff | | |
| **C-COMPILER OPTIMIZED** | | | | | | |
| ADDFSR | n, k | Add Literal k to FSRn | 1 | 11 0001 0nkk kkkk | | |
| MOVIW | n mm | Move Indirect FSRn to W with pre/post inc/dec modifier, mm | 1 | 00 0000 0001 0nmm | Z | **2, 3** |
| | k[n] | Move INDFn to W, Indexed Indirect. | 1 | 11 1111 0nkk kkkk | Z | **2** |
| MOVWI | n mm | Move W to Indirect FSRn with pre/post inc/dec modifier, mm | 1 | 00 0000 0001 1nmm | | **2, 3** |
| | k[n] | Move W to INDFn, Indexed Indirect. | 1 | 11 1111 1nkk kkkk | | **2** |

**Note 1:** If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

**2:** If this instruction addresses an INDF register and the MSb of the corresponding FSR is set, this instruction will require one additional instruction cycle.

**3:** See Table in the MOVIW and MOVWI instruction descriptions.

## 36.4 AC Characteristics

Timing Parameter Symbology has been created with one of the following formats:

1. TppS2ppS
2. TppS

| | | | |
|---|---|---|---|
| **T** | | | |
| F | Frequency | T | Time |

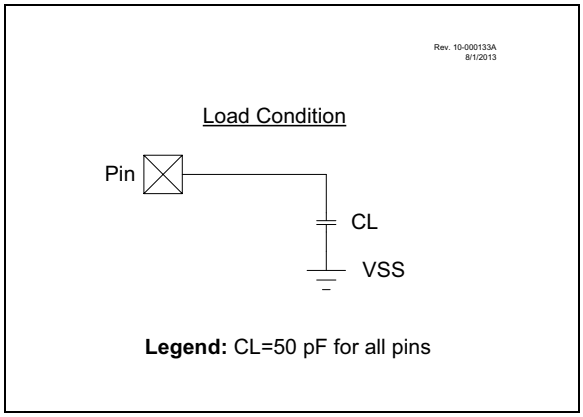
Lowercase letters (pp) and their meanings:

| | | | |
|---|---|---|---|
| **pp** | | | |
| cc | CCP1 | osc | OSC1 |
| ck | CLKOUT | rd | $\overline{RD}$ |
| cs | $\overline{CS}$ | rw | $\overline{RD}$ or $\overline{WR}$ |
| di | SDI | sc | SCK |
| do | SDO | ss | $\overline{SS}$ |
| dt | Data in | t0 | T0CKI |
| io | I/O PORT | t1 | T1CKI |
| mc | $\overline{MCLR}$ | wr | $\overline{WR}$ |

Uppercase letters and their meanings:

| | | | |
|---|---|---|---|
| **S** | | | |
| F | Fall | P | Period |
| H | High | R | Rise |
| I | Invalid (High-impedance) | V | Valid |
| L | Low | Z | High-impedance |

**FIGURE 36-4: LOAD CONDITIONS**




**Legend:** CL=50 pF for all pins

**TABLE 36-15: ANALOG-TO-DIGITAL CONVERTER (ADC) CHARACTERISTICS(1,2,3,4):**

| Operating Conditions (unless otherwise stated)<br>VDD = 3.0V, TA = 25°C, Single-ended, 2 μs TAD, VREF+ = 3V, VREF- = VSS | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| AD01 | NR | Resolution | — | — | 10 | bit | |
| AD02 | EIL | Integral Error | — | — | ±1.7 | LSb | VREF = 3.0V |
| AD03 | EDL | Differential Error | — | — | ±1 | LSb | No missing codes, VREF = 3.0V |
| AD04 | EOFF | Offset Error | — | — | ±2.5 | LSb | VREF = 3.0V |
| AD05 | EGN | Gain Error | — | — | ±2.0 | LSb | VREF = 3.0V |
| AD06 | VREF | Reference Voltage | 1.8 | — | VDD | V | VREF = (VREF+ minus VREF-) |
| AD07 | VAIN | Full-Scale Range | VSS | — | VREF | V | |
| AD08 | ZAIN | Recommended Impedance of Analog Voltage Source | — | — | 10 | kΩ | Can go higher if external 0.01μF capacitor is present on input pin. |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Total Absolute Error includes integral, differential, offset and gain errors.

**2:** The ADC conversion result never decreases with an increase in the input voltage and has no missing codes.

**3:** ADC VREF is from external VREF+ pin, VDD pin or FVR, whichever is selected as reference input.

**4:** See **Section 31.0 "DC and AC Characteristics Graphs and Charts"** for operating characterization.

**TABLE 36-16: ADC CONVERSION REQUIREMENTS**

| Standard Operating Conditions (unless otherwise stated) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| AD130* | TAD | ADC Clock Period (TADC) | 1.0 | — | 9.0 | μs | FOSC-based |
| | | ADC Internal FRC Oscillator Period (TFRC) | 1.0 | 2.5 | 6.0 | μs | ADCS<1:0> = 11 (ADC FRC mode) |
| AD131 | TCNV | Conversion Time (not including Acquisition Time)(1) | — | 13 | — | TAD | Set GO/$\overline{\text{DONE}}$ bit to conversion complete |
| AD132* | TACQ | Acquisition Time | — | 5.0 | — | μs | |
| AD133* | THCD | Holding Capacitor Disconnect Time | — | 1/2 TAD | — | | ADCS<2:0> ≠ x11 (FOSC-based) |
| | | | — | 1/2 TAD + 1TCY | — | | ADCS<2:0> = x11 (FRC-based) |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The ADRES register may be read on the following TCY cycle.

**Note:** Unless otherwise noted, $V_{IN}$ = 5V, $F_{OSC}$ = 300 kHz, $C_{IN}$ = 0.1 µF, $T_A$ = 25°C.

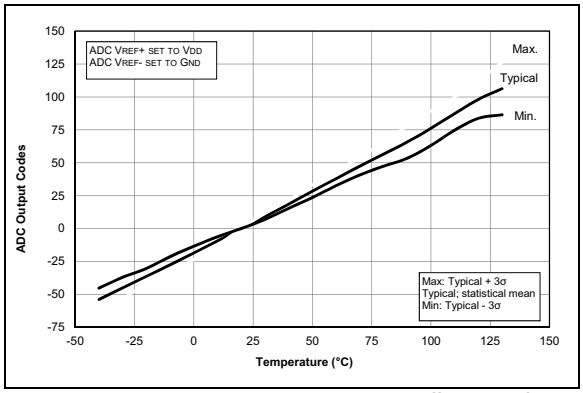



***FIGURE 37-91:*** *Temperature Indicator Slope Normalized to 20°C, Low Range, $V_{DD}$ = 3.0V, PIC16F1777/8/9 only.*

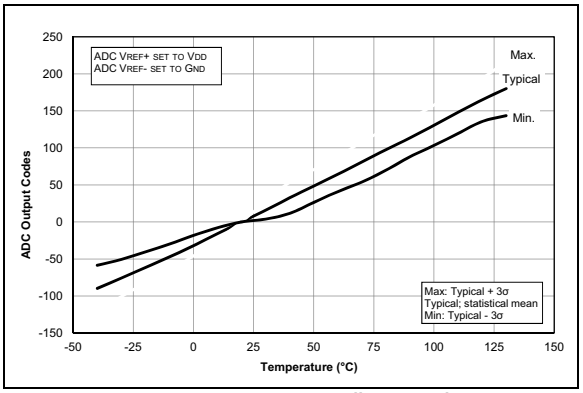



***FIGURE 37-92:*** *Temp. Indicator Slope Normalized to 20°C, Low Range, $V_{DD}$ = 1.8V, PIC16LF1773/6 Only.*

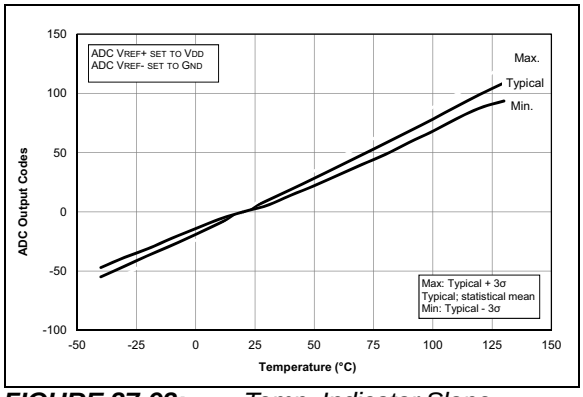



***FIGURE 37-93:*** *Temp. Indicator Slope Normalized to 20°C, Low Range, $V_{DD}$ = 3.0V, PIC16LF1773/6 Only.*

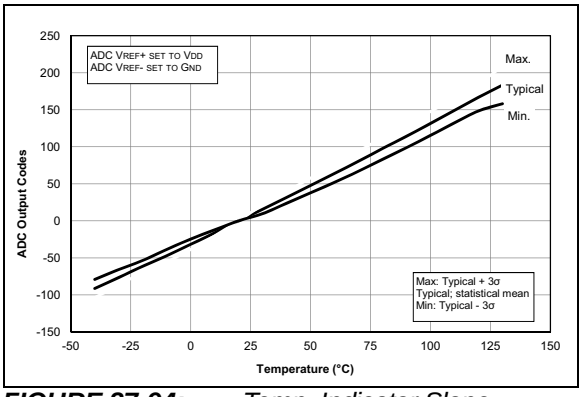



***FIGURE 37-94:*** *Temp. Indicator Slope Normalized to 20°C, High Range, $V_{DD}$ = 3.6V, PIC16LF1773/6 Only.*

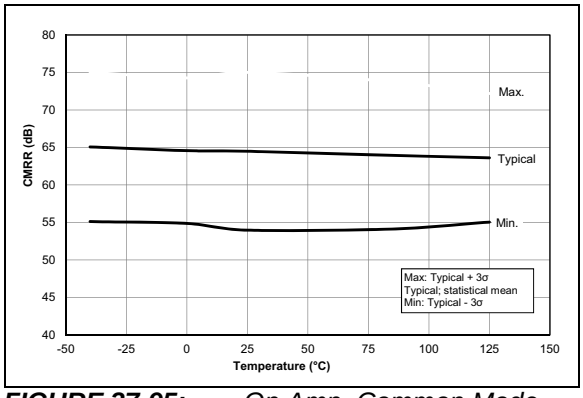



***FIGURE 37-95:*** *Op Amp, Common Mode Rejection Ratio (CMRR), $V_{DD}$ = 3.0V.*

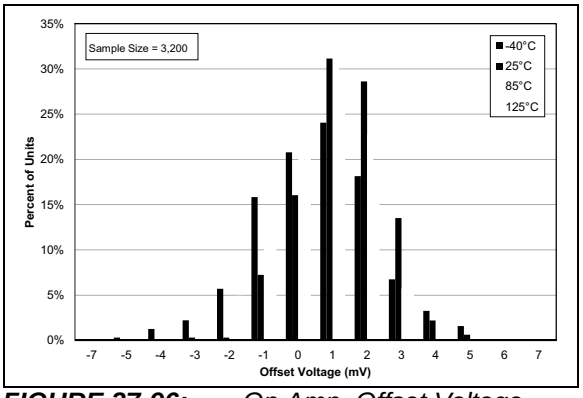



***FIGURE 37-96:*** *Op Amp, Offset Voltage Histogram, $V_{DD}$ = 3.0V, $V_{CM}$ = $V_{DD}$/2.*

**Note:** Unless otherwise noted, $V_{IN}$ = 5V, $F_{OSC}$ = 300 kHz, $C_{IN}$ = 0.1 µF, $T_A$ = 25°C.

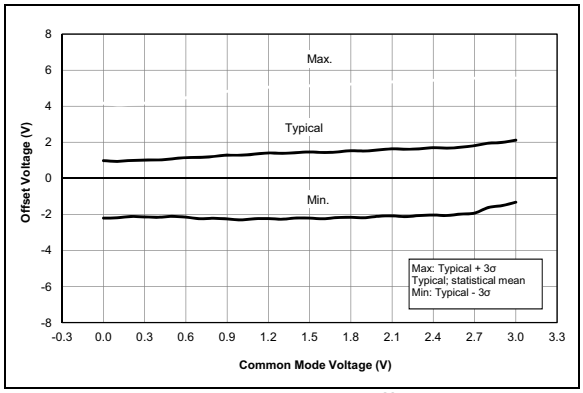



***FIGURE 37-97:*** *Op Amp, Offset over Common Mode Voltage, $V_{DD}$ = 3.0V, Temp. = 25°C*

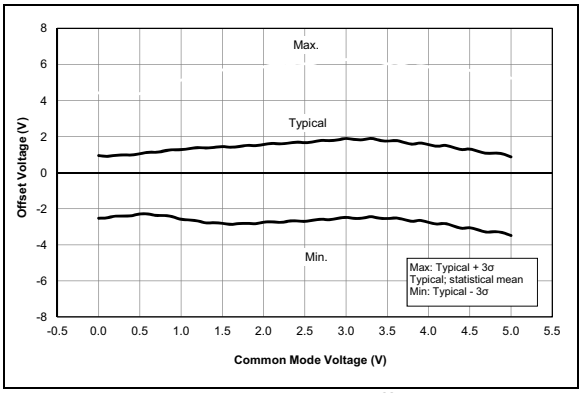



***FIGURE 37-98:*** *Op Amp, Offset over Common Mode Voltage, $V_{DD}$ = 5.0V, Temp. = 25°C, PIC16F1777/8/9 Only.*

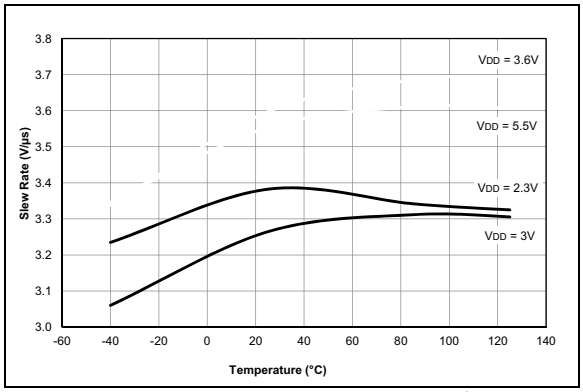



***FIGURE 37-99:*** *Op Amp, Output Slew Rate, Rising Edge, PIC16F1777/8/9 Only.*

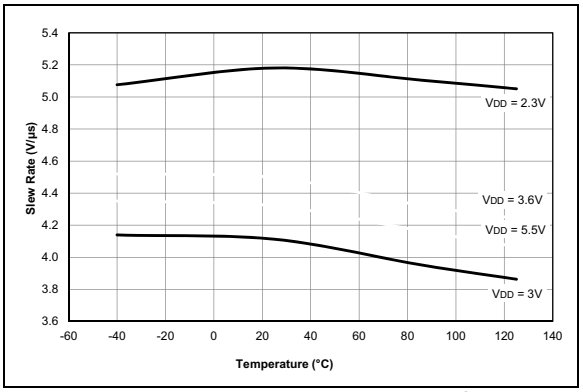



***FIGURE 37-100:*** *Op Amp, Output Slew Rate, Falling Edge, PIC16F1777/8/9 Only.*

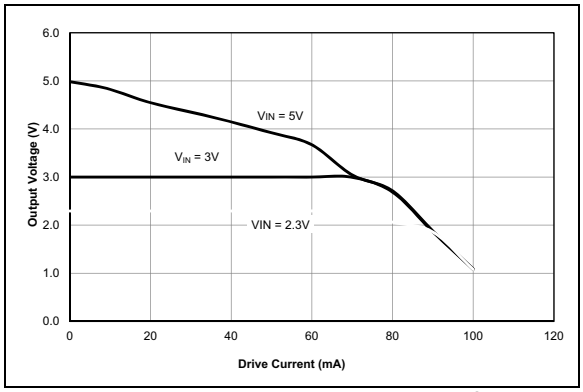



***FIGURE 37-101:*** *Op Amp, Output Drive Strength, $V_{DD}$ = 5.0V, Temp. = 25°C, PIC16F1777/8/9 Only.*

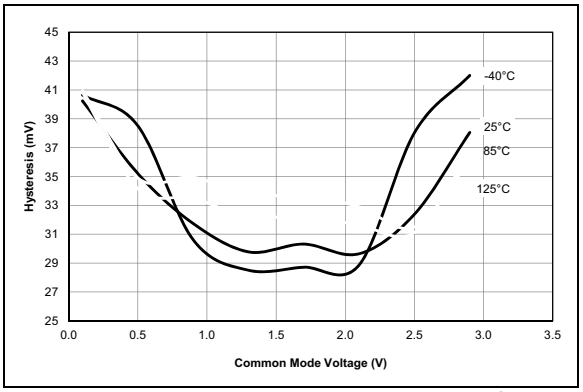



***FIGURE 37-102:*** *Comparator Hysteresis, NP Mode (CxSP = 1), $V_{DD}$ = 3.0V, Typical Measured Values.*