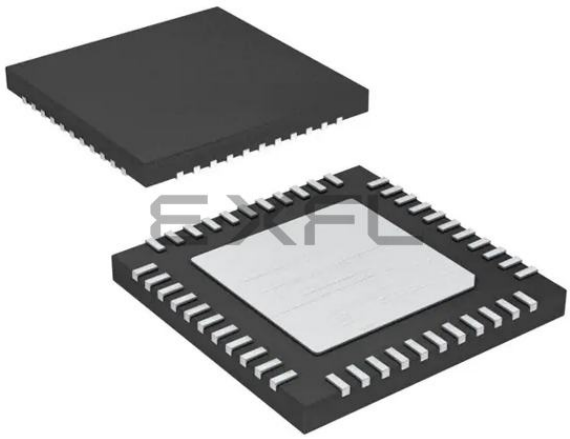

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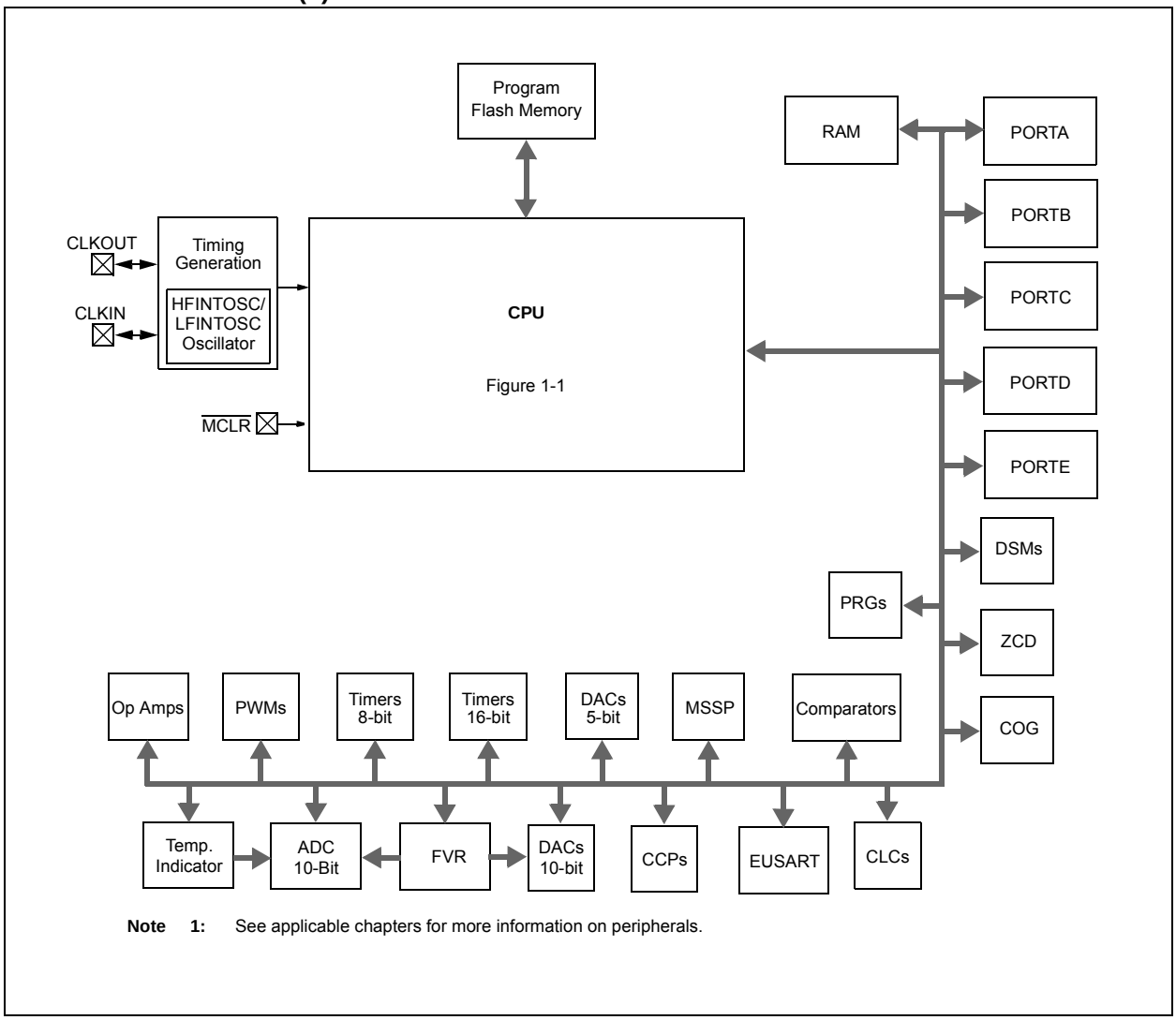
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x10b; D/A 4x5b, 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1779-i-ml

FIGURE 1-1: PIC16(L)F1777/8/9 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.

3.4.5 CORE FUNCTION REGISTERS SUMMARY

The Core Function registers listed in Table 3-17 can be addressed from any Bank.

TABLE 3-17: CORE FUNCTION REGISTERS SUMMARY(1)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 0-31											
x00h or x80h	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
x01h or x81h	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
x02h or x82h	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
x03h or x83h	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
x04h or x84h	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
x05h or x85h	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
x06h or x86h	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
x07h or x87h	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
x08h or x88h	BSR	—	—	—	BSR4	BSR3	BSR2	BSR1	BSR0	---0 0000	---0 0000
x09h or x89h	WREG	Working Register								0000 0000	uuuu uuuu
x0Ah or x8Ah	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
x0Bh or x8Bh	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

TABLE 3-18: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 28 (Continued)											
E27h	MD3CLPPS	—	—	MD3CLPPS<5:0>						--00 1100	--uu uuuu
E28h	MD3CHPPS	—	—	MD3CHPPS<5:0>						--00 1011	--uu uuuu
E29h	MD3MODPPS	—	—	MD3MODPPS<5:0>						--00 0101	--uu uuuu
E2Ah	MD4CLPPS(3)	—	—	MD4CLPPS<5:0>						--00 1100	--uu uuuu
E2Bh	MD4CHPPS(3)	—	—	MD4CHPPS<5:0>						--00 1011	--uu uuuu
E2Ch	MD4MODPPS(3)	—	—	MD4MODPPS<5:0>						--00 0101	--uu uuuu
E2Dh	PRG1RPPS	—	—	PRG1RPPS<5:0>						--00 0100	--uu uuuu
E2Eh	PRG1FPPS	—	—	PRG1FPPS<5:0>						--00 0101	--uu uuuu
E2Fh	PRG2RPPS	—	—	PRG2RPPS<5:0>						--01 0001	--uu uuuu
E30h	PRG2FPPS	—	—	PRG2FPPS<5:0>						--01 0010	--uu uuuu
E31h	PRG3RPPS	—	—	PRG3RPPS<5:0>						--01 0100	--uu uuuu
E32h	PRG3FPPS	—	—	PRG3FPPS<5:0>						--01 0101	--uu uuuu
E33h	PRG4RPPS(3)	—	—	PRG4RPPS<5:0>						--01 0100	--uu uuuu
E34h	PRG4FPPS(3)	—	—	PRG4FPPS<5:0>						--01 0101	--uu uuuu
E35h	CLC1IN0PPS	—	—	CLCIN0PPS<5:0>						--00 0000	--uu uuuu
E36h	CLC1IN1PPS	—	—	CLCIN1PPS<5:0>						--00 0001	--uu uuuu
E37h	CLC1IN2PPS	—	—	CLCIN2PPS<5:0>						--00 1110	--uu uuuu
E38h	CLC1IN3PPS	—	—	CLCIN3PPS<5:0>						--00 1111	--uu uuuu
E39h	ADCACTPPS	—	—	ADCACTPPS<5:0>						--00 1100	--uu uuuu
E3Ah	SSPCLKPPS	—	—	SSPCLKPPS<5:0>						--01 0011	--uu uuuu
E3Bh	SSPDATPPS	—	—	SSPDATPPS<5:0>						--01 0100	--uu uuuu
E3Ch	SSPSSPPS	—	—	SSPSSPPS<5:0>						--00 0101	--uu uuuu
E3Dh	RXPPS	—	—	RXPPS<5:0>						--01 0111	--uu uuuu
E3Eh	CKPPS	—	—	CKPPS<5:0>						--01 0110	--uu uuuu
E3Fh — E6Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: Unimplemented on PIC16LF1777/8/9.
3: Unimplemented on PIC16(L)F1778.

REGISTER 7-5: PIE4: PERIPHERAL INTERRUPT ENABLE REGISTER 4

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	TMR8IE	TMR5GIE	TMR5IE	TMR3GIE	TMR3IE	TMR6IE	TRM4IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **TMR8IE:** TMR8 to T8PR Match Interrupt Enable bit
1 = Enables the Timer8 to T8PR match interrupt
0 = Disables the Timer8 to T8PR match interrupt

bit 5 **TMR5GIE:** Timer5 Gate Interrupt Enable bit
1 = Enables the Timer5 gate acquisition interrupt
0 = Disables the Timer5 gate acquisition interrupt

bit 4 **TMR5IE:** TMR5 to Overflow Interrupt Enable bit
1 = Enables the Timer5 to T5PR match interrupt
0 = Disables the Timer5 to T5PR match interrupt

bit 3 **TMR3GIE:** Timer3 Gate Interrupt Enable bit
1 = Enables the Timer3 gate acquisition interrupt
0 = Disables the Timer3 gate acquisition interrupt

bit 2 **TMR3IE:** TMR3 to Overflow Interrupt Enable bit
1 = Enables the Timer3 to T3PR match interrupt
0 = Disables the Timer3 to T3PR match interrupt

bit 1 **TMR6IE:** TMR6 to T6PR Match Interrupt Enable bit
1 = Enables the Timer6 to T6PR match interrupt
0 = Disables the Timer6 to T6PR match interrupt

bit 0 **TMR4IE:** TMR4 to T4PR Match Interrupt Enable bit
1 = Enables the Timer4 to T4PR match interrupt
0 = Disables the Timer4 to T4PR match interrupt

REGISTER 7-12: PIR5: PERIPHERAL INTERRUPT REQUEST REGISTER 5

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
CCP8IF(1)	CCP7IF	COG4IF	COG3IF	C8IF(1)	C7IF(1)	C6IF	C5IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **CCP8IF:** CCP8 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 6 **CCP7IF:** CCP7 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 5 **COG4IF:** COG4 Auto-Shutdown Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 4 **COG3IF:** COG3 Auto-Shutdown Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 3 **C8IF:** Comparator C8 Interrupt Flag bit(1)
1 = Interrupt is pending
0 = Interrupt is not pending

bit 2 **C7IF:** Comparator C7 Interrupt Flag bit(1)
1 = Interrupt is pending
0 = Interrupt is not pending

bit 1 **C6IF:** Comparator C6 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 0 **C5IF:** Comparator C5 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

Note 1: PIC16(L)F1777/9 only.

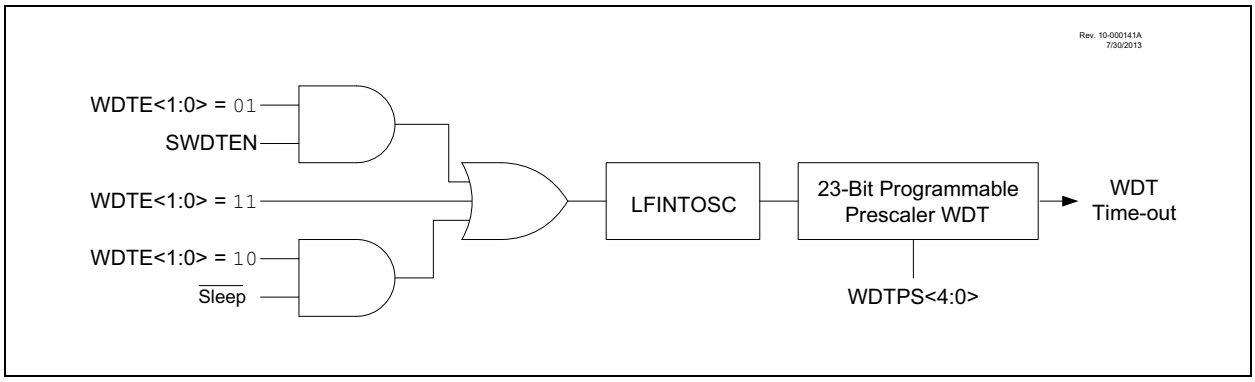
9.0 WATCHDOG TIMER (WDT)

The Watchdog Timer is a system timer that generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events.

The WDT has the following features:

- Independent clock source
- Multiple operating modes
  - WDT is always on
  - WDT is off when in Sleep
  - WDT is controlled by software
  - WDT is always off
- Configurable time-out period is from 1 ms to 256 seconds (nominal)
- Multiple Reset conditions
- Operation during Sleep

FIGURE 9-1: WATCHDOG TIMER BLOCK DIAGRAM



REGISTER 13-6: IOCBF: INTERRUPT-ON-CHANGE PORTB FLAG REGISTER

R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
IOCBF7	IOCBF6	IOCBF5	IOCBF4	IOCBF3	IOCBF2	IOCBF1	IOCBF0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HS - Bit is set in hardware

bit 7-0 **IOCBF<7:0>:** Interrupt-on-Change PORTB Flag bits

1 = An enabled change was detected on the associated pin.
Set when IOCBPx = 1 and a rising edge was detected on RBx, or when IOCBNx = 1 and a falling edge was detected on RBx.

0 = No change was detected, or the user cleared the detected change.

20.5.2 CORRECTION BY OFFSET CURRENT

When the waveform is varying relative to Vss then the zero cross is detected too early as the waveform falls and too late as the waveform rises. When the waveform is varying relative to VDD then the zero cross is detected too late as the waveform rises and too early as the waveform falls. The actual offset time can be determined for sinusoidal waveforms with the corresponding equations shown in Equation 20-4.

EQUATION 20-4: ZCD EVENT OFFSET

When External Voltage Source is relative to Vss:

$$T_{offset} = \frac{\text{asin}\left(\frac{Z_{cpinv}}{V_{peak}}\right)}{2\pi \bullet Freq}$$

When External Voltage Source is relative to VDD:

$$T_{offset} = \frac{\text{asin}\left(\frac{V_{DD}-Z_{cpinv}}{V_{peak}}\right)}{2\pi \bullet Freq}$$

This offset time can be compensated for by adding a pull-up or pull-down biasing resistor to the ZCD pin. A pull-up resistor is used when the external voltage source is varying relative to Vss. A pull-down resistor is used when the voltage is varying relative to VDD.The resistor adds a bias to the ZCD pin so that the target external voltage source must go to zero to pull the pin voltage to the ZCPINV switching voltage. The pull-up or pull-down value can be determined with the equations shown in Equation 20-5.

EQUATION 20-5: ZCD PULL-UP/DOWN

When External Signal is relative to Vss:

$$R_{pullup} = \frac{R_{series}(V_{pullup} - Z_{cpinv})}{Z_{cpinv}}$$

When External Signal is relative to VDD:

$$R_{pulldown} = \frac{R_{series}(Z_{cpinv})}{(V_{DD} - Z_{cpinv})}$$

The pull-up and pull-down resistor values are significantly affected by small variations of ZCPINV. Measuring ZCPINV can be difficult, especially when the waveform is relative to VDD. However, by combining Equation 20-4 and Equation 20-5 the resistor value can be determined from the time difference between the ZCDOUT high and low periods. Note that the time difference, ΔT, is $4*T_{offset}$. The equation for determining the pull-up and pull-down resistor values from the high and low ZCDOUT periods is shown in Equation 20-6. The ZCDOUT signal can be directly observed on a pin by routing the ZCDOUT signal through one of the CLCs.

EQUATION 20-6:

$$R = R_{series}\left(\frac{V_{bias}}{V_{peak}\left(\sin\left(\pi Freq\frac{(\Delta T)}{2}\right)\right)} - 1\right)$$

R is pull-up or pull-down resistor

V_{bias} is V_{pullup} when R is pull-up or VDD when R is pull-down

ΔT is the ZCDOUT high and low period difference

20.6 Handling V_{peak} variations

If the peak amplitude of the external voltage is expected to vary then the series resistor must be selected to keep the ZCD current source and sink below the design maximum range of ± 600 µA for the maximum expected voltage and high enough to be detected accurately at the minimum peak voltage. A general rule of thumb is that the maximum peak voltage can be no more than six times the minimum peak voltage. To ensure that the maximum current does not exceed ± 600 µA and the minimum is at least ± 100 µA, compute the series resistance as shown in Equation 20-7. The compensating pull-up for this series resistance can be determined with Equation 20-5 because the pull-up value is independent from the peak voltage.

EQUATION 20-7: SERIES R FOR V RANGE

$$R_{series} = \frac{V_{maxpeak} + V_{minpeak}}{7\times10^{-4}}$$

22.7 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt-on-rollover, you must set these bits:

- ON bit of the T1CON register
- TMR1IE bit of the PIE1 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

Note:	The TMR1H:TMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

22.8 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set
- $\overline{\text{SYNC}}$ bit of the T1CON register must be set
- CS bits of the T1CON register must be configured
- OSCEN bit of the T1CON register must be configured

The device will wake-up on an overflow and execute the next instructions. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine.

Secondary oscillator will continue to operate in Sleep regardless of the $\overline{\text{SYNC}}$ bit setting.

22.9 CCP Capture/Compare Time Base

The CCP modules use the TMR1H:TMR1L register pair as the time base when operating in Capture or Compare mode.

In Capture mode, the value in the TMR1H:TMR1L register pair is copied into the CCPR1H:CCPR1L register pair on a configured event.

In Compare mode, an event is triggered when the value in the CCPR1H:CCPR1L register pair matches the value in the TMR1H:TMR1L register pair. This event can be an Auto-conversion Trigger.

For more information, see **Section 24.0 "Capture/Compare/PWM Modules"**.

22.10 CCP Auto-Conversion Trigger

When any of the CCP's are configured to trigger an auto-conversion, the trigger will clear the TMR1H:TMR1L register pair. This auto-conversion does not cause a Timer1 interrupt. The CCP module may still be configured to generate a CCP interrupt.

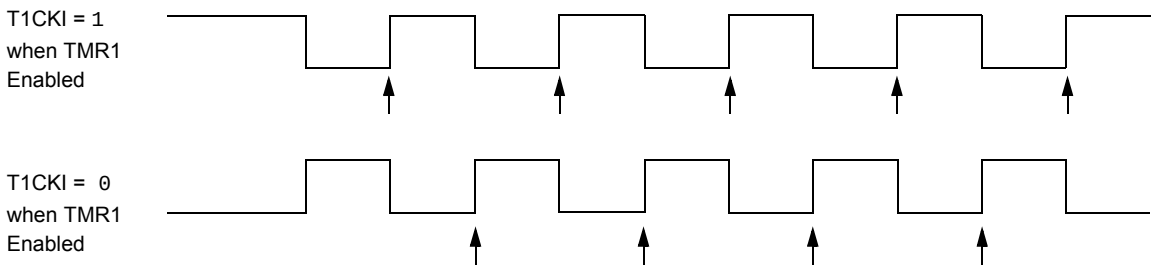
In this mode of operation, the CCPR1H:CCPR1L register pair becomes the period register for Timer1.

Timer1 should be synchronized and FOSC/4 should be selected as the clock source in order to utilize the Auto-conversion Trigger. Asynchronous operation of Timer1 can cause an Auto-conversion Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with an Auto-conversion Trigger from the CCP, the write will take precedence.

For more information, see **Section 24.2.1 "Auto-Conversion Trigger"**.

FIGURE 22-2: TIMER1 INCREMENTING EDGE



Note 1: Arrows indicate counter increments.

2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

24.2 Compare Mode

The Compare mode function described in this section is available and identical for all CCP modules.

Compare mode makes use of the 16-bit Timer1 resource. The 16-bit value of the CCPRxH:CCPRxL register pair is constantly compared against the 16-bit value of the TMR1H:TMR1L register pair. When a match occurs, one of the following events can occur:

- Toggle the CCPx output
- Set the CCPx output
- Clear the CCPx output
- Pulse the CCPx output
- Generate a Software Interrupt
- Auto-conversion Trigger

The action on the pin is based on the value of the MODE<3:0> control bits of the CCPxCON register. At the same time, the interrupt flag CCPxIF bit is set.

All Compare modes can generate an interrupt.

Figure 24-2 shows a simplified diagram of the compare operation.

24.2.1 AUTO-CONVERSION TRIGGER

When Auto-Conversion Trigger mode is chosen (CCPxM<3:0> = 1011), the CCPx module does the following:

- Resets Timer1
- Starts an ADC conversion if ADC is enabled

The CCPx module does not assert control of the CCPx pin in this mode.

The Auto-conversion Trigger output of the CCP occurs immediately upon a match between the TMR1H, TMR1L register pair and the CCPRxH:CCPRxL register pair. The TMR1H:TMR1L register pair is not reset until the next rising edge of the Timer1 clock. The Auto-conversion Trigger output starts an ADC conversion (if the ADC module is enabled). This allows the CCPRxH:CCPRxL register pair to effectively provide a 16-bit programmable period register for Timer1.

Refer to **Section 16.2.5 "Auto-Conversion Trigger"** for more information.

Note 1:	The Auto-conversion Trigger from the CCP module does not set interrupt flag bit TMR1IF of the PIR1 register.
2:	Removing the match condition by changing the contents of the CCPRxH and CCPRxL register pair, between the clock edge that generates the Auto-conversion Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring.

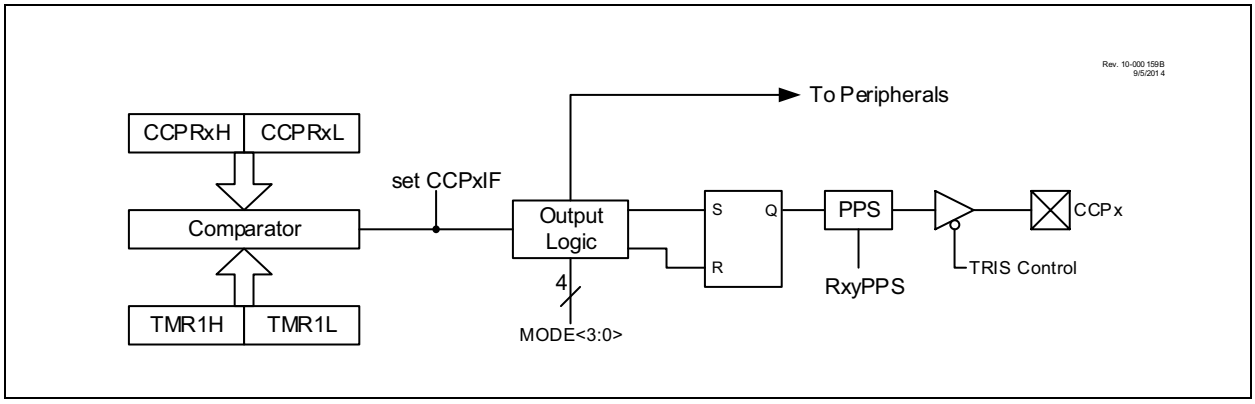
24.2.2 CCPx PIN CONFIGURATION

The user must configure the CCPx pin as an output by clearing the associated TRIS bit.

The CCPx pin function can be moved to alternate pins using the PPS controls. See **Section 12.0 "Peripheral Pin Select (PPS) Module"** for more detail.

Note:	Clearing the CCPxCON register will force the CCPx compare output latch to the default low level. This is not the PORT I/O data latch.

FIGURE 24-2: COMPARE MODE OPERATION BLOCK DIAGRAM



REGISTER 24-4: CCPxCAP: CCPx CAPTURE INPUT SELECTION REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	CTS<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Reset
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **CTS<3:0>:** Capture Trigger Input Selection bits

1101 = IOC_event
1100 = LC4_output
1011 = LC3_output
1010 = LC2_output
1001 = LC1_output
1000 = C8_sync_out(1)
0111 = C7_sync_out(1)
0110 = C6_sync_out
0101 = C5_sync_out
0100 = C4_sync_out
0011 = C3_sync_out
0010 = C2_sync_out
0001 = C1_sync_out
0000 = Pin selected with the CCPxPPS register

Note 1: PIC16LF1777/9 only.

26.7 Register Definitions: PWM Control

Long bit name prefixes for the 16-bit PWM peripherals are shown in Table 26-2. Refer to **Section 1.1 "Register and Bit naming conventions"** for more information

TABLE 26-2:

Peripheral	Bit Name Prefix
PWM5	PWM5
PWM6	PWM6
PWM11	PWM11
PWM12(1)	PWM12

Note 1: PIC16(L)F1777/9 only.

REGISTER 26-1: PWMxCON: PWM CONTROL REGISTER

R/W-0/0	U-0	R/HS/HC-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0
EN	—	OUT	POL	MODE<1:0>		—	—
bit 7							bit 0

Legend:		
HC = Bit is cleared by hardware		HS = Bit is set by hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **EN:** PWM Module Enable bit
1 = Module is enabled
0 = Module is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **OUT:** Output State of the PWM module

bit 4 **POL:** PWM Output Polarity Control bit
1 = PWM output active state is low
0 = PWM output active state is high

bit 3-2 **MODE<1:0>:** PWM Mode Control bits
11 = Center Aligned mode
10 = Toggle On Match mode
01 = Set On Match mode
00 = Standard PWM mode

bit 1-0 **Unimplemented:** Read as '0'

REGISTER 26-9: PWMxDCH: PWMx DUTY CYCLE COUNT HIGH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
DC<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **DC<15:8>**: PWM Duty Cycle High bits
Upper eight bits of PWM duty cycle count

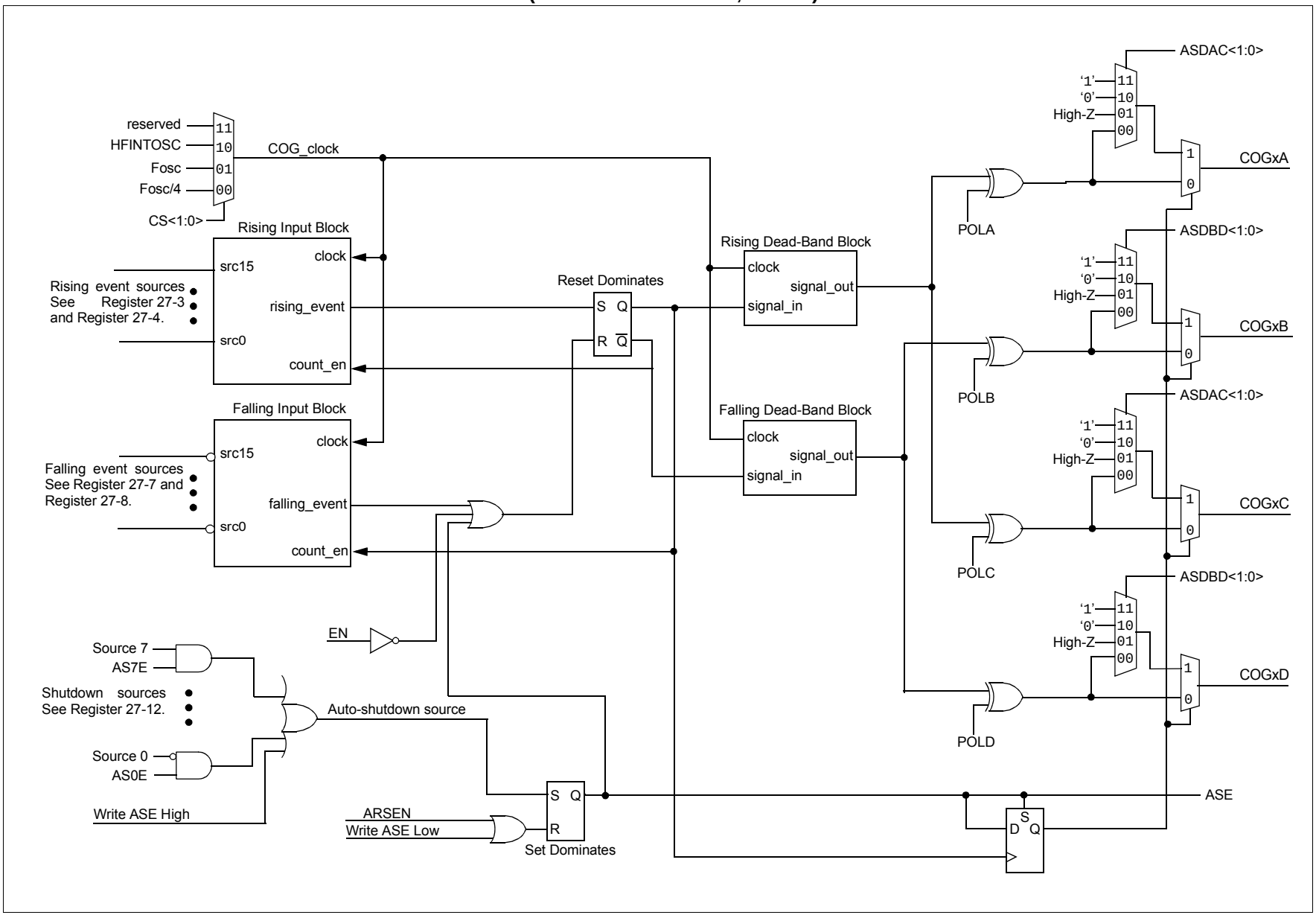
REGISTER 26-10: PWMxDCL: PWMx DUTY CYCLE COUNT LOW REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
DC<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **DC<7:0>**: PWM Duty Cycle Low bits
Lower eight bits of PWM duty cycle count

FIGURE 27-5: SIMPLIFIED COG BLOCK DIAGRAM (HALF-BRIDGE MODE, MD = 4)



REGISTER 27-18: COGxPHR: COG RISING EVENT PHASE DELAY COUNT REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	PHR<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **PHR<5:0>:** Rising Event Phase Delay Count Value bits
= Number of COGx clock periods to delay rising event

REGISTER 27-19: COGxPHF: COG FALLING EVENT PHASE DELAY COUNT REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	PHF<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **PHF<5:0>:** Falling Event Phase Delay Count Value bits
= Number of COGx clock periods to delay falling event

REGISTER 30-2: PRGxCON1: PROGRAMMABLE RAMP GENERATOR CONTROL 1 REGISTER

U-0	U-0	U-0	U-0	U-0	R-0	R/W-0/0	R/W-0/0
—	—	—	—	—	RDY	FPOL	RPOL
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = value depends on configuration bits

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **RDY:** Slope Generator Ready Status bit
1 = PRG is ready
0 = PRG is not ready

bit 1 **FPOL:** Fall Event Polarity Select bit
1 = Set_falling timing input is active-low
0 = Set_falling timing input is active-high

bit 0 **RPOL:** Rise Event Polarity Select bit
1 = Set_rising timing input is active-low
0 = Set_rising timing input is active-high

REGISTER 30-3: PRGxINS: VOLTAGE INPUT SELECT REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	INS<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = value depends on configuration bits

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **INS<3:0>:** Voltage Input Select bits
Selects source of voltage level at which the ramp starts. See Table 30-3.

TABLE 30-3: VOLTAGE INPUT SOURCES

INS<2:0>	PRG1 Voltage Source	PRG2 Voltage Source	PRG3 Voltage Source	PRG4 Voltage Source(2)
1010-1111	Reserved	Reserved	Reserved	Reserved
1001(1)	Switched PRG1IN1/OPA2OUT	Switched PRG1IN1/OPA2OUT	Switched PRG3IN1/OPA4OUT(2)	Switched PRG4IN1/OPA3OUT
1000(1)	Switched PRG1IN0/OPA1OUT	Switched PRG1IN0/OPA1OUT	Switched PRG3IN0/OPA3OUT	Switched PRG4IN0/OPA4OUT
0111	Reserved	Reserved	Reserved	Reserved
0110	DAC4_output	DAC4_output	DAC8_output(2)	DAC8_output
0101	DAC3_output	DAC3_output	DAC7_output	DAC7_output
0100	DAC2_output	DAC2_output	DAC6_output(2)	DAC6_output
0011	DAC1_output	DAC1_output	DAC5_output	DAC5_output
0010	FVR_buffer1	FVR_buffer1	FVR_buffer2	FVR_buffer2
0001	PRG1IN1/OPA2OUT	PRG2IN1/OPA1OUT	PRG3IN1/OPA4OUT(2)	PRG4IN1/OPA3OUT
0000	PRG1IN0/OPA1OUT	PRG2IN0/OPA2OUT	PRG3IN0/OPA3OUT	PRG4IN0/OPA4OUT

Note 1: Input source is switched off when op amp override is forcing tri-state. See **Section 29.3 "Override Control"**.
2: PIC16(L)F1777/9 only.

DECFSZ **Decrement f, Skip if 0**

Syntax:	[*label*] DECFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 → (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a 2-cycle instruction.

GOTO **Unconditional Branch**

Syntax:	[*label*] GOTO k
Operands:	$0 \le k \le 2047$
Operation:	k → PC<10:0> PCLATH<6:3> → PC<14:11>
Status Affected:	None
Description:	GOTO is an unconditional branch. The 11-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a 2-cycle instruction.

INCF **Increment f**

Syntax:	[*label*] INCF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 → (destination)
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

INCFSZ **Increment f, Skip if 0**

Syntax:	[*label*] INCFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 → (destination), skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2-cycle instruction.

IORLW **Inclusive OR literal with W**

Syntax:	[*label*] IORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .OR. k → (W)
Status Affected:	Z
Description:	The contents of the W register are OR'ed with the 8-bit literal 'k'. The result is placed in the W register.

IORWF **Inclusive OR W with f**

Syntax:	[*label*] IORWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .OR. (f) → (destination)
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

36.0 ELECTRICAL SPECIFICATIONS

36.1 Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on pins with respect to V_{SS}
- on V_{DD} pin
  - PIC16F1777/8/9 ..... -0.3V to +6.5V
  - PIC16LF1777/8/9 ..... -0.3V to +4.0V
- on $\overline{MCLR}$ pin ..... -0.3V to +9.0V
- on all other pins ..... -0.3V to (V_{DD} + 0.3V)

Maximum current
- on V_{SS} pin(1)
  - -40°C ≤ T_A ≤ +85°C ..... 350 mA
  - -40°C ≤ T_A ≤ +125°C ..... 120 mA
- on V_{DD} pin(1) PIC16(L)F1778 only
  - -40°C ≤ T_A ≤ +85°C ..... 250 mA
  - -40°C ≤ T_A ≤ +125°C ..... 85 mA
- on V_{DD} pin(1) PIC16(L)F1777/9 only
  - -40°C ≤ T_A ≤ +85°C ..... 350 mA
  - -40°C ≤ T_A ≤ +125°C ..... 120 mA
- Sunk by any standard I/O pin ..... 50 mA
- Sourced by any standard I/O pin ..... 50 mA
- Sunk by any High Current I/O pin ..... 100 mA
- Sourced by any High Current I/O pin ..... 100 mA
- Sourced by any Op Amp output pin ..... 100 mA

Clamp current, I_K (V_{PIN} < 0 or V_{PIN} > V_{DD}) ..... ±20 mA
Total power dissipation(2) ..... 800 mW

Note 1: Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characterizations, see Table 36-6: Thermal Characteristics to calculate device specifications.

2: Power dissipation is calculated as follows:

$Pdis = V_{DD} * \{Idd - \Sigma Ioh\} + \Sigma\{V_{DD} - Voh) * Ioh\} + \Sigma(Vol * Iol)$.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

TABLE 36-11: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
30	TMCL	$\overline{MCLR}$ Pulse Width (low)	2	—	—	μs	
31	TWDTLP	Low-Power Watchdog Timer Time-out Period	10	16	27	ms	VDD = 3.3V-5V 1:512 Prescaler used
32	TOST	Oscillator Start-up Timer Period(1)	—	1024	—	Tosc	
33*	TPWRT	Power-up Timer Period, $\overline{PWRTE}$ = 0	40	65	140	ms	
34*	TIOZ	I/O high-impedance from $\overline{MCLR}$ Low or Watchdog Timer Reset	—	—	2.0	μs	
35	VBOR	Brown-out Reset Voltage(2)	2.55 2.30 1.80	2.70 2.45 1.90	2.85 2.60 2.10	V V V	BORV = 0 BORV = 1 (PIC16F1777/8/9) BORV = 1 (PIC16LF1777/8/9)
35A	VLPBOR	Low-Power Brown-out	1.8	2.1	2.5	V	LPBOR = 1
36*	VHYST	Brown-out Reset Hysteresis	0	25	75	mV	-40°C ≤ TA ≤ +85°C
37*	TBORDC	Brown-out Reset DC Response Time	1	3	35	μs	VDD ≤ VBOR

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: By design, the Oscillator Start-up Timer (OST) counts the first 1024 cycles, independent of frequency.

2: To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

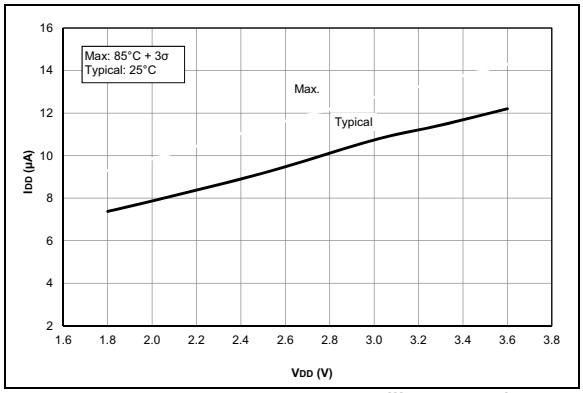


FIGURE 37-1: *IDD, LP Oscillator Mode, Fosc = 32 kHz, PIC16LF1777/8/9 Only.*

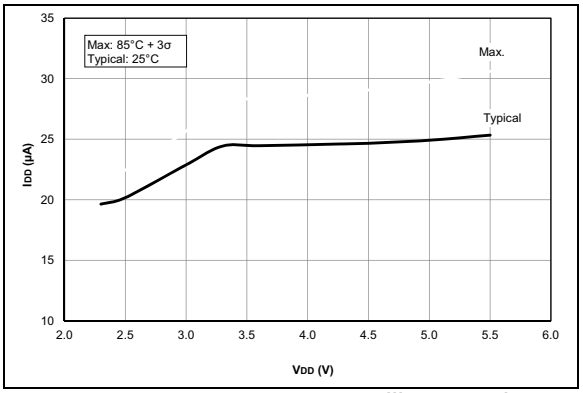


FIGURE 37-2: *IDD, LP Oscillator Mode, Fosc = 32 kHz, PIC16F1777/8/9 Only.*

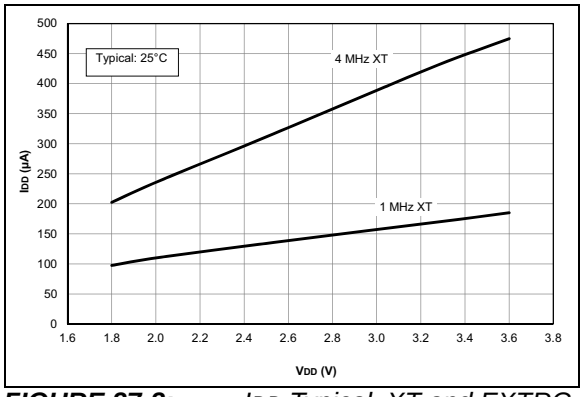


FIGURE 37-3: *IDD Typical, XT and EXTRC Oscillator, PIC16LF1777/8/9 Only.*

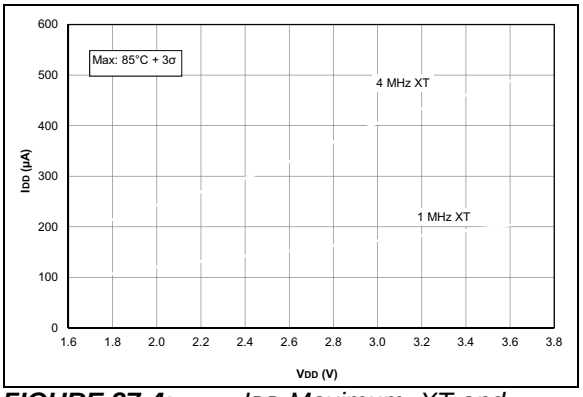


FIGURE 37-4: *IDD Maximum, XT and EXTRC Oscillator, PIC16LF1777/8/9 Only.*

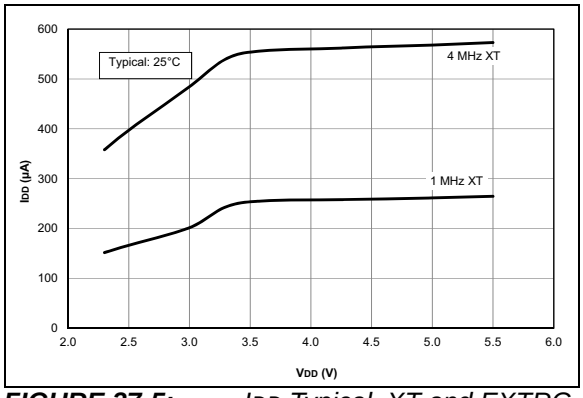


FIGURE 37-5: *IDD Typical, XT and EXTRC Oscillator, PIC16F1777/8/9 Only.*

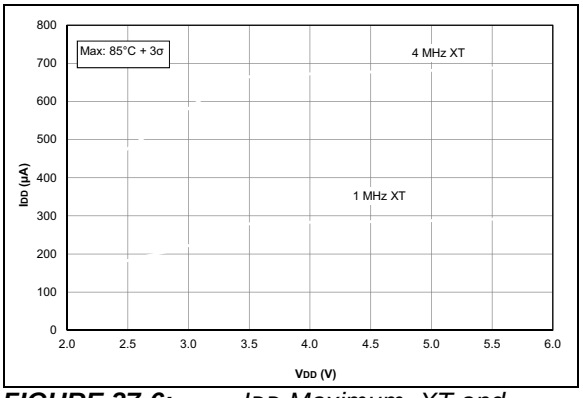


FIGURE 37-6: *IDD Maximum, XT and EXTRC Oscillator, PIC16F1777/8/9 Only.*